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Universal Evaluation Board for Dual, High Speed Op Amps Offered in 8-Lead SOT-23 Packages

FEATURES

Enables quick breadboarding/prototyping
User-defined circuit configuration
Edge-mounted SMA connector provisions
Easy connection to test equipment and other circuits
RoHS Compliant

GENERAL DESCRIPTION

The Analog Devices, Inc., high speed universal evaluation board (EB-O8RJ-2Z) is designed to help customers quickly prototype new dual op amp circuits and reduce design time. The evaluation board can be used with almost any Analog Devices dual op amp in various configurations and applications. Figure 1 shows the component side of the bare evaluation board, and Figure 2 shows the circuit side of the bare evaluation board.

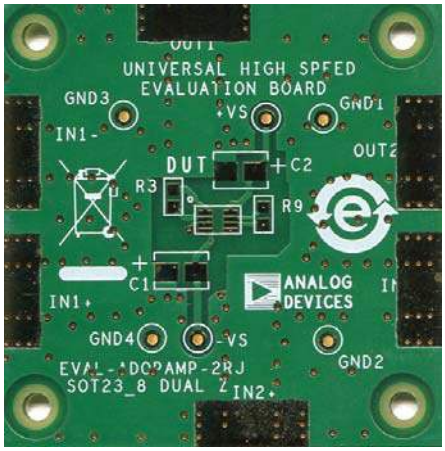
The evaluation board is a 2-layer PCB that accepts SMA connectors on the input and output for efficient connection to test equipment. The ground plane, component placement, and supply bypassing are laid out to minimize parasitic inductances and capacitances. The evaluation board components are primarily SMT 0805 case size, with the exception of the electrolytic bypass capacitors (C1, C2), which are 3528 case size.

There are two options for supply bypassing. The first option is connecting additional shunt capacitors (C3, C4) in parallel with the electrolytic capacitors (C1, C2) from each supply to ground. This technique of power supply bypassing provides wideband rejection of unwanted noise on the supply lines. It is implemented by placing a 0 Ω resistor in the C5 position and shunt capacitors in the C1, C2, C3, and C4 positions.

The second approach to supply bypassing connects one capacitor between the supply rails. This method uses fewer components and can improve the power supply rejection ratio (PSRR) at higher frequencies. It is implemented by inserting a 0 Ω resistor in the C3 position, inserting the bypass capacitor in the C4 position, and omitting C5. Optimal bypassing is circuit dependent and therefore must be evaluated by the designer.

Figure 3 shows the evaluation board schematic. Figure 4 and Figure 6 show the evaluation board assembly drawings. The PCB layout pattern for the component side is shown in Figure 5, and the PCB layout pattern for the circuit side is shown in Figure 7.

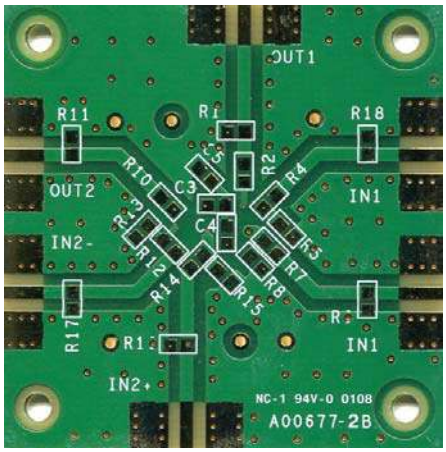
EVALUATION BOARD COMPONENT AND CIRCUIT SIDE DIAGRAMS



NOTES
1. THE EVALUATION BOARD SILKSCREEN PART NUMBER LABELING ON YOUR BOARD MAY BE DIFFERENT FROM WHAT IS SHOWN HERE.

08146-001

Figure 1. EB-O8RJ-2Z Component Side of Evaluation Board



NOTES
1. THE EVALUATION BOARD SILKSCREEN PART NUMBER LABELING ON YOUR BOARD MAY BE DIFFERENT FROM WHAT IS SHOWN HERE.

08146-002

Figure 2. EB-O8RJ-2Z Circuit Side of Evaluation Board

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REVISION HISTORY

4/10—Revision 0: Initial Version

EVALUATION BOARD SCHEMATIC, ASSEMBLY DRAWINGS, AND LAYOUT PATTERNS

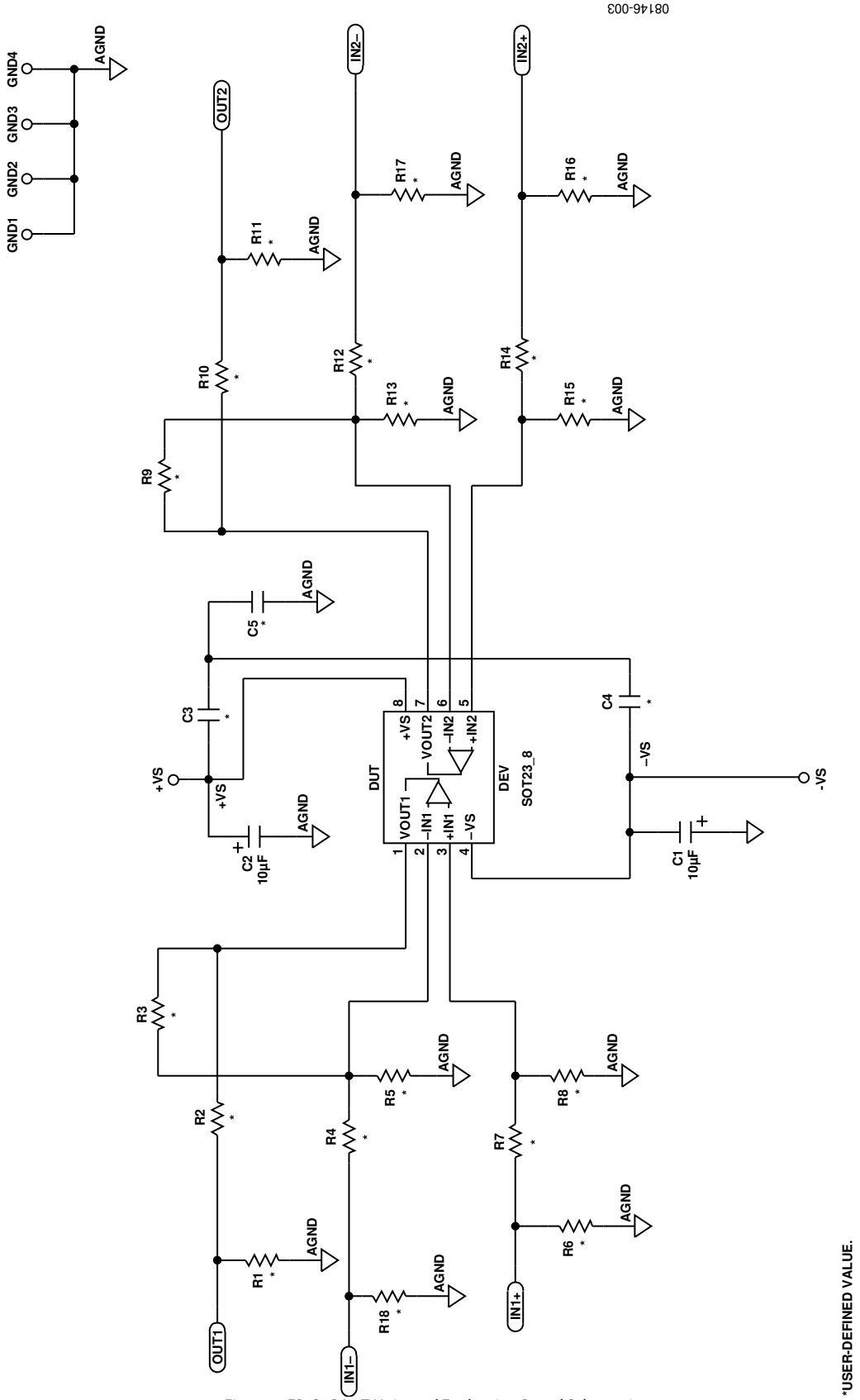

Figure 3. EB-O8RJ-2Z Universal Evaluation Board Schematic

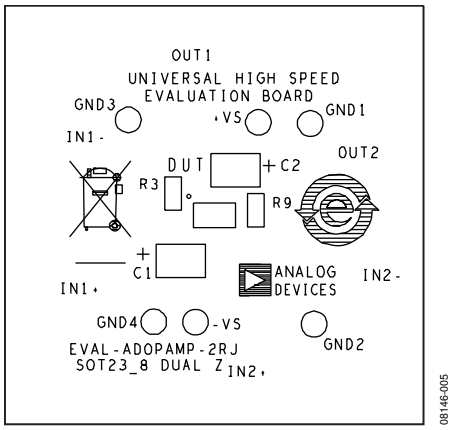

Figure 4. Evaluation Board Assembly Drawing, Component Side

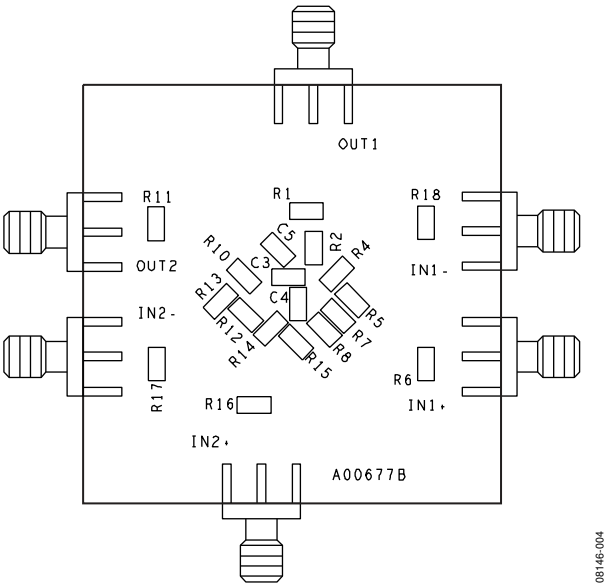

Figure 6. Evaluation Board Assembly Drawing, Circuit Side

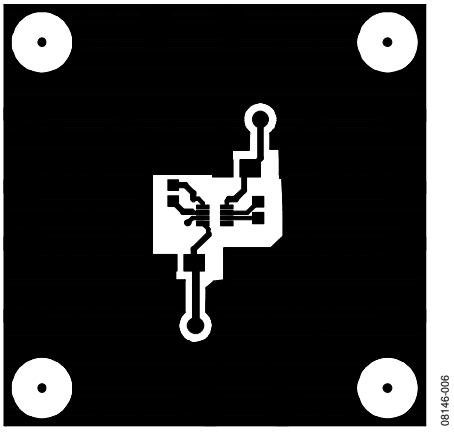

Figure 5. Evaluation Board Layout Pattern, Component Side

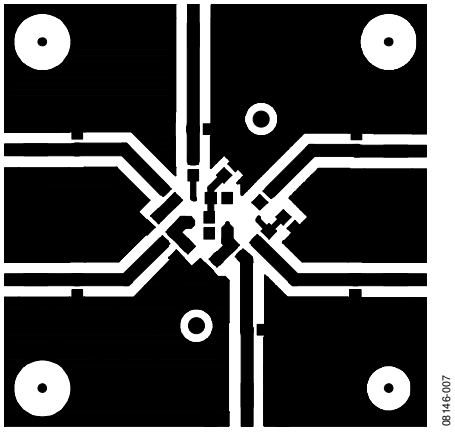

Figure 7. Evaluation Board Layout Pattern, Circuit Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Quantity	Reference Designator	Description	Package
6	+VS, –VS, GND1, GND2, GND3, GND4	Test point	TP
2	C1, C2	10 µF capacitor	C3528
3	C3, C4, C5	User-defined capacitor	C0805
1	DUT	Device under test	SOT-23-8
6	IN1+, IN1–, IN2+, IN2–, OUT1, OUT2	SMA/SMT	SMA/SMT
18	R1 to R18	User-defined resistor	R0805

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ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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