# Host-Side Single Cell Lithium Battery Gauge

## General Description

The RT9428 is a compact, host-side fuel gauge IC for lithium-ion (Li+) battery-powered systems.

For the embedded Fuel Gauge function, the state-of-charge (SOC) calculation is based on the battery voltage information and the dynamic difference between battery voltage and relaxed OCV, by using iteration to estimate the increasing or decreasing SOC.

Voltage-based algorithm can support smoothly SOC and does not accumulate error with time and current. That is an advantage compared to coulomb counter which suffer from SOC drift caused by current-sense error and battery self-discharge. The disadvantage of voltage-based fuel gauge, it can report incremental SOC (%), but can't report capacity (mAh).

A quick sensing operation provides a good initial estimate of the battery's SOC. This feature allows the IC to be located on system side, reducing cost and supply chain constraints on the battery. Measurement and estimated capacity data sets are accessed through an I$^2$C interface.

The RT9428 is available in the WL-CSP-8B 1.6x1.52 (BSC) package.

## Features

- Host-Side Fuel Gauging
- Precision Voltage Measurement ±7.5mV Accuracy
- Accurate Relative Capacity (RSOC) Calculated from Voltaic Gauge Algorithm with Temperature Compensation
- No Accumulation Error on Capacity Calculation
- No Battery Relearning Necessary
- No Current Sense Resistor Required
- External Alarm/Interrupt for Low Battery Alert
- I$^2$C Compatible Interface
- Low Power Consumption
- RoHS Compliant and Halogen Free

## Applications

- Smartphones
- Tablet PC
- Digital Still Cameras
- Digital Video Cameras
- Handheld and Portable Applications

## Simplified Application Circuit
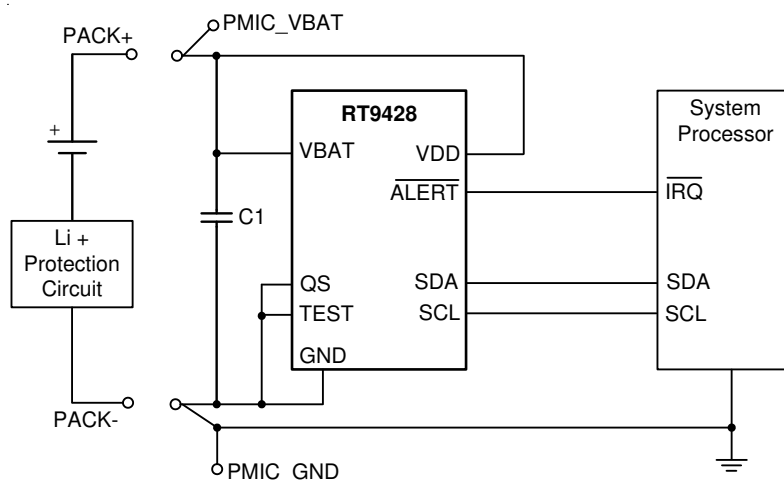
# RT9428

## Ordering Information
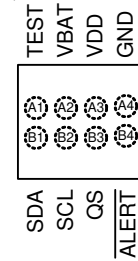
RT9428 □

└ Package Type
　WSC : WL-CSP-8B 1.6x1.52 (BSC)

Note :

Richtek products are :

▸ RoHS compliant and compatible with the current require-
ments of IPC/JEDEC J-STD-020.
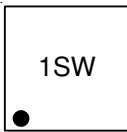
▸ Suitable for use in SnPb or Pb-free soldering processes.

## Pin Configuration

(TOP VIEW)

TEST　VBAT　VDD　GND

(A1) (A2) (A3) (A4)
(B1) (B2) (B3) (B4)

SDA　SCL　QS　ALERT

WL-CSP-8B 1.6x1.52 (BSC)

## Marking Information

1SW
●

1S : Product Code

W : Date Code

## Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---------|----------|--------------|
| A1 | TEST | Test pin. Connect to GND pin during normal operation. |
| A2 | VBAT | Battery voltage measurement input. |
| A3 | VDD | Processor power input. Decouple with a 10nF capacitor. |
| A4 | GND | Ground. |
| B1 | SDA | Serial data input. Slave $I^2C$ data line for communication with system. Open-drain I/O. |
| B2 | SCL | Serial clock input. Slave $I^2C$ clock line for communication with system. |
| B3 | QS | Quick sensing input. Active high to restart the calculation. Pull low to GND during normal operation. |
| B4 | $\overline{\text{ALERT}}$ | Alert output. When SOCLow condition is detected, It outputs low as interrupt signal. Connect to interrupt input of the system processor. Connect to GND if not used. |

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## Functional Block Diagram
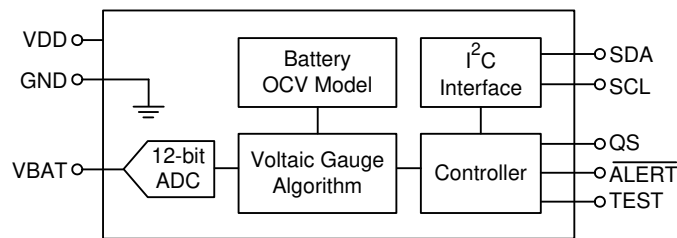


## Operation

### 12-bit ADC

Analog-to-Digital Converter. It converts the voltage input from VBAT pin to target value.

### Battery OCV Model

Parameters for battery characteristics.

### Voltaic Gauge Algorithm

The RT9428 calculates and determines that the embedded Fuel Gauge calculates and determines the Li+ battery SOC according to battery voltage only.

The algorithm estimates the increasing or decreasing SOC by an iteration model according to the difference between battery voltage and the battery OCV. The dynamic voltaic information can effectively emulate the Li+ battery behavior and determines the SOC (%), but can't report capacity (mAh).

### Controller

The controller takes care of the control flow of system routine, ADC measurement flow, algorithm calculation and alert determined.

### I²C Interface

The fuel gauge registers can be accessed through the I²C Interface.

## Absolute Maximum Ratings    (Note 1)

- Voltage on TEST Pin Relative to GND ------------------------------------------------------------------------------------- −0.3V to 5.5V
- Voltage on VBAT Pin Relative to GND ------------------------------------------------------------------------------------- −0.3V to 5.5V
- Voltage on All Other Pins Relative to GND ------------------------------------------------------------------------------- −0.3V to 6V
- SCL, SDA, QS, $\overline{\text{ALERT}}$ to GND ------------------------------------------------------------------------------------------- −0.3V to 5.5V
- VBAT to GND ------------------------------------------------------------------------------------------------------------------ −0.3V to 5V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  WL-CSP-8B 1.6x1.52 (BSC) ------------------------------------------------------------------------------------- 0.87W
- Package Thermal Resistance  (Note 2)
  WL-CSP-8B 1.6x1.52 (BSC), $\theta_{JA}$ ------------------------------------------------------------------------------- 114.4°C/W
- Lead Temperature (Soldering, 10 sec.) ------------------------------------------------------------------------------ 260°C
- Junction Temperature Range ------------------------------------------------------------------------------------------ 150°C
- Storage Temperature Range -------------------------------------------------------------------------------------- −65°C to 150°C

## Recommended Operating Conditions    (Note 3)

- Supply Voltage, VDD ------------------------------------------------------------------------------------------------------ 2.5V to 4.5V
- Junction Temperature Range ------------------------------------------------------------------------------------------ −40°C to 125°C
- Ambient Temperature Range ------------------------------------------------------------------------------------------ −40°C to 85°C

## Electrical Characteristics

(2.5V ≤ $V_{DD}$ ≤ 4.5V, $T_A$ = 25°C unless otherwise specified)   (Note 4)

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **DC Section** | | | | | | | |
| Active Current | | $I_{ACTIVE}$ | | -- | 22 | 40 | μA |
| Sleep-Mode Current    (Note 5) | | $I_{SLEEP}$ | $V_{DD}$ = 2.5V | -- | 0.5 | 1 | μA |
| | | | | -- | 1 | 3 | |
| Time-Base Accuracy | | $t_{ERR}$ | $T_A$ = −20°C to 70°C    (Note 4) | −3.5 | ±1 | 3.5 | % |
| Voltage Measurement Error | | $V_{GERR}$ | $V_{BAT}$ = 4V | −7.5 | -- | 7.5 | mV |
| | | | $T_A$ = −20°C to 70°C    (Note 4) | −20 | -- | 20 | |
| VBAT Pin Input Impedance | | $R_{VBAT}$ | | 15 | -- | -- | MΩ |
| SCL, SDA, QS Input Voltage | Logic-High | | All voltage reference to GND | 1.4 | -- | -- | V |
| | Logic-Low | | All voltage reference to GND | -- | -- | 0.5 | |
| SDA Output Logic-Low | | $V_{OL\_SDA}$ | $I_{OL\_SDA}$ = 4mA, All voltage reference to GND | -- | -- | 0.4 | V |
| $\overline{\text{ALERT}}$ Output Logic-Low | | $V_{OL\_\overline{ALERT}}$ | $I_{OL\_\overline{ALERT}}$ = 2mA, All voltage reference to GND | -- | -- | 0.4 | V |
| SCL, SDA Pull-Down Current | | $I_{PD}$ | $V_{DD}$ = 4.5V, $V_{SCL}$ = $V_{SDA}$ = 0.4V | -- | 0.2 | 0.4 | μA |
| Bus Low Timeout | | $t_{SLEEP}$ | (Note 6) | 2 | -- | 3 | s |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **I$^2$C Interface** | | | | | | |
| Clock Operating Frequency | $f_{SCL}$ | (Note 7) | 10 | -- | 250 | kHz |
| Bus Free Time Between a STOP and START Condition | $t_{BUF}$ | | 1.3 | -- | -- | μs |
| Hold Time After START Condition | $t_{HD\_STA}$ | (Note 7) | 0.6 | -- | -- | μs |
| Low Period of the SCL Clock | $t_{LOW}$ | | 1.3 | -- | -- | μs |
| High Period of the SCL Clock | $t_{HIGH}$ | | 0.6 | -- | -- | μs |
| Setup Time for a Repeated START Condition | $t_{SU\_STA}$ | | 0.6 | -- | -- | μs |
| Data Hold Time | $t_{HD\_DAT}$ | (Note 8, Note 9) | 0.2 | -- | 0.9 | ms |
| Data Setup Time | $t_{SU\_DAT}$ | (Note 8) | 100 | -- | -- | ns |
| Clock Data Rising Time | $t_R$ | | 20 | -- | 300 | ns |
| Clock Data Falling Time | $t_F$ | | 20 | -- | 300 | ns |
| Set-Up Time for STOP Condition | $t_{SU\_STO}$ | | 0.6 | -- | -- | μs |
| Spike Pulse Widths Suppressed by Input Filter | $t_{SP}$ | (Note 10) | 0 | -- | 50 | ns |
| Capacitive Load for Each Bus Line | $C_B$ | (Note 11) | 400 | -- | -- | pF |
| SCL, SDA Input Capacitance | $C_{BIN}$ | | -- | -- | 60 | pF |

**Note 1.** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** $\theta_{JA}$ is measured at $T_A$ = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. $\theta_{JC}$ is measured at the exposed pad of the package.

**Note 3.** The device is not guaranteed to function outside its operating conditions.

**Note 4.** Specifications are 100% tested at $T_A$ = 25°C. Limits over the operating range are guaranteed by design and characterization.

**Note 5.** SDA, SCL = GND; QS, $\overline{ALERT}$ idle.

**Note 6.** The RT9428 enter sleep mode after SCL and SDA low for longer than 3s.

**Note 7.** $f_{SCL}$ must meet the minimum clock low time plus the rise/fall time.

**Note 8.** The maximum $t_{HD\_DAT}$ has only to be met if the device does not stretch the low period ($t_{LOW}$) of the SCL signal.

**Note 9.** This device internally provides a hold time of at least 75ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

**Note 10.** Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.
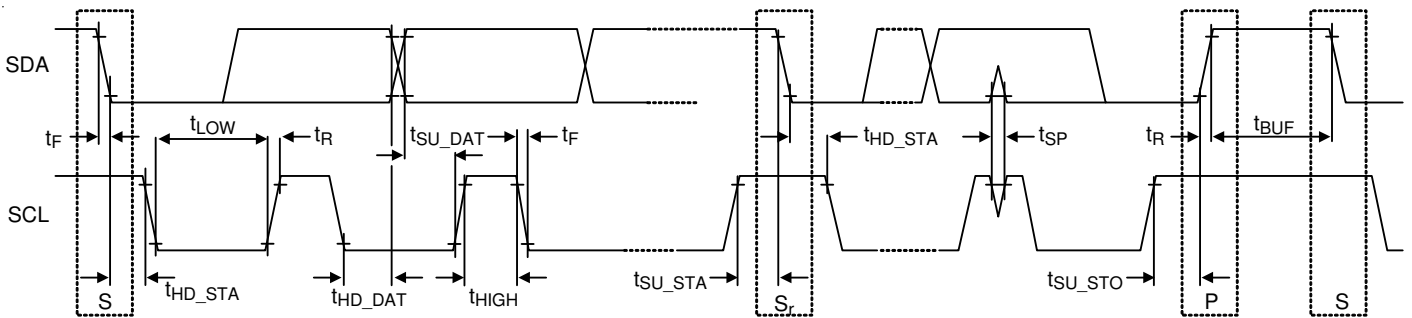
**Note 11.** $C_B$ total capacitance of one bus line in pF.
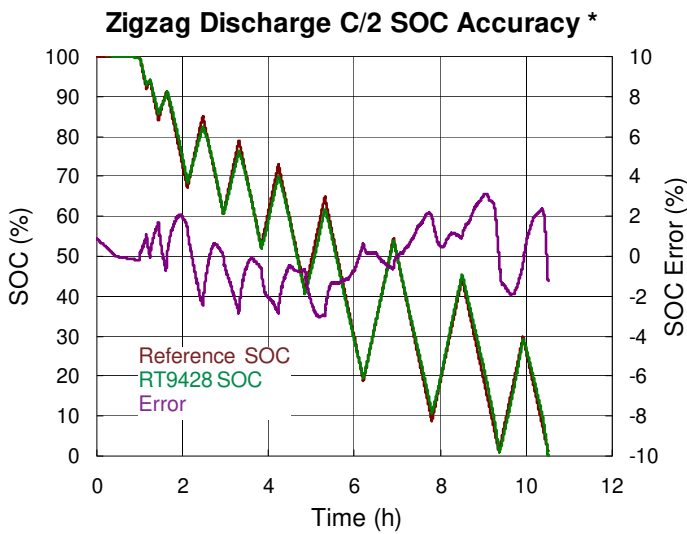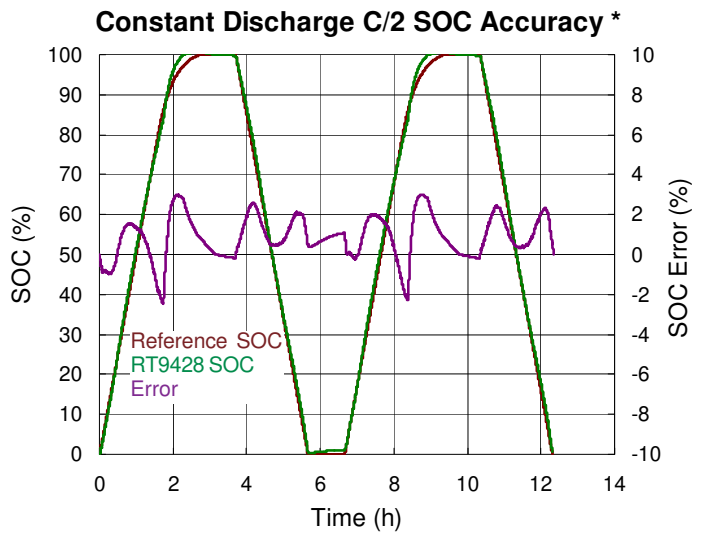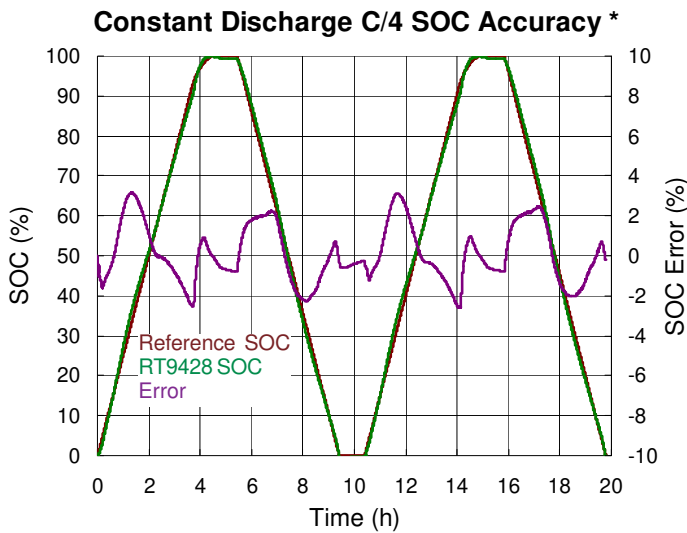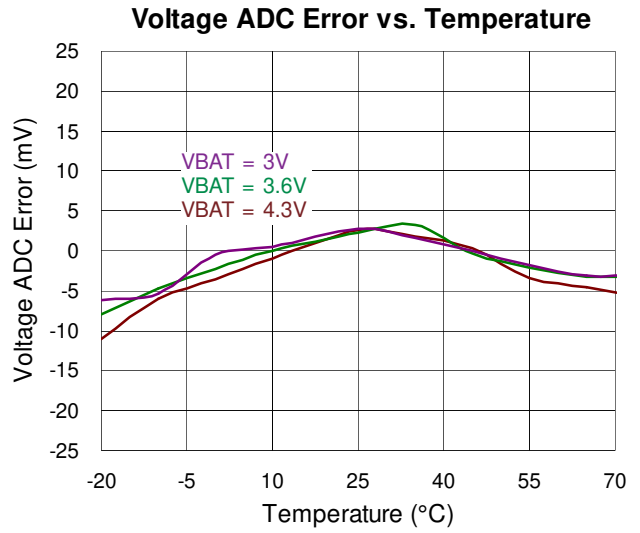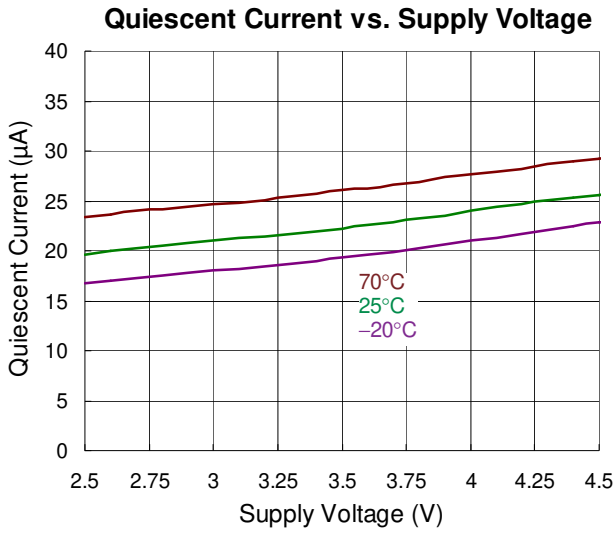
## Typical Application Circuit
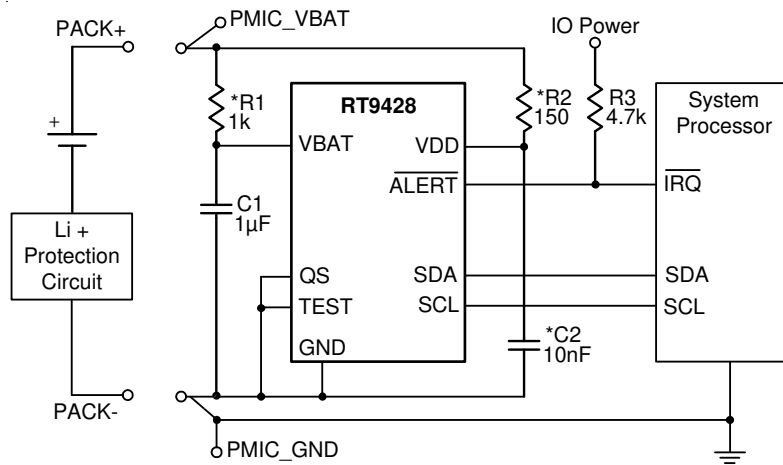


* : For better noise reduction performance and improve measurement accuracy, add R1 R2 C2 are optional and recommended.

## Timing Diagram

# Typical Operating Characteristics

($T_A$ = 25°C, battery is Sanyo UF534553F, unless otherwise specified.)

**Quiescent Current vs. Supply Voltage**

**Voltage ADC Error vs. Temperature**

**Constant Discharge C/4 SOC Accuracy \***

**Constant Discharge C/2 SOC Accuracy \***

**Zigzag Discharge C/2 SOC Accuracy \***

\* : Sample accuracy with custom parameters into the IC.

## Application Information

**Voltaic Gauge Theory and Performance**

The embedded Fuel Gauge calculates and determines the Li+ battery SOC according to battery voltage only.

The algorithm estimates the increasing or decreasing SOC by an iteration model according to the difference between battery voltage and the battery OCV. The dynamic voltaic information can effectively emulate the Li+ battery behavior and determines the SOC (%), but can't report capacity (mAh).

The calculation is based on the battery voltage information and the dynamic difference between battery voltage and relaxed OCV, by using iteration algorithm to estimate the increasing or decreasing SOC to calculate SOC. Comparing to coulomb counter based fuel gauge solution; voltaic gauge does not accumulate error with time and current. The coulomb counter based fuel gauge suffers from SOC drift due to current-sense error and cell self-discharge. Even there is a very small current sensing error, the coulomb counter accumulates the error from time to time. The accumulated error can be eliminated by only full charged or full discharged. The VoltaicGauge estimates battery SOC by only voltage information and will not accumulate error because it does not rely on battery current information.

**Power On**

When the IC is powered on by the battery insertion, the IC measures the battery voltage quickly and predicts the first SOC according to the voltage. The first SOC would be accurate if the battery has been well relaxed for over 30 min. Otherwise, the initial SOC error occurs.

However, the initial SOC error will be convergent and the SOC will be adjusted gradually and finally approach to the accurate SOC without accumulation error.

**Quick Sensing**

A Quick Sensing operation allows the RT9428 to restart sensing and SOC calculation. It has the same behavior as power on. The operation is used to reduce the initial SOC error caused by unwell power-on sequence. A Quick Sensing operation could be performed by either a rising edge on the QS pin or I²C Quick Sensing command to the Control register.

QS pin active high to restart the SOC calculation, and pull low to GND during normal operation.

**Temperature Compensation**

To maximize the SOC performance, the host must measure battery temperature periodically, and compensate the VGCOMP Voltaic-Gauge parameter at least once per minute.

Contact Richtek for instructions for temperature compensation.

**ALERT Interrupt**

The RT9428 monitors the SOC and reports the alert condition if the SOC change over 1% or if the SOC falls below the SOCLow which is in the Config (0Dh) register.

When alert condition occurs, the RT9428 outputs logic-low to the $\overline{ALERT}$ pin and sets 1 to the [Alert] bit in the Config register and sets 1 to the corresponding alert flag in the Status register. The only three ways to recover the alert condition is writing 0 to clear [Alert] bit or writing 0 to clear both [SL] and [SC] bit or power on reset. Before the recovery, the [Alert] bit will keep 1 and the $\overline{ALERT}$ pin will keep logic-low. It can't recover the alert condition by entering sleep mode.

Please note that the SOC low alert detection function is enable when power on.

**Sleep Mode**

RT9428 will enter sleep mode if host pulls low both SDA and SCL to logic-low at least 2.5s. All operation such as voltage measurement and SOC calculation are halted and power consumption is reduced under 3μA in sleep mode. Any rising edge of SDA or SCL will transfer IC back to active mode immediately.

The other way to enter sleep mode is write [Sleep] bit in the Config register to 1 through I²C communication, and the only way to exit sleep mode is to write [Sleep] bit to logic 0 or power on reset the IC.

## Initialization

The RT9428 can be reset by writing an initialization command to MFA resister. The behavior of initialization is the same as power on reset.

## I²C Register

The RT9428 supports the following 16-bit I²C registers: VBAT, SOC, Control, Device ID, Config and MFA.

The register writing is valid when all of 16 bits data are transferred; otherwise, the write data will be ignored. The valid register addresses are defined in Table 1. Other remaining addresses are reserved.

**Table 1. I²C Register**

| Address (Hex) | Register | Description | Read/ Write | Default (Hex) |
|---|---|---|---|---|
| 02h-03h | VBAT | It reports voltage measured from the input of VBAT pin. | R | -- |
| 04h-05h | SOC | It reports the SOC result calculated by voltaic-gauge algorithm. | R | -- |
| 06h-07h | Control | It's the command interface for special function such as Quick Sensing. | W | -- |
| 08h-09h | Device ID | It reports the device ID. | R | -- |
| 0Ah | Status | It reports alert status. | R/W | 01h |
| 0Bh | dSOC | It reports approximately incremental SOC in unit of 1% per hour. | R | -- |
| 0Ch-0Dh | Config | The Config register includes the parameter of compensation, setting of sleep mode and SOCLow threshold. It also indicates the alert status. | R/W | 321Ch |
| 0Eh-0Fh | OCV | It reports Open Circuit Voltage corresponding to present SOC in unit of 1.25mV. | R | -- |
| FEh-FFh | MFA | Manufacturer Access. Sends special commands to the IC for the manufacturing. | W | -- |

## VBAT

The VBAT register is a read only register that reports the measured voltage at VBAT pin. The VBAT is reported in units of 1.25mV. The first report is made after chip POR with 250ms delay and then updates 1s periodically. Figure 1 shows the VBAT register format.
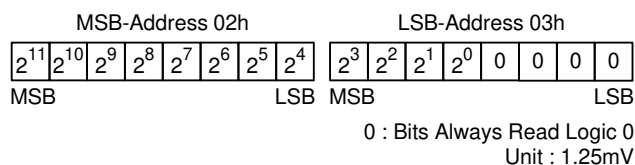
MSB-Address 02h  LSB-Address 03h

| $2^{11}$ | $2^{10}$ | $2^9$ | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ | 0 | 0 | 0 | 0 |

0 : Bits Always Read Logic 0
Unit : 1.25mV

Figure 1. VBAT Register

## SOC

The SOC register is a read only register that returns the relative state of charge of the cell as calculated by the voltaic gauge algorithm. The result is displayed as a percentage of the cell's full capacity. The high byte is reported in units of %. The low byte is reported in units of 1/256%. Figure 2 shows the SOC register format.
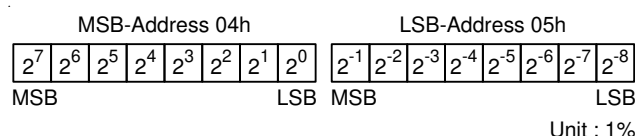
MSB-Address 04h  LSB-Address 05h

| $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ | $2^{-6}$ | $2^{-7}$ | $2^{-8}$ |

Unit : 1%

Figure 2. SOC Register

## Control

The Control register allows the host processor to send special commands to the IC (Table2). Valid Control register write values are listed as follows. All other Control register values are reserved.

**Table 2. Control Register Commands**

| Value | Command | Description |
|---|---|---|
| 4000h | Quick Sensing | Restart sensing and SOC calculation |

## Device ID

The Device ID register is a read only register that contains a value indicating the production ID of the RT9428.

## dSOC

The dSOC register is a read only registert that reports the approximately incremetal SOC in unit of 1% per hour.

## Config

The Config register includes the parameter of compensation, setting of sleep mode and SOCLow threshold. It also indicates the alert status. The format of Config is shown in Figure 3.

VGCOMP is the setting to optimize IC performance for different cell chemistries or temperatures. Contact Richtek for instructions for optimization. The power on reset value for VGCOMP is 32h.

| Register | Bit | Description |
|---|---|---|
| 0x0C | 7 : 0 | VGCOMP |
| 0x0D | 7 | Sleep |
| | 6 | SCEN |
| | 5 | Alert |
| | 4 : 0 | SOCLow |

Figure 3. Config Register

## [Sleep]

Writing [Sleep] to logic 1 forces the IC to enter Sleep mode. Writing [Sleep] to logic 0 forces the IC to exit Sleep mode. The power on reset value for [Sleep] is logic 0.

[SCEN]

Writing [SCEN] to logic 1 to enable SOC Change Alert. When SOC Change Alert is enabled, the [SC] flag is set to 1 if SOC is changed at least 1%. The power on reset value for [SCEN] is logic 0.

## [Alert]

The [Alert] bit is set by the IC when the alert condition occurs. The [Alert] bit is cleared by either host writing 0 to clear or a reset condition occurs.

The power on reset value for [Alert] is logic 0.

## [SOCLow]

The SOCLow is a 5-bit value for setting the low battery alert threshold and defined as 2's-complement form. The programming unit is 1% and range is 32% to 1%. (00000 = 32%, 10001 = 15%, 11100 = 4%, 11111 = 1%). The power on reset value for SOCLow is 4% or 1Ch.

## MFA

The MFA register allows the host processor to send special commands to the chip for manufacturing. Valid MFA register write values are listed as follows. All other MFA register values are reserved. Table 3 shows MFA register commands.

Table 3. MFA Register Commands

| Value | Command | Description |
|---|---|---|
| 5400h | Initialization | Reset the IC |

## Status

The Status register reports the alert status of RT9428. When any alert flag of Status register is set, the [Alert] flag of Config register will be set.

## [SC]

The [SC] flag is set when SOC changes at least 1%. The [SC] flag is cleared by either host writing 0 to clear or a reset condition occurs. The power on reset value of [SC] is logic 0.

## [SL]

The [SL] flag is set when SOC is lower than SOC threshold set by [SOCLow] bits. The [SL] flag is cleared by either host writing 0 to clear or a reset condition occurs. The power on reset value of [SL] is logic 0.

## [RI]

The [RI] flag is set at POR and could be cleared after configuration. The power on reset value of [RI] is logic 1.

## OCV

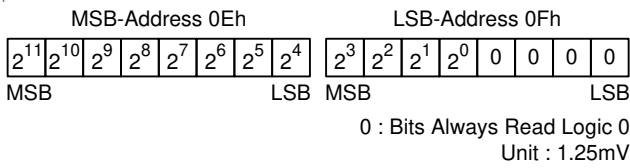The OCV register reports Open Circuit Voltage corresponding to present SOC in unit of 1.25mV.

MSB-Address 0Eh

| $2^{11}$ | $2^{10}$ | $2^9$ | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ |
|---|---|---|---|---|---|---|---|

MSB          LSB

LSB-Address 0Fh

| $2^3$ | $2^2$ | $2^1$ | $2^0$ | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|

MSB          LSB

0 : Bits Always Read Logic 0
Unit : 1.25mV

Figure 4. OCV Register

| Register | Bit | Description |
|---|---|---|
| | 7 : 6 | Reserved |
| | 5 | SC |
| 0x0A | 4 | SL |
| | 3 : 1 | Reserved |
| | 0 | RI |

Figure 5. Status Register
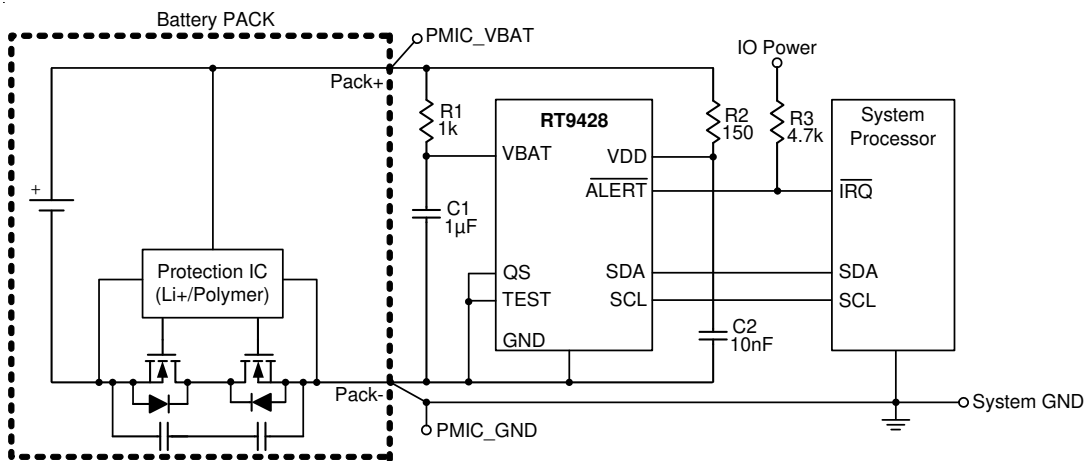


Figure 6. RT9428 Application Example with Alert Interrupt

Figure 6 presents a single cell battery-powered system application. The RT9428 is used on system side and direct powered from the battery.

The RC filter saves the noise for IC power supply and voltage measurement on VBAT pin.

To reduce the I-R drop effect, make the connection of VBAT as close as possible to the battery pack.

The $\overline{\text{ALERT}}$ pin provides a battery low interrupt signal to system processor when capacity low is detected.

The QS pin is unused in this configuration, so it needs to be tied to GND.

## I$^2$C Bus Interface

Figure 7 shows the timing diagram of the I$^2$C interface.

The RT9428 communicates with a host (master) by using the standard I$^2$C 2-wire interface. After the START condition, the I$^2$C master sends 8-bit data, consisting of 7-bit slave address and a following data direction bit (R/W).

A byte of data consists of 8 bits ordered MSB first and the LSB followed by the Acknowledge bit.

The RT9428 address is 0110110 (6Ch) and is a receive only (slave) device. The second word selects the register to which the data will be written. The third word contains data to write to the selected register.
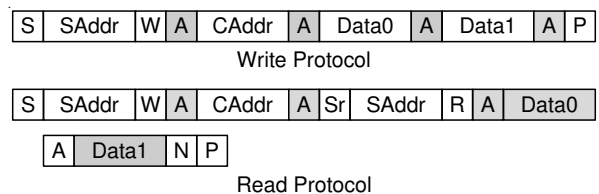
Table 4 applies to the transaction formats.



Figure 7. I$^2$C Timing Diagram

**Table4. 2-Wire Protocol**

| Symbol | Description | Symbol | Description |
|--------|-------------|--------|-------------|
| S | START bit | Sr | Repeated START |
| SAddr | Slave address (7bit) | R/W | Read : R/W = 1; Write : R/W = 0 |
| CAddr | Command address (byte) | P | STOP bit |
| Data | Data byte written by master | Data | Data byte returned by slave |
| A | Acknowledge bit written by master | A | Acknowledge bit returned by slave |
| N | No acknowledge bit written by master | N | No acknowledge bit returned by slave |

## Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. For WL-CSP-8B 1.6x1.52 (BSC) package, the thermal resistance, $\theta_{JA}$ is 114.4°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at $T_A = 25$°C can be calculated by the following formula :

$$P_{D(MAX)} = (125°C - 25°C) / (114.4°C/W) = 0.87W \text{ for}$$
WL-CSP-8B 1.6x1.52 (BSC) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, $\theta_{JA}$. The derating curve in Figure 8 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.
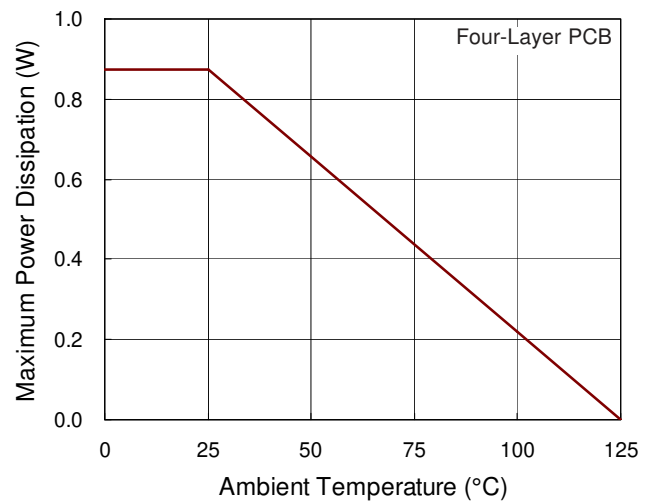


Figure 8. Derating Curve of Maximum Power Dissipation
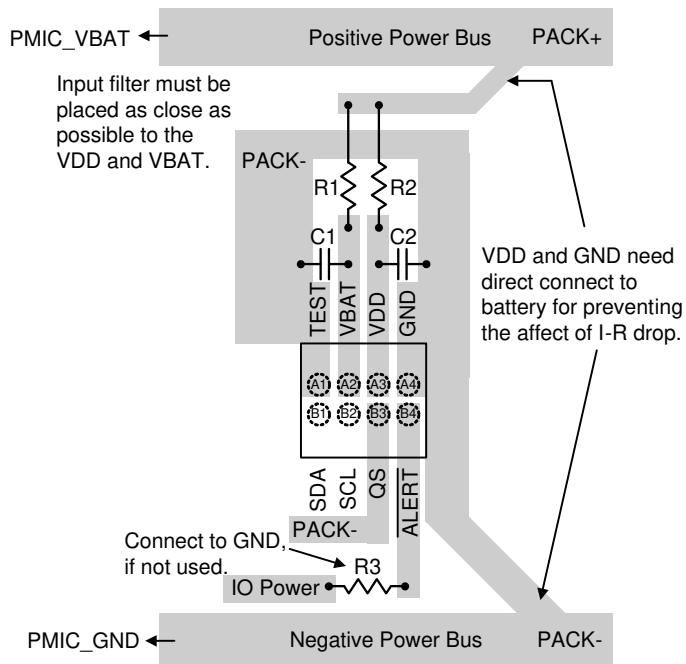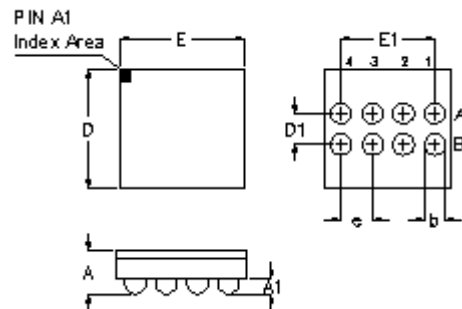
**Layout Considerations**



Figure 9. PCB Layout Guide

## Outline Dimension



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.500 | 0.600 | 0.020 | 0.024 |
| A1 | 0.170 | 0.230 | 0.007 | 0.009 |
| b | 0.240 | 0.300 | 0.009 | 0.012 |
| D | 1.470 | 1.570 | 0.058 | 0.062 |
| D1 | 0.400 | | 0.016 | |
| E | 1.550 | 1.650 | 0.061 | 0.065 |
| E1 | 1.200 | | 0.047 | |
| e | 0.400 | | 0.016 | |

**8B WL-CSP 1.6x1.52 Package (BSC)**

## Footprint Information
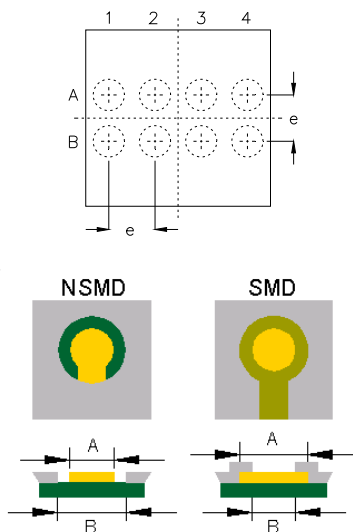


| Package | Number of Pin | Type | Footprint Dimension (mm) | | | Tolerance |
|---------|---------------|------|------|------|------|-----------|
| | | | e | A | B | |
| WL-CSP1.6x1.52-8(BSC) | 8 | NSMD | 0.400 | 0.240 | 0.340 | ±0.025 |
| | | SMD | | 0.270 | 0.240 | |

## Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789