

General Description

- Trench Power MV MOSFET technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- Logic level driven

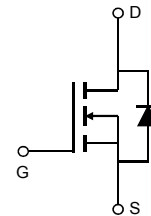
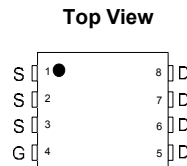
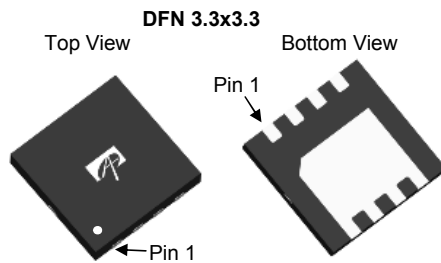
Applications

- Synchronous Rectification in DC/DC and AC/DC Converters
- Synchronous Rectification in cell phone Quick Charger

Product Summary

V_{DS}	100V
I_D (at $V_{GS}=10V$)	47A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 11.5m Ω
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 15.5m Ω

100% UIS Tested
 100% Rg Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AON7230	DFN 3.3x3.3	Tape & Reel	3000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	47
		$T_C=100^\circ\text{C}$	30
Pulsed Drain Current ^C	I_{DM}	125	A
Continuous Drain Current	I_{DSM}	$T_A=25^\circ\text{C}$	13
		$T_A=70^\circ\text{C}$	10
Avalanche Current ^C	I_{AS}	33	A
Avalanche energy $L=0.1\text{mH}$ ^C	E_{AS}	54	mJ
V_{DS} Spike	V_{SPIKE}	120	V
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	54
		$T_C=100^\circ\text{C}$	21
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	4.1
		$T_A=70^\circ\text{C}$	2.6
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	25	30	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A D}		Steady-State	50	60
Maximum Junction-to-Case	$R_{\theta JC}$	1.8	2.3	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	100			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.5	1.95	2.5	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =13A T _J =125°C		9.5 18	11.5 22	mΩ
		V _{GS} =4.5V, I _D =11A		12	15.5	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =13A		55		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current				47	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =50V, f=1MHz		2320		pF
C _{oss}	Output Capacitance			175		pF
C _{rss}	Reverse Transfer Capacitance			11		pF
R _g	Gate resistance	f=1MHz	0.7	1.4	2.1	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =50V, I _D =13A		30	45	nC
Q _{g(4.5V)}	Total Gate Charge			13	21	nC
Q _{gs}	Gate Source Charge			7		nC
Q _{gd}	Gate Drain Charge			3		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =50V, R _L =3.85Ω, R _{GEN} =3Ω		8		ns
t _r	Turn-On Rise Time			4		ns
t _{D(off)}	Turn-Off DelayTime			27		ns
t _f	Turn-Off Fall Time			5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =13A, di/dt=500A/μs		25		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =13A, di/dt=500A/μs		120		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

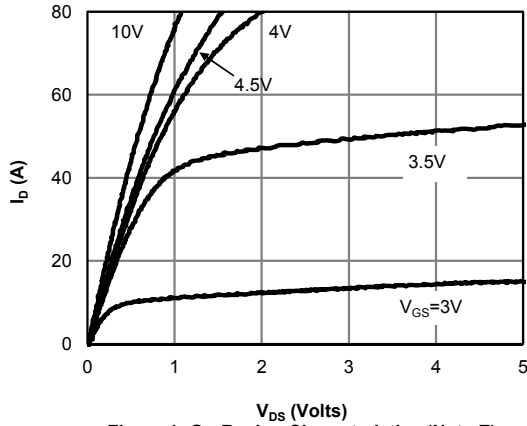


Figure 1: On-Region Characteristics (Note E)

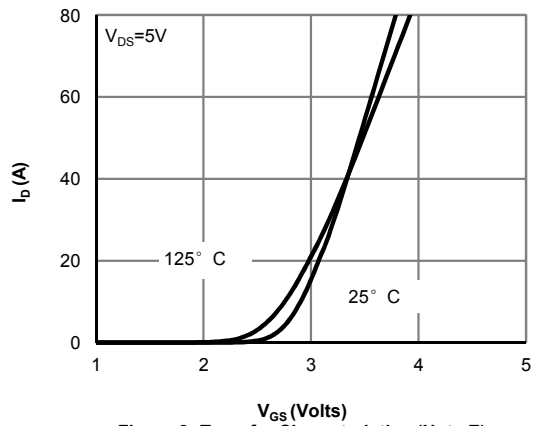


Figure 2: Transfer Characteristics (Note E)

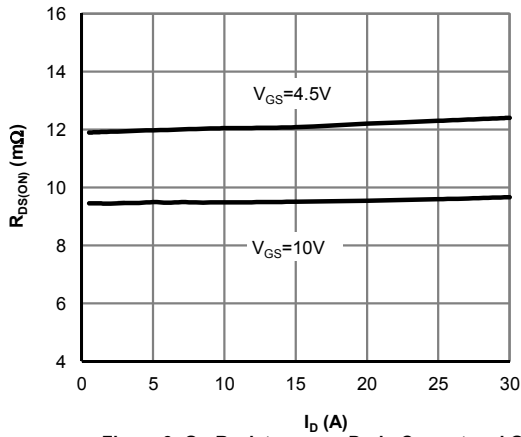


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

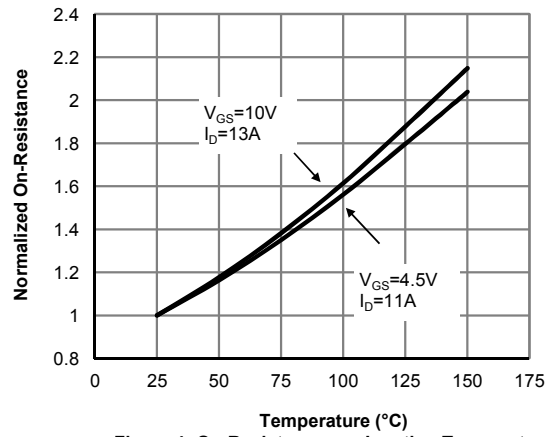


Figure 4: On-Resistance vs. Junction Temperature (Note E)

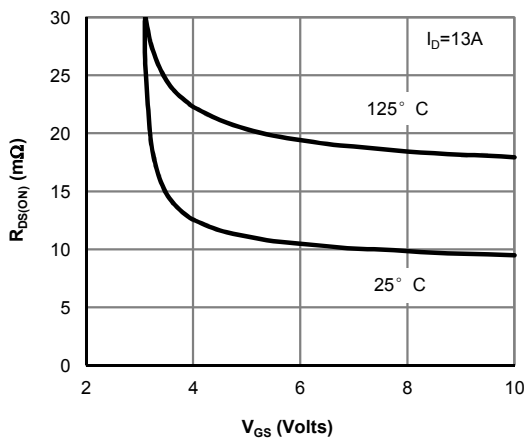


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

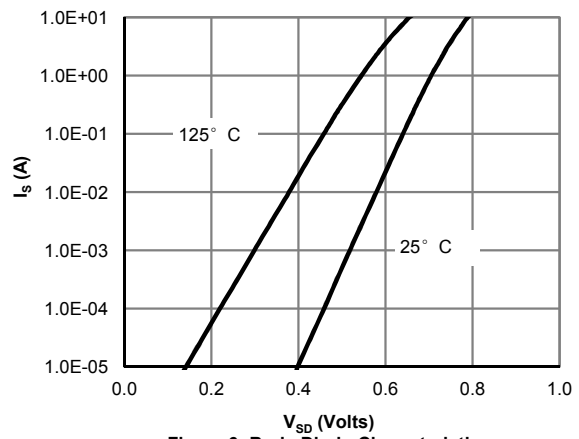


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

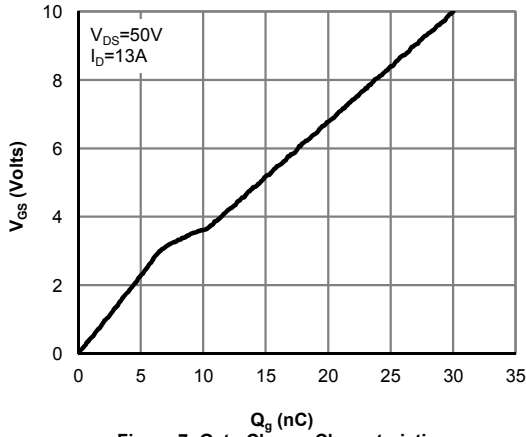


Figure 7: Gate-Charge Characteristics

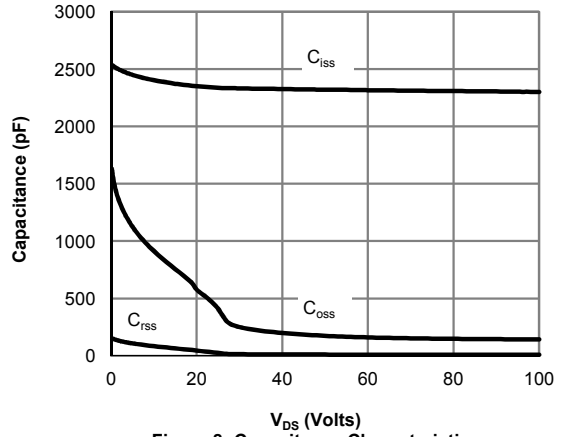


Figure 8: Capacitance Characteristics

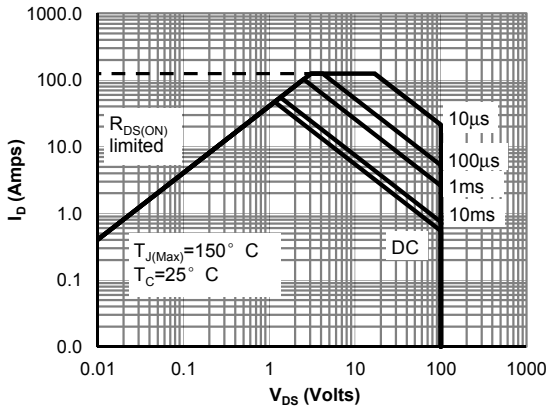


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

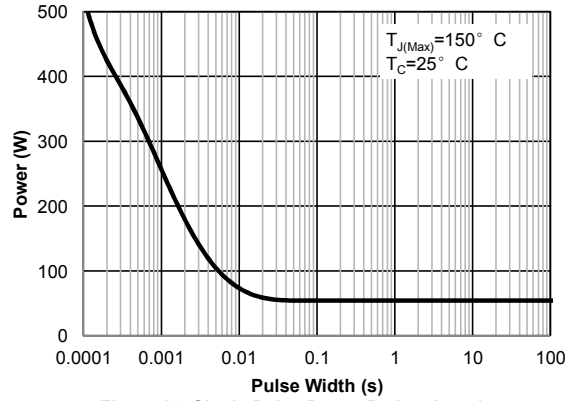


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

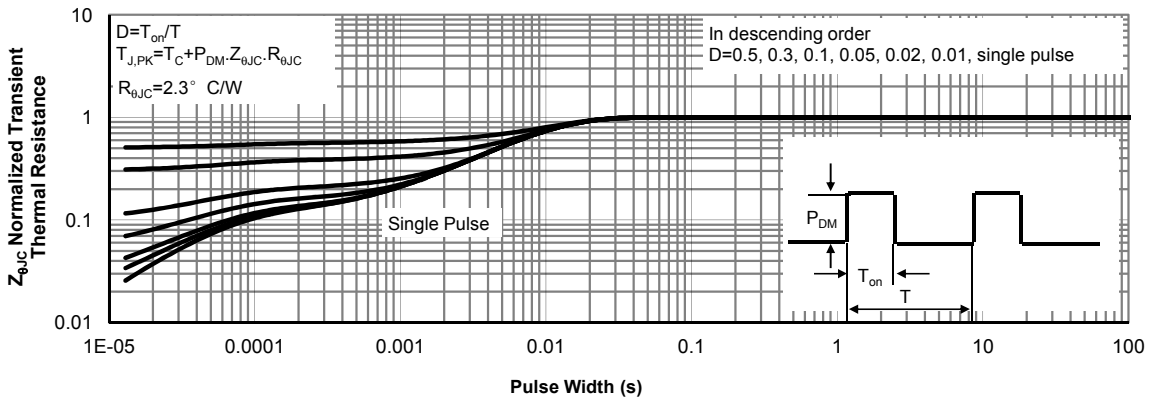


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

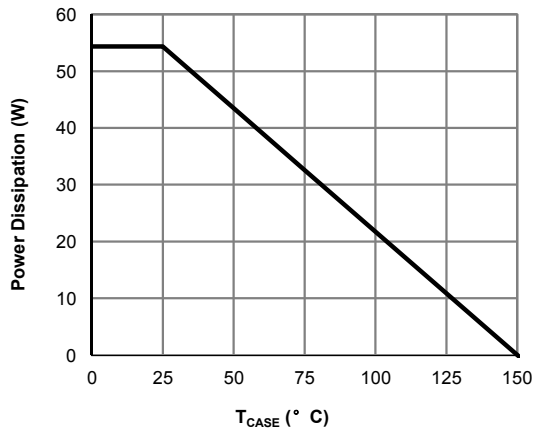


Figure 12: Power De-rating (Note F)

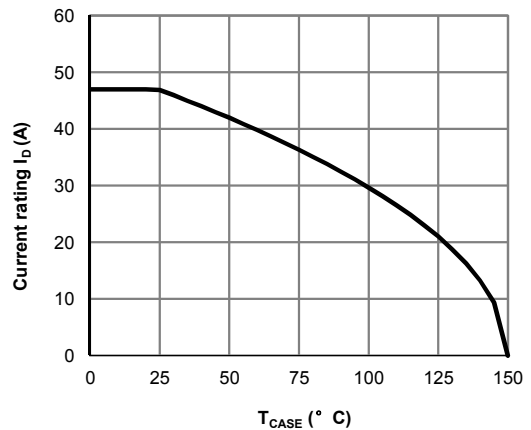


Figure 13: Current De-rating (Note F)

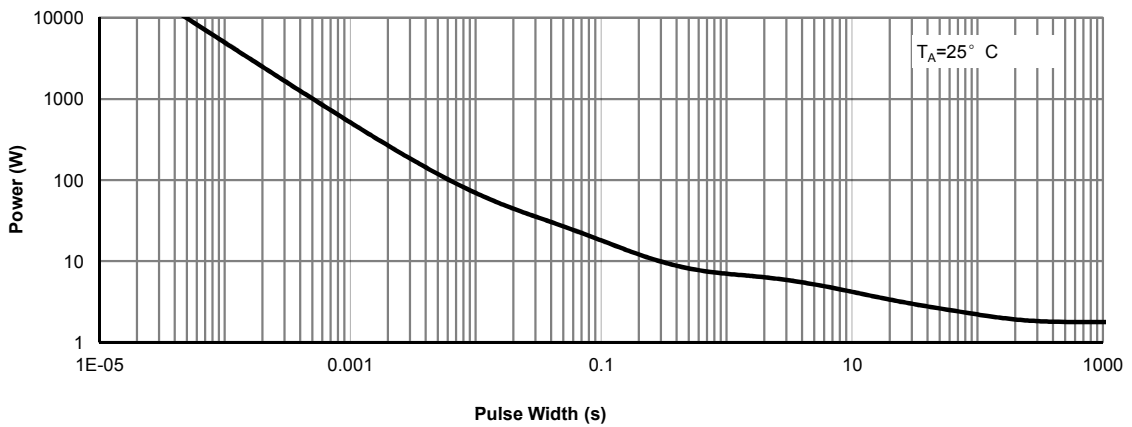


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

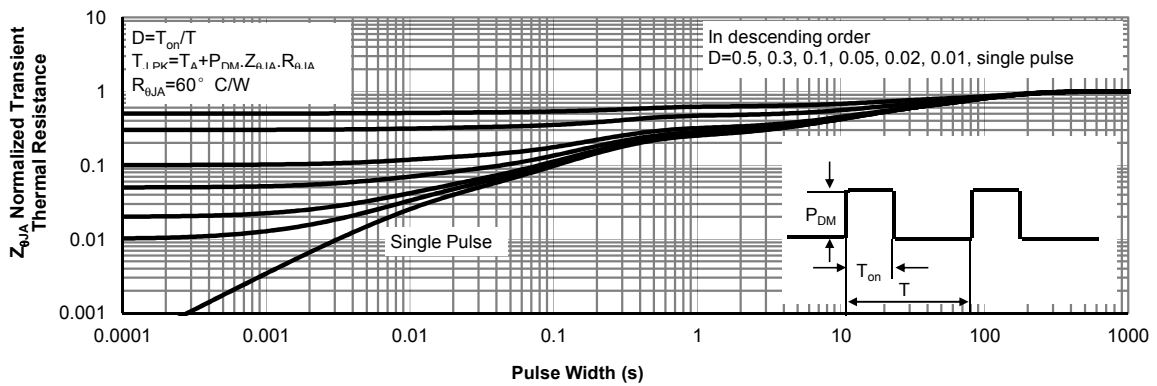


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

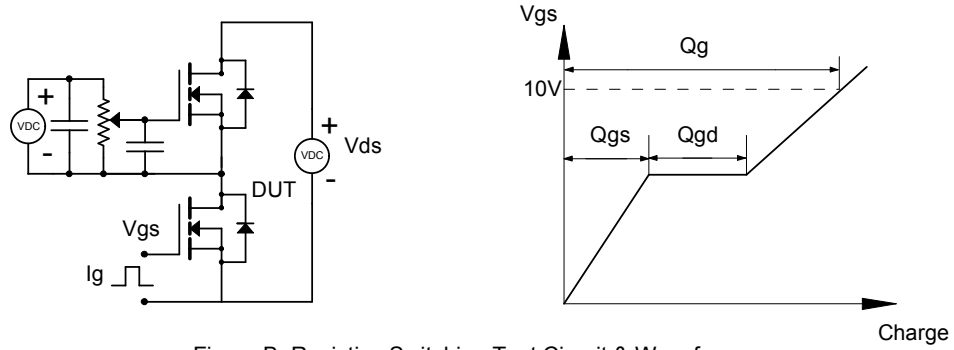


Figure B: Resistive Switching Test Circuit & Waveforms

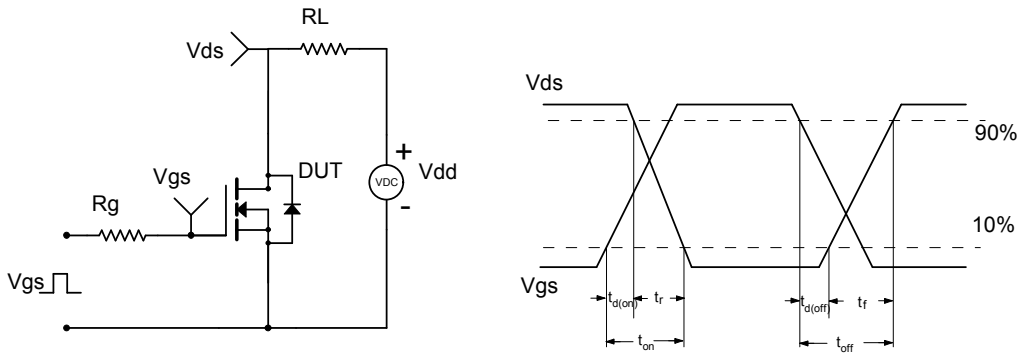


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

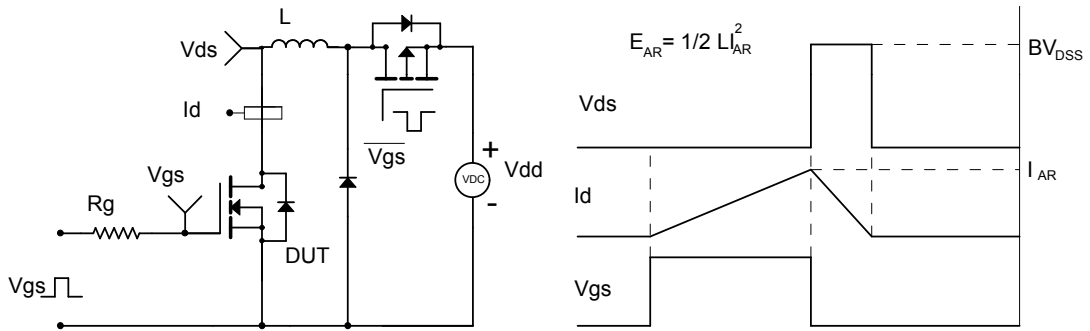


Figure D: Diode Recovery Test Circuit & Waveforms

