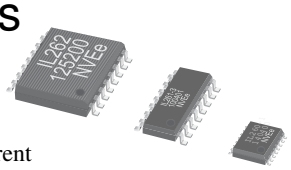
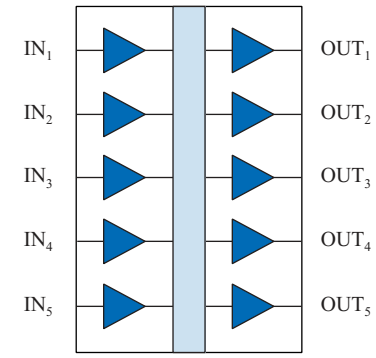
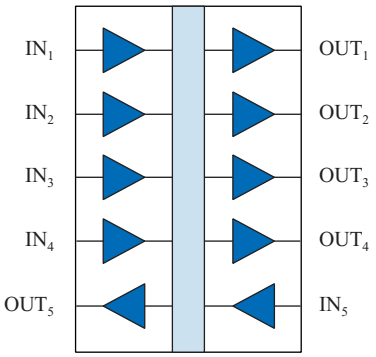
# High Speed Five-Channel Digital Isolators



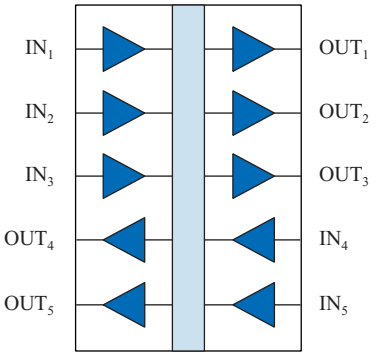
## Functional Diagrams




**IL260**




**IL261**




**IL262**

## Features

- High Speed: 110 Mbps
- 1.2 mA/channel typical quiescent current
- Very high isolation: 6 $kV_{RMS}$ Reinforced Isolation (VE-Series)
- 50 kV/µs typ.; 30 kV/µs min. common mode transient immunity
- No carrier or clock for low EMI emissions and susceptibility
- –40 to 85 °C operating temperature
- 44000-year barrier life
- Excellent magnetic immunity
- 2 ns typical pulse width distortion
- 100 ps pulse jitter
- 4 ns typical propagation delay skew
- 10 ns typical propagation delay
- 2 ns channel-to-channel skew
- IEC 60747-17 (VDE 0884-17):2021-10 certified; UL 1577 recognized
- 0.15" and True 8™ mm 16-pin SOIC; 16-pin QSOP packages

## Applications

- ADCs and DACs
- Multiplexed data transmission
- Board-to-board communication
- Peripheral interfaces
- Equipment covered under IEC 61010-1 Edition 3
- >5 $kV_{RMS}$ rated IEC 60601-1 medical applications

## Description

NVE's IL260-Series five-channel high-speed digital isolators are CMOS devices manufactured with NVE's patented* spintronic Giant Magnetoresistive (GMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

Performance is specified over the temperature range of –40 °C to +85 °C without derating. All transmit and receive channels operate at 110 Mbps over the full temperature and supply voltage range. The symmetric magnetic coupling barrier provides a typical propagation delay of only 10 ns and a pulse width distortion of 2 ns, achieving the best specifications of any isolator. The fifth channel can be is used to distribute isolated clocks or handshake signals to multiple delta-sigma A/D converters.

Parts are available in ultraminiature 16-pin QSOPs, as well as 0.15"and 0.3"-wide SOIC packages. V-Series versions offer extremely high isolation voltage of 6 $kV_{RMS}$, and true 8 mm creepage.

High channel density and low jitter, skew, and pulse-width distortion makes these devices ideal for isolating ADCs and DACs, parallel buses and peripheral interfaces.





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## Absolute Maximum Ratings(1)

| Parameters | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Storage Temperature | $T_S$ | −55 | | 150 | °C | |
| Junction Temperature | $T_J$ | −55 | | 150 | °C | |
| Supply Voltage | $V_{DD1}$,$V_{DD2}$ | −0.5 | | 7 | V | |
| Input Voltage | $V_I$ | −0.5 | | $V_{DD}$ + 0.5 | V | |
| Output Voltage | $V_O$ | −0.5 | | $V_{DD}$ + 0.5 | V | |
| Output Current Drive | $I_O$ | −10 | | 10 | mA | |
| Lead Solder Temperature | | | | 260 | °C | 10 sec. |
| ESD | | | 2 | | kV | HBM |

## Recommended Operating Conditions

| Parameters | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Ambient Operating Temperature | $T_A$ | −40 | | 85 | °C | |
| Junction Temperature | $T_J$ | −40 | | 100 | °C | |
| Supply Voltage | $V_{DD1}$,$V_{DD2}$ | 2.7 | | 5.5 | V | |
| Logic High Input Voltage | $V_{IH}$ | 2.4 | | $V_{DD}$ | V | |
| Logic Low Input Voltage | $V_{IL}$ | 0 | | 0.8 | V | |
| Input Signal Rise and Fall Times | $t_{IR}$, $t_{IF}$ | | | 1 | µs | |

## Safety and Approvals

***IEC 60747-17 (VDE 0884-17):2021-10:***

"VE" version (Reinforced Isolation; VDE File Number 5016933-4880-0002)

- Working Voltage ($V_{IORM}$): 1200 $V_{RMS}$ (1700 $V_{PK}$) with 20% Safety Factor; pollution degree 2
- Isolation voltage ($V_{ISO}$): 6000 $V_{RMS}$
- Surge immunity ($V_{IOSM}$): 12.8 $kV_{PK}$
- Surge rating: 8000 V
- Transient overvoltage ($V_{IOTM}$): 6000 $V_{PK}$
- Each part tested at 2387 $V_{PK}$ for 1 second, 5 pC partial discharge limit
- Samples tested at 6000 $V_{PK}$ for 60 sec.; then 2122 $V_{PK}$ for 10 sec. with 5 pC partial discharge limit

Standard versions (Basic Isolation; VDE File Number 5016933-4880-0001)

- Isolation voltage ($V_{ISO}$): 2500 $V_{RMS}$
- Transient overvoltage ($V_{IOTM}$): 4000 $V_{PK}$
- Surge rating: 4000 V
- Each part tested at 1590 $V_{PK}$ for 1 second, 5 pC partial discharge limit.
- Samples tested at 4000 $V_{PK}$ for 60 sec.; then 1358 $V_{PK}$ for 10 sec. with 5 pC partial discharge limit.

- Working Voltage ($V_{IORM}$; pollution degree 2):

| Package | Part No. Suffix | Working Voltage |
|---|---|---|
| QSOP16 | -1 | 600 $V_{RMS}$ |
| Narrow-body SOIC16 | -3 | 700 $V_{RMS}$ |
| Wide-body SOIC16/True 8™ | None | 600 $V_{RMS}$ |

| Safety-Limiting Values | Symbol | Value | Units |
|---|---|---|---|
| Safety rating ambient temperature | $T_S$ | 180 | °C |
| Safety rating power (180 °C) | $P_S$ | 270 | mW |
| Supply current safety rating (total of supplies) | $I_S$ | 54 | mA |

***UL 1577*** (Component Recognition Program File Number E207481)

V-Series isolation grade

6 kV rating; tested at 7.2 $kV_{RMS}$ (10.2 $kV_{PK}$) for 1 second; each lot sample tested at 6 $kV_{RMS}$ (8485 $V_{PK}$) for 1 minute.

Standard isolation grade

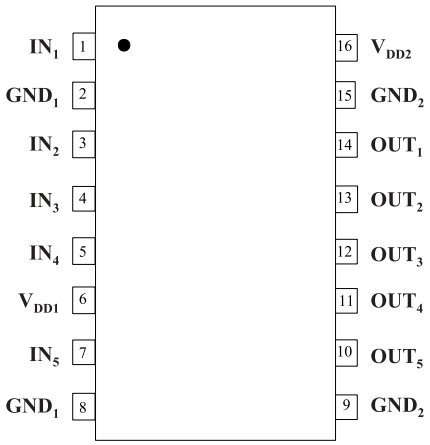
Each part tested at 3000 $V_{RMS}$ (4243 $V_{PK}$) for 1 second; each lot sample tested at 2500 $V_{RMS}$ (3536 $V_{PK}$) for 1 minute.

## Soldering Profile

Per JEDEC J-STD-020C, MSL 1

### IL260 Pin Connections

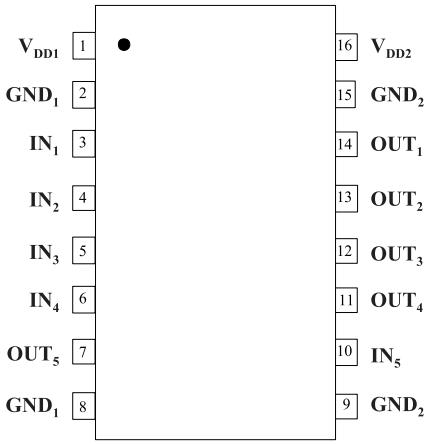
| | | |
|---|---|---|
| 1 | $IN_1$ | Input 1 |
| 2 | $GND_1$ | Ground* |
| 3 | $IN_2$ | Input 2 |
| 4 | $IN_3$ | Input 3 |
| 5 | $IN_4$ | Input 4 |
| 6 | $V_{DD1}$ | Supply Voltage 1 |
| 7 | $IN_5$ | Input 5 |
| 8 | $GND_1$ | Ground* |
| 9 | $GND_2$ | Ground* |
| 10 | $OUT_5$ | Output 5 |
| 11 | $OUT_4$ | Output 4 |
| 12 | $OUT_3$ | Output 3 |
| 13 | $OUT_2$ | Output 2 |
| 14 | $OUT_1$ | Output 1 |
| 15 | $GND_2$ | Ground* |
| 16 | $V_{DD2}$ | Supply Voltage 2 |




IL260

### IL261 Pin Connections

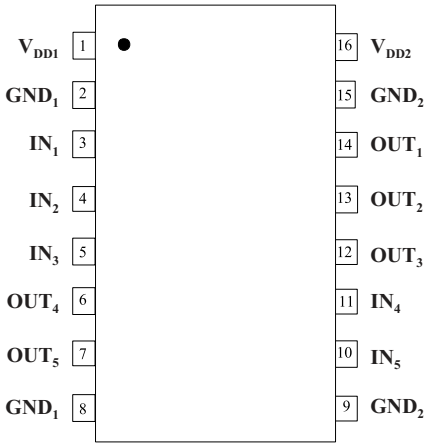
| | | |
|---|---|---|
| 1 | $V_{DD1}$ | Supply Voltage 1 |
| 2 | $GND_1$ | Ground* |
| 3 | $IN_1$ | Input 1 |
| 4 | $IN_2$ | Input 2 |
| 5 | $IN_3$ | Input 3 |
| 6 | $IN_4$ | Input 4 |
| 7 | $OUT_5$ | Output 5 |
| 8 | $GND_1$ | Ground* |
| 9 | $GND_2$ | Ground* |
| 10 | $IN_5$ | Input 5 |
| 11 | $OUT_4$ | Output 4 |
| 12 | $OUT_3$ | Output 3 |
| 13 | $OUT_2$ | Output 2 |
| 14 | $OUT_1$ | Output 1 |
| 15 | $GND_2$ | Ground* |
| 16 | $V_{DD2}$ | Supply Voltage 2 |




IL261

### IL262 Pin Connections

| | | |
|---|---|---|
| 1 | $V_{DD1}$ | Supply Voltage 1 |
| 2 | $GND_1$ | Ground* |
| 3 | $IN_1$ | Input 1 |
| 4 | $IN_2$ | Input 2 |
| 5 | $IN_3$ | Input 3 |
| 6 | $OUT_4$ | Output 4 |
| 7 | $OUT_5$ | Output 5 |
| 8 | $GND_1$ | Ground* |
| 9 | $GND_2$ | Ground* |
| 10 | $IN_5$ | Input 5 |
| 11 | $IN_4$ | Input 4 |
| 12 | $OUT_3$ | Output 3 |
| 13 | $OUT_2$ | Output 2 |
| 14 | $OUT_1$ | Output 1 |
| 15 | $GND_2$ | Ground* |
| 16 | $V_{DD2}$ | Supply Voltage 2 |




IL262

***NOTE:** Pins 2 and 8 are internally connected, as are pins 9 and 15.

| **3.3 Volt Electrical Specifications** ($T_{min}$ to $T_{max}$) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameters** | | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Test Conditions** |
| Input Quiescent Current | IL260 | $I_{DD1}$ | | 300 | 400 | µA | |
| | IL261 | | | 1.2 | 1.75 | mA | |
| | IL262 | | | 2.4 | 3.5 | mA | |
| Output Quiescent Current | IL260 | $I_{DD2}$ | | 6 | 8.75 | mA | |
| | IL261 | | | 4.8 | 7 | mA | |
| | IL262 | | | 3.6 | 5.25 | mA | |
| Logic Input Current | | $I_i$ | −10 | | 10 | µA | |
| Logic High Output Voltage | | $V_{OH}$ | $V_{DD}$−0.1 | $V_{DD}$ | | V | $I_O$ = −20 µA, $V_I$=$V_{IH}$ |
| | | | 0.8 x $V_{DD}$ | 0.9 x $V_{DD}$ | | | $I_O$ = −4 mA, $V_I$=$V_{IH}$ |
| Logic Low Output Voltage | | $V_{OL}$ | | 0 | 0.1 | V | $I_O$ = 20 µA, $V_I$=$V_{IL}$ |
| | | | | 0.5 | 0.8 | | $I_O$ = 4 mA, $V_I$=$V_{IL}$ |

| **Switching Specifications** (2.7 V <$V_{DD}$ < 3.6 V) | | | | | | |
|---|---|---|---|---|---|---|
| Maximum Data Rate | | 100 | 110 | | Mbps | $C_L$ = 15 pF |
| Minimum Pulse Width[7] | PW | 10 | | | ns | 50% Points, $V_O$ |
| Propagation Delay Input to Output (High to Low) | $t_{PHL}$ | | 12 | 18 | ns | $C_L$ = 15 pF |
| Propagation Delay Input to Output (Low to High) | $t_{PLH}$ | | 12 | 18 | ns | $C_L$ = 15 pF |
| Pulse Width Distortion $\lvert t_{PHL}-t_{PLH}\rvert$[2] | PWD | | 2 | 3 | ns | $C_L$ = 15 pF |
| Propagation Delay Skew[3] | $t_{PSK}$ | | 4 | 6 | ns | $C_L$ = 15 pF |
| Output Rise Time (10%–90%) | $t_R$ | | 2 | 4 | ns | $C_L$ = 15 pF |
| Output Fall Time (10%–90%) | $t_F$ | | 2 | 4 | ns | $C_L$ = 15 pF |
| Common Mode Transient Immunity (Output Logic High to Logic Low)[4] | $\lvert CM_H\rvert$,$\lvert CM_L\rvert$ | 30 | 50 | | kV/µs | $V_{CM}$ = 1500 $V_{DC}$<br>$t_{TRANSIENT}$ = 25 ns |
| Channel-to-Channel Skew | | | 2 | 3 | ns | $C_L$ = 15 pF |
| Dynamic Power Consumption[6] | | | 140 | 240 | µA/Mbps | per channel |

| **Magnetic Field Immunity**[8] ($V_{DD2}$ = 3 V, 3 V < $V_{DD1}$ < 5.5 V) | | | | | | |
|---|---|---|---|---|---|---|
| Power Frequency Magnetic Immunity | $H_{PF}$ | | 1500 | | A/m | 50Hz/60Hz |
| Pulse Magnetic Field Immunity | $H_{PM}$ | | 2000 | | A/m | $t_p$ = 8µs |
| Damped Oscillatory Magnetic Field | $H_{OSC}$ | | 2000 | | A/m | 0.1Hz – 1MHz |
| Cross-axis Immunity Multiplier[9] | $K_X$ | | 2.5 | | | |

| **5 Volt Electrical Specifications** ($T_{min}$ to $T_{max}$) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameters** | | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Test Conditions** |
| Input Quiescent Current | IL260 | $I_{DD1}$ | | 350 | 500 | µA | |
| | IL261 | | | 1.8 | 2.5 | mA | |
| | IL262 | | | 3.6 | 5 | mA | |
| Output Quiescent Current | IL260 | $I_{DD2}$ | | 9 | 12.5 | mA | |
| | IL261 | | | 7.2 | 10 | mA | |
| | IL262 | | | 5.4 | 7.5 | mA | |
| Logic Input Current | | $I_i$ | −10 | | 10 | µA | |
| Logic High Output Voltage | | $V_{OH}$ | $V_{DD}$−0.1 | $V_{DD}$ | | V | $I_O$ = −20 µA, $V_I$ = $V_{IH}$ |
| | | | 0.8 x $V_{DD}$ | 0.9 x $V_{DD}$ | | | $I_O$ = −4 mA, $V_I$ = $V_{IH}$ |
| Logic Low Output Voltage | | $V_{OL}$ | | 0 | 0.1 | V | $I_O$ = 20 µA, $V_I$ = $V_{IL}$ |
| | | | | 0.5 | 0.8 | | $I_O$ = 4 mA, $V_I$ = $V_{IL}$ |

| **Switching Specifications** ($V_{DD}$ = 5 V) | | | | | | |
|---|---|---|---|---|---|---|
| Maximum Data Rate | | 100 | 110 | | Mbps | $C_L$ = 15 pF |
| Minimum Pulse Width[7] | PW | 10 | | | ns | 50% Points, $V_O$ |
| Propagation Delay Input to Output (High to Low) | $t_{PHL}$ | | 10 | 15 | ns | $C_L$ = 15 pF |
| Propagation Delay Input to Output (Low to High) | $t_{PLH}$ | | 10 | 15 | ns | $C_L$ = 15 pF |
| Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$[2] | PWD | | 2 | 3 | ns | $C_L$ = 15 pF |
| Pulse Jitter[10] | $t_J$ | | 100 | | ps | $C_L$ = 15 pF |
| Propagation Delay Skew[3] | $t_{PSK}$ | | 4 | 6 | ns | $C_L$ = 15 pF |
| Output Rise Time (10%–90%) | $t_R$ | | 1 | 3 | ns | $C_L$ = 15 pF |
| Output Fall Time (10%–90%) | $t_F$ | | 1 | 3 | ns | $C_L$ = 15 pF |
| Common Mode Transient Immunity (Output Logic High to Logic Low)[4] | $\lvert CM_H \rvert$,$\lvert CM_L \rvert$ | 30 | 50 | | kV/µs | $V_{CM}$ = 1500 $V_{DC}$<br>$t_{TRANSIENT}$ = 25 ns |
| Channel-to-Channel Skew | | | 2 | 3 | ns | $C_L$ = 15 pF |
| Dynamic Power Consumption[6] | | | 200 | 340 | µA/Mbps | per channel |

| **Magnetic Field Immunity**[8] ($V_{DD2}$ = 5 V, 3 V < $V_{DD1}$ < 5.5V) | | | | | | |
|---|---|---|---|---|---|---|
| Power Frequency Magnetic Immunity | $H_{PF}$ | | 3500 | | A/m | 50Hz/60Hz |
| Pulse Magnetic Field Immunity | $H_{PM}$ | | 4500 | | A/m | $t_p$ = 8µs |
| Damped Oscillatory Magnetic Field | $H_{OSC}$ | | 4500 | | A/m | 0.1Hz – 1MHz |
| Cross-axis Immunity Multiplier[9] | $K_X$ | | 2.5 | | | |

| Insulation Specifications | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Test Conditions** |
| | | | | | | | |
| Creepage Distance (external) | QSOP<br>0.15" SOIC<br>0.3" SOIC | | 4.03<br>4.03<br>8.03 | <br><br>8.3 | | mm | Per IEC 60601 |
| Total Barrier Thickness (internal) | | | 0.012 | 0.016 | | mm | |
| Leakage Current[5] | | | | 0.2 | | $\mu A_{RMS}$ | 240 $V_{RMS}$ |
| Barrier Resistance[5] | | $R_{IO}$ | | $>10^{14}$ | | Ω | 500 V |
| Barrier Capacitance[5] | | $C_{IO}$ | | 5 | | pF | f = 1 MHz |
| Comparative Tracking Index | | CTI | ≥600 | | | $V_{RMS}$ | Per IEC 60112 |
| High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life) | AC<br>DC | $V_{IO}$ | 1000<br>1500 | | | $V_{RMS}$<br>$V_{DC}$ | At maximum operating temperature |
| Surge Immunity ("V" Versions) | | $V_{IOSM}$ | 12.8 | | | $kV_{PK}$ | Per IEC 61000-4-5 |
| Barrier Life | | | | 44000 | | Years | 100°C, 1000 $V_{RMS}$, 60% CL activation energy |

| Thermal Characteristics | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Test Conditions** |
| Junction–Ambient Thermal Resistance | QSOP<br>0.15" SOIC16<br>0.3" SOIC16 | $\theta_{JA}$ | | 100<br>82<br>67 | | °C/W | Double-sided PCB in free air |
| Junction–Case (Top) Thermal Resistance | QSOP<br>0.15" SOIC16<br>0.3" SOIC16 | $\theta_{JC}$ | | 9<br>8<br>12 | | | |
| Junction–Ambient Thermal Resistance | 0.3" SOIC | $\theta_{JA}$ | | 46 | | | 2s2p PCB in free air per JESD51 |
| Junction–Case (Top) Thermal Resistance | | $\theta_{JC}$ | | 9 | | | |
| Power Dissipation | QSOP<br>0.15" SOIC16<br>0.3" SOIC16 | $P_D$ | | | 675<br>675<br>1500 | mW | |

## Notes:

1. Absolute maximum means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD is equal to PWD divided by pulse width.
3. $t_{PSK}$ is the magnitude of the worst-case difference in $t_{PHL}$ and/or $t_{PLH}$ between devices at 25°C.
4. $CM_H$ is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. $CM_L$ is the maximum common mode input voltage that can be sustained while maintaining $V_O < 0.8$ V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
5. Device is considered a two-terminal device: pins 1–8 shorted and pins 9–16 shorted.
6. Dynamic power consumption numbers are calculated per channel and are supplied by the channel's input side power supply.
7. Minimum pulse width is the minimum value at which specified PWD is guaranteed.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 8.
9. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see diagram on p. 8).
10. 66,535-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800 ps transition time.

## Application Information

### Electrostatic Discharge Sensitivity

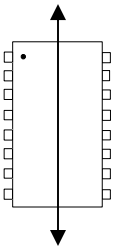
This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

### Electromagnetic Compatibility

IsoLoop Isolators have the lowest EMC footprint of any isolation technology. There are no internal clocks or carriers. IsoLoop Isolators' Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards.

These isolators are fully compliant with IEC 61000-6-1 and IEC 61000-6-2 standards for immunity, and IEC 61000-6-3, IEC 61000-6-4, CISPR, and FCC Class A standards for emissions.

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than to "pin-to-pin" as shown in the diagram below:



Cross-axis Field Direction

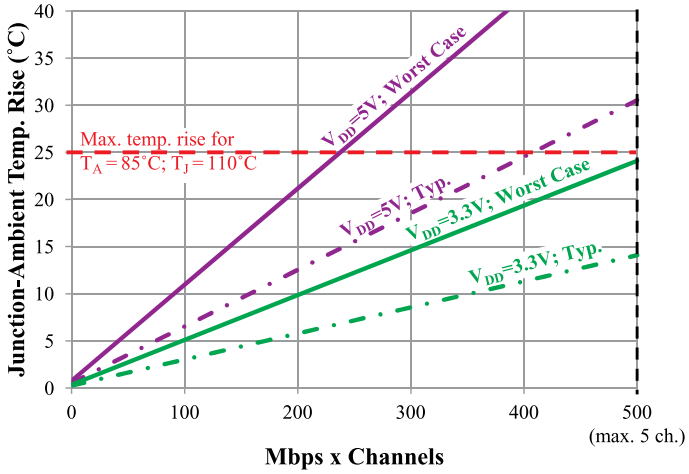
### Dynamic Power Consumption

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

### Thermal Management

IsoLoop Isolators are designed for low power dissipation and thermal performance, providing unmatched channel density for high-performance isolators. Nevertheless, package temperature rise should be considered when running multiple channels at high speed. Power consumption is higher at 5 volt operation than at 3.3 volts, and dynamic supply current is higher on the input side of the isolators than the output side, so thermal management is more important with five-volt input-side power supplies.

IL260/IL261/IL262 parts have a maximum junction temperature of 110°C. Based on the specifications contained in this datasheet, the derating curve at typical operating conditions is as follows:




### Power Supply Decoupling

Both power supplies should be bypassed with 0.1 µF typical (0.047 µF minimum) capacitors as close as possible to the $V_{DD}$ pins. Ground planes for both $GND_1$ and $GND_2$ are highly recommended for data rates above 10 Mbps.

### Maintaining Creepage

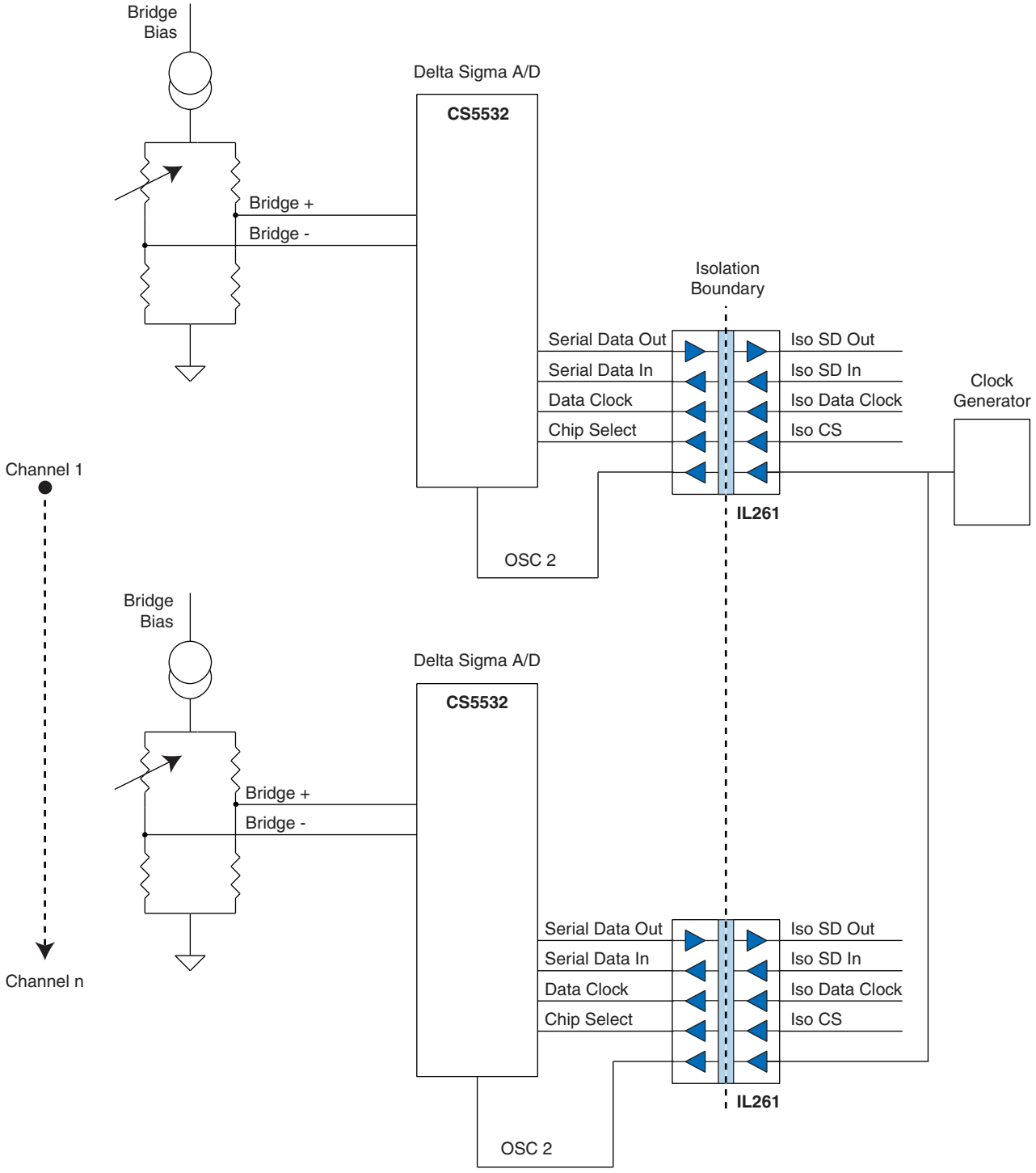
Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

### Signal Status on Start-up and Shut Down

To minimize power dissipation, input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider including an initialization signal in the start-up circuit. Initialization consists of toggling the input either high then low, or low then high.

## Application Diagram—Multi-Channel Delta-Sigma A/D Converter

In a typical single-channel delta-sigma ADC, the system clock is located on the isolated side of the system and only four channels of isolation are required. With multiple ADCs configured in a channel-to-channel isolation configuration, however, clock jitter and edge placement accuracy of the system clock must be matched between ADCs. The best solution is to use a single clock on the system side and distribute the clock to each ADC. The five-channel IL261 is ideal, with the fifth channel used to distribute a single, isolated clock to multiple ADCs as shown below:



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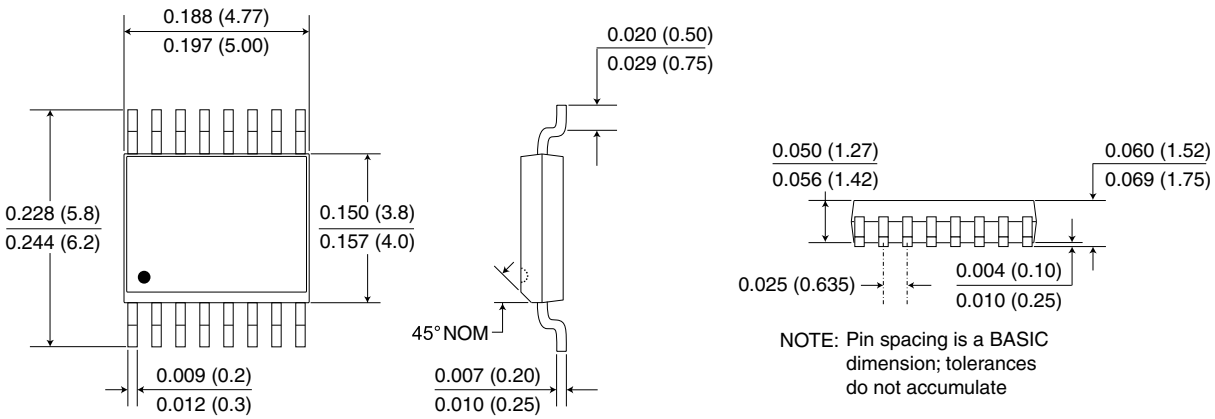
## Package Drawings

### **Ultraminiature 16-pin QSOP Package** (-1 suffix)

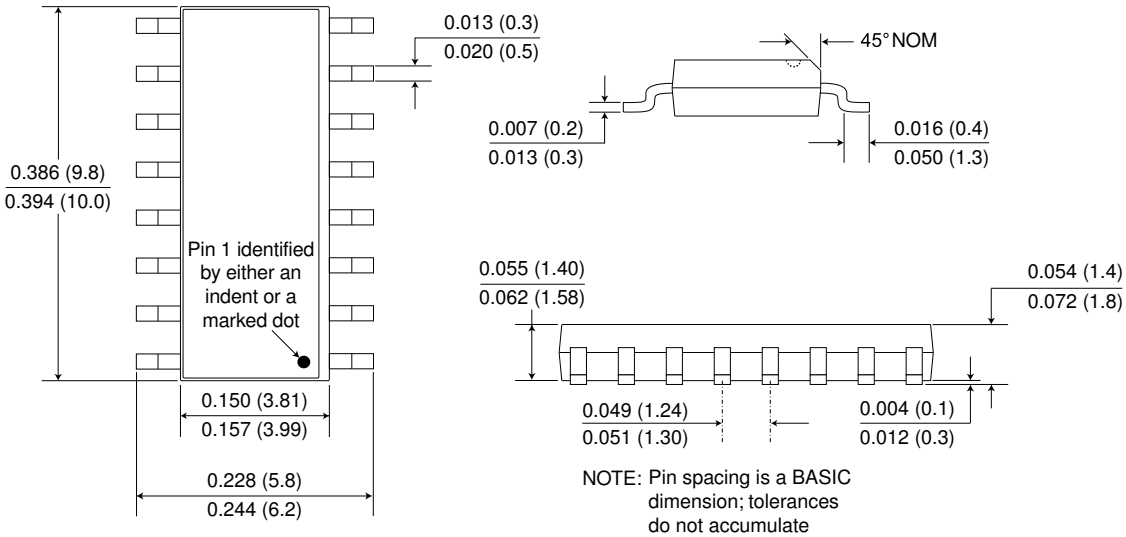
Dimensions in inches (mm); scale = approx. 5X




NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

### **0.15" 16-pin SOIC Package** (-3 suffix)

Dimensions in inches (mm); scale = approx. 5X




NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate



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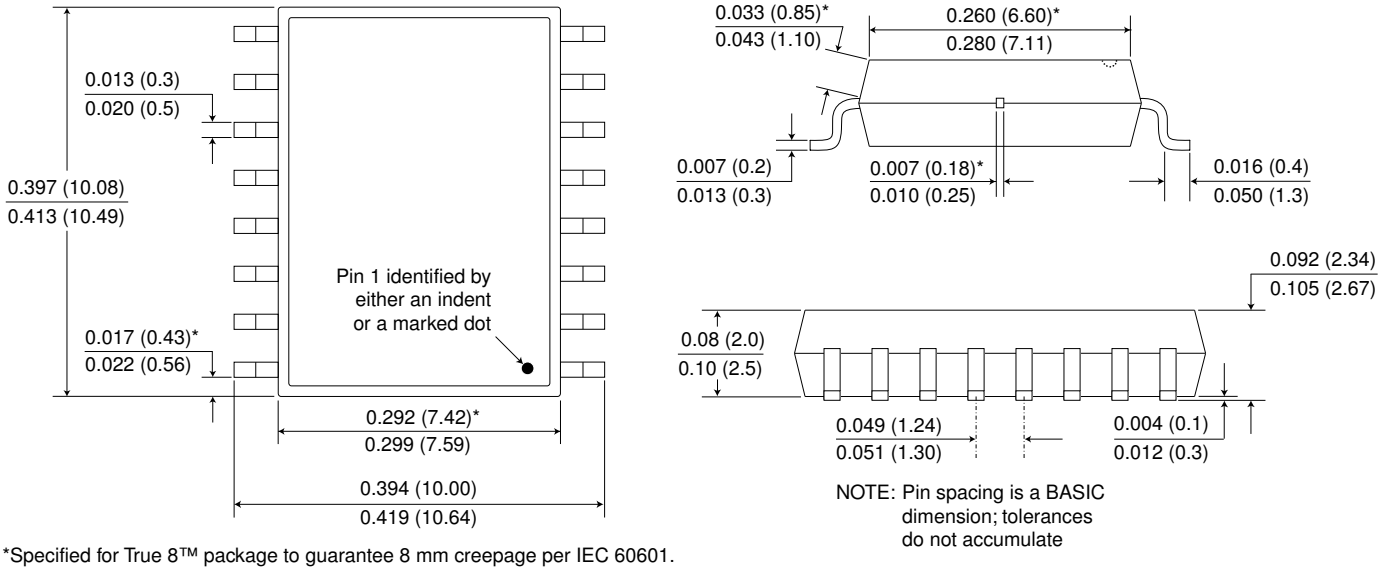
## **0.3" 16-pin SOIC Package** (no suffix)

Dimensions in inches (mm); scale = approx. 5X




NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.



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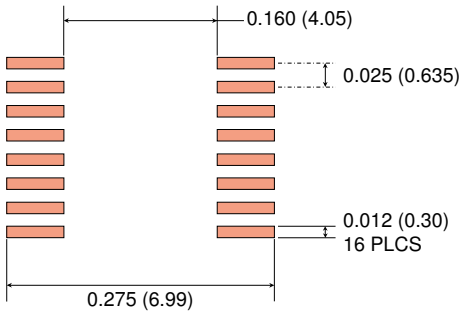
## Recommended Pad Layouts

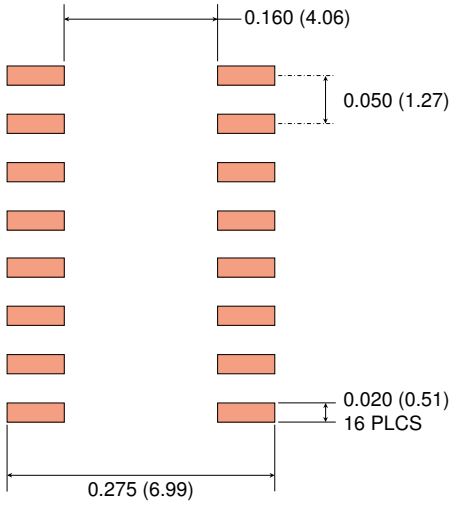
### 4 mm x 5 mm 16-pin QSOP Pad Layout

Dimensions in inches (mm); scale = approx. 5X




### 0.15" 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



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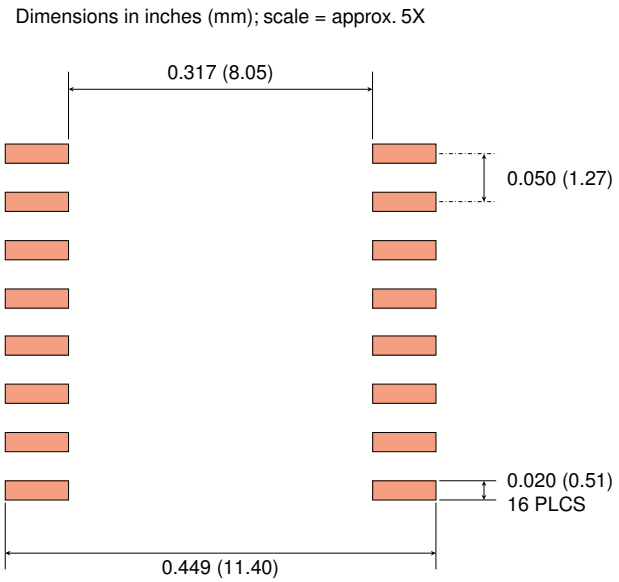
## 0.3" 16-pin SOIC Pad Layout



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## Available Parts

| Available Parts | Transmit Channels | Receive Channels | Isolation Voltage (RMS) | Package |
|---|---|---|---|---|
| IL260-1E | 5 | 0 | 2.5 kV | QSOP |
| IL260-3E | 5 | 0 | 2.5 kV | Narrow SOIC |
| IL260E | 5 | 0 | 2.5 kV | Wide SOIC |
| IL260VE | 5 | 0 | 6 kV | Wide SOIC |
| IL261-1E | 4 | 1 | 2.5 kV | QSOP |
| IL261-3E | 4 | 1 | 2.5 kV | Narrow SOIC |
| IL261E | 4 | 1 | 2.5 kV | Wide SOIC |
| IL261VE | 4 | 1 | 6 kV | Wide SOIC |
| IL262-3E | 3 | 2 | 2.5 kV | Narrow SOIC |
| IL262E | 3 | 2 | 2.5 kV | Wide SOIC |
| IL262VE | 3 | 2 | 6 kV | Wide SOIC |

All part types are available on tape and reel.

## Part Numbering

IL 260 - 3 E TR13

**Bulk Package**
Blank = Tube
TR7 = 7" Tape and Reel
TR13 = 13" Tape and Reel

**Package**
Blank = 80/20 Tin/Lead Plating
E = RoHS Compliant

**Package Type**
Blank = 0.3" 16-pin SOIC
-3 = 0.15" 16-pin SOIC

**Base Part Number**
260 = 5 Drive Channels
261 = 4 Drive Channels, 1 Receive Channel
262 = 3 Drive Channels, 2 Receive Channel

**Product Family**
IL = Isolators

RoHS COMPLIANT



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## Revision History

**ISB-DS-001-IL260/1/2-Y**
**February 2023**

**Changes**
- Increased minimum supply voltage from 2.5 V to 2.7 V (p. 2).
- Eliminated redundant “valid part numbers” list (p. 14).

**ISB-DS-001-IL260/1/2-X**

**Changes**
- Upgraded to IEC 60747-17 (VDE 0884-17):2021-10 (p. 3).
- Increased Working Voltage ratings based on latest VDE testing (p. 3).

**ISB-DS-001-IL260/1/2-W**

**Changes**
- Reduced minimum supply voltage to 2.5 V (p. 2).
- Updated EMC standards.
- Deleted minimum magnetic field immunity specifications (not 100% tested).
- Updated thermal specifications (p. 7).

**ISB-DS-001-IL260/1/2-V**

**Change**
- VDE certification and UL approval for V-Series versions (6 kV reinforced isolation).

**ISB-DS-001-IL260/1/2-U**

**Changes**
- Updated VDE certification standard to VDE V 0884-10.
- Upgraded “VE” Version Surge Immunity specification to 12.8 kV.
- Upgraded “VE” Version VDE 0884-10 rating to reinforced insulation.
- Corrected QSOP pin width dimension (p. 10).

**ISB-DS-001-IL260/1/2-T**

**Changes**
- Increased V-Series isolation voltage to 6 kVrms.
- Increased typ. Total Barrier Thickness specification to 0.016 mm.
- Increased CTI min. specification to ≥600 $V_{RMS}$.

**ISB-DS-001-IL260/1/2-S**

**Changes**
- Added V-Series 5 kV isolation voltage versions.
- More detailed “Available Parts” table.

**ISB-DS-001-IL260/1/2-R**

**Changes**
- Added QSOP packages (-1 suffix).
- Revised and added details to thermal characteristic specifications (p. 2).
- Added VDE 0884 Safety-Limiting Values (p. 3).
- Added “Thermal Management” paragraph in Applications section.



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ISB-DS-001-IL260/1/2-Y

*February 2023*