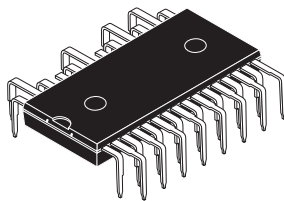
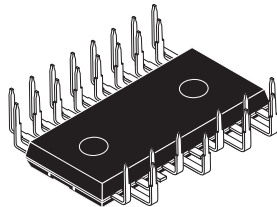


## SLLIMM-nano IPM, 3-phase inverter, 1 A, 3.6 Ω max., 500 V MOSFET



NDIP-26L

### Features

- IPM 1 A, 500 V,  $R_{DS(on)} = 3.6 \Omega$ , 3-phase MOSFET inverter bridge including control ICs for gate driving
- Optimized for low electromagnetic interference
- 3.3 V, 5 V, 15 V CMOS/TTL input comparators with hysteresis and pull-down/pull-up resistors
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- Shutdown function
- Comparator for fault protection against overtemperature and overcurrent
- Op-amp for advanced current sensing
- Optimized pinout for easy board layout
- Up to  $\pm 2$  kV ESD protection (HBM C = 100 pF, R = 1.5 kΩ)

### Applications

- 3-phase inverters for motor drives
- Dish washers
- Roller shutters
- Air-conditioning fans
- Draining and recirculation pumps



#### Product status link

[STIPN1M50-H](#)

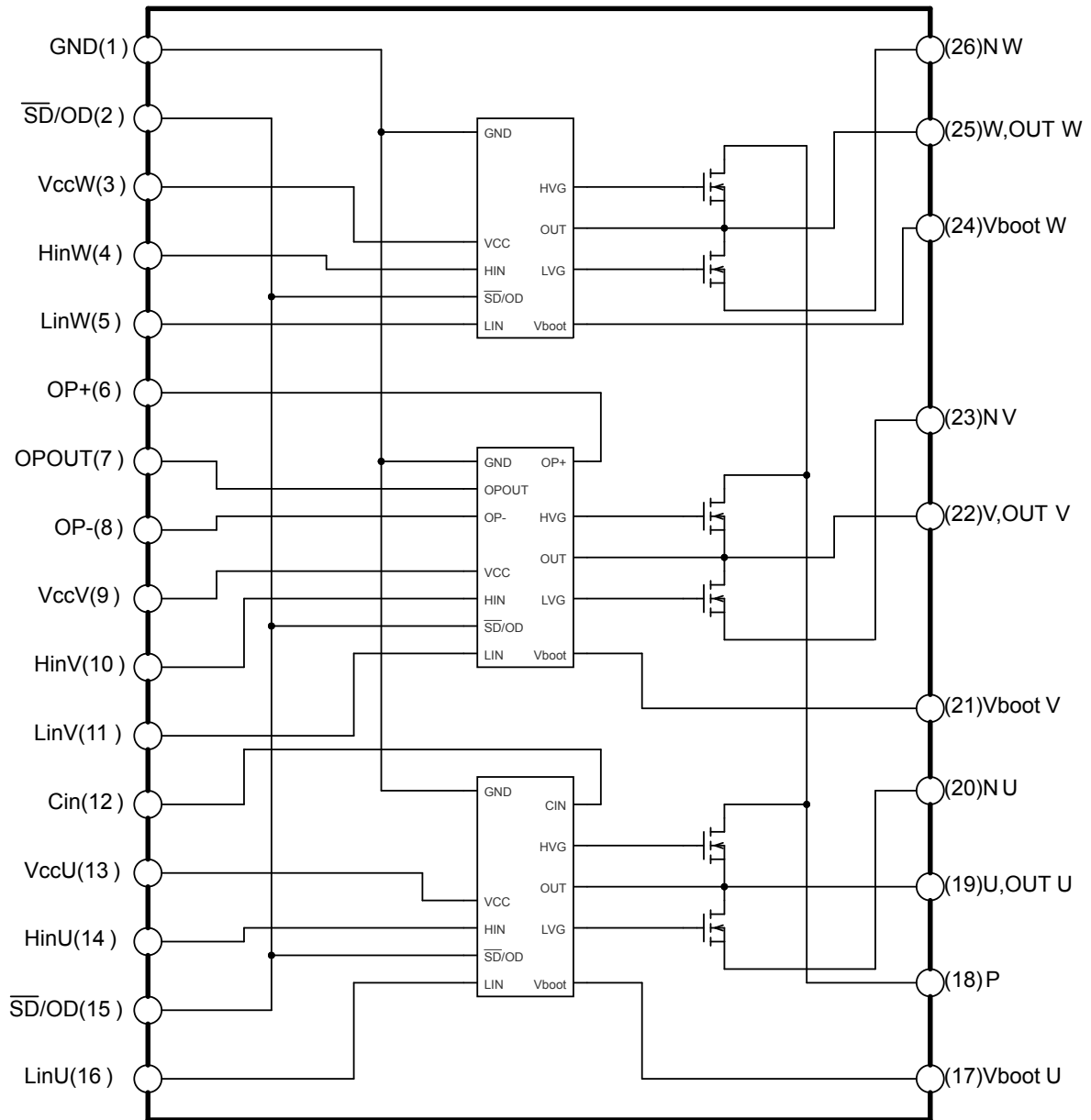
#### Product summary

<b>Order code</b>	STIPN1M50-H
<b>Marking</b>	IPN1M50-H
<b>Package</b>	NDIP-26L
<b>Packing</b>	Tube

### Description

This SLLIMM (small low-loss intelligent molded module) nano provides a compact, high-performance AC motor drive in a simple, rugged design. It is composed of six MOSFETs and three half-bridge HVICs for gate driving, providing low electromagnetic interference (EMI) characteristics with optimized switching speed. The package is optimized for thermal performance and compactness in built-in motor applications, or other low power applications where assembly space is limited. This IPM includes an operational amplifier, completely uncommitted, and a comparator that can be used to design a fast and efficient protection circuit. SLLIMM is a trademark of STMicroelectronics.

# 1 Internal schematic diagram and pin configuration

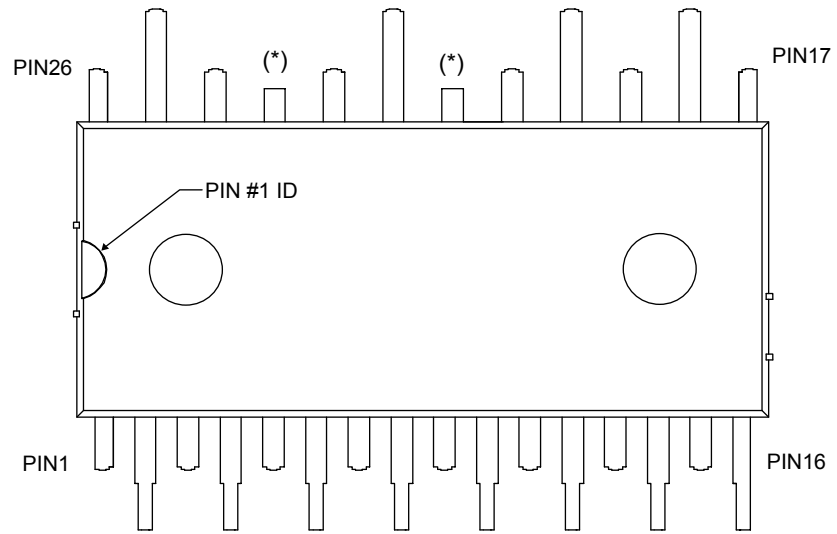
**Figure 1. Internal schematic diagram**


ADG171120161035SA

**Table 1. Pin description**

Pin	Symbol	Description
1	GND	Ground
2	$\overline{\text{SD}}/\text{OD}$	Shutdown logic input (active low) / open-drain (comparator output)
3	$V_{\text{CC W}}$	Low voltage power supply W phase
4	HIN W	High-side logic input for W phase
5	LIN W	Low-side logic input for W phase
6	OP+	Op-amp non inverting input
7	OP <sub>OUT</sub>	Op-amp output
8	OP-	Op-amp inverting input
9	$V_{\text{CC V}}$	Low voltage power supply V phase
10	HIN V	High-side logic input for V phase
11	LIN V	Low-side logic input for V phase
12	CIN	Comparator input
13	$V_{\text{CC U}}$	Low voltage power supply for U phase
14	HIN U	High-side logic input for U phase
15	$\overline{\text{SD}}/\text{OD}$	Shutdown logic input (active low) / open-drain (comparator output)
16	LIN U	Low-side logic input for U phase
17	$V_{\text{BOOT U}}$	Bootstrap voltage for U phase
18	P	Positive DC input
19	U, OUT <sub>U</sub>	U phase output
20	N <sub>U</sub>	Negative DC input for U phase
21	$V_{\text{BOOT V}}$	Bootstrap voltage for V phase
22	V, OUT <sub>V</sub>	V phase output
23	N <sub>V</sub>	Negative DC input for V phase
24	$V_{\text{BOOT W}}$	Bootstrap voltage for W phase
25	W, OUT <sub>W</sub>	W phase output
26	N <sub>W</sub>	Negative DC input for W phase

Figure 2. Pin layout (top view)



(\* Dummy pin internally connected to P (positive DC input).

AM09368V1

## 2 Electrical ratings

### 2.1 Absolute maximum ratings

**Table 2. Inverter part**

Symbol	Parameter	Value	Unit
$V_{DSS}$	MOSFET blocking voltage (or drain-source voltage) for each MOSFET ( $V_{IN}^{(1)} = 0\text{ V}$ )	500	V
$\pm I_D$	Continuous drain current each MOSFET ( $T_C = 25\text{ °C}$ )	1	A
$\pm I_{DP}^{(2)}$	Peak drain current each MOSFET (less than 1 ms)	2	A
$P_{TOT}$	Total power dissipation for each MOSFET ( $T_C = 25\text{ °C}$ )	10.8	W

1. Applied between  $HIN_i$ ,  $LIN_i$  and GND for  $i = U, V, W$ .
2. Pulse width limited by max. junction temperature.

**Table 3. Control part**

Symbol	Parameter	Min.	Max.	Unit
$V_{OUT}$	Output voltage applied between $OUT_U$ , $OUT_V$ , $OUT_W$ - GND	$V_{boot} - 21$	$V_{boot} + 0.3$	V
$V_{CC}$	Low voltage power supply	-0.3	21	V
$V_{CIN}$	Comparator input voltage	-0.3	$V_{CC} + 0.3$	V
$V_{op+}$	Op-amp non-inverting input	-0.3	$V_{CC} + 0.3$	V
$V_{op-}$	Op-amp inverting input	-0.3	$V_{CC} + 0.3$	V
$V_{boot}$	Bootstrap voltage	-0.3	620	V
$V_{IN}$	Logic input voltage applied between $HIN$ , $LIN$ and GND	-0.3	15	V
$V_{T\overline{SD/OD}}$	Open-drain voltage	-0.3	15	V
$dV_{out}/dt$	Allowed output slew rate		50	V/ns

**Table 4. Total system**

Symbol	Parameter	Value	Unit
$V_{ISO}$	Isolation withstand voltage applied between each pin and heat sink plate (AC voltage, $t = 60\text{ s}$ )	1000	Vrms
$T_J$	Power chip operating junction temperature range	-40 to 150	°C
$T_C$	Module case operation temperature range	-40 to 125	°C

## 2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Thermal resistance junction-case single MOSFET	11.5	°C/W
$R_{th(j-a)}$	Thermal resistance junction-ambient (per module)	22	°C/W

### 3 Electrical characteristics

$T_J = 25\text{ °C}$  unless otherwise specified.

#### 3.1 Inverter part

**Table 6. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{DSS}$	Zero-gate voltage drain current	$V_{DS} = 500\text{ V}$ , $V_{CC} = 15\text{ V}$ ; $V_{Boot} = 15\text{ V}$			1	mA
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{CC} = V_{boot} = 15\text{ V}$ , $V_{IN}^{(1)} = 0\text{ V}$ , $I_D = 1\text{ mA}$	500			V
$R_{DS(on)}$	Static drain source turn-on resistance	$V_{CC} = V_{boot} = 15\text{ V}$ , $V_{IN}^{(1)} = 0\text{ to }5\text{ V}$ , $I_D = 0.5\text{ A}$		3.2	3.6	$\Omega$
$V_{SD}$	Drain-source diode forward voltage	$V_{IN}^{(1)} = 0$ "logic state", $I_D = 1\text{ A}$		0.9	1.6	V

1. Applied between  $HINx$ ,  $LINx$  and  $GND$  for  $x=U,V,W$ .

**Table 7. Inductive load switching time and energy**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{on}^{(1)}$	Turn-on time	$V_{DD} = 300\text{ V}$ , $V_{CC} = V_{boot} = 15\text{ V}$ , $V_{IN}^{(2)} = 0\text{ to }5\text{ V}$ , $I_C = 0.5\text{ A}$ (see Figure 4. Switching time definition)	-	226	-	ns
$t_{c(on)}^{(1)}$	Crossover time (on)		-	130	-	
$t_{off}^{(1)}$	Turn-off time		-	248	-	
$t_{c(off)}^{(1)}$	Crossover time (off)		-	56	-	
$t_{rr}$	Reverse recovery time		-	155	-	
$E_{on}$	Turn-on switching energy		-	25	-	$\mu\text{J}$
$E_{off}$	Turn-off switching energy	-	3.8	-		

1.  $t_{ON}$  and  $t_{OFF}$  include the propagation delay time of the internal drive.  $t_{C(ON)}$  and  $t_{C(OFF)}$  are the switching time of MOSFET itself under the internally given gate driving conditions.

2. Applied between  $HINx$ ,  $LINx$  and  $GND$  for  $x=U,V,W$ .

Figure 3. Switching time test circuit

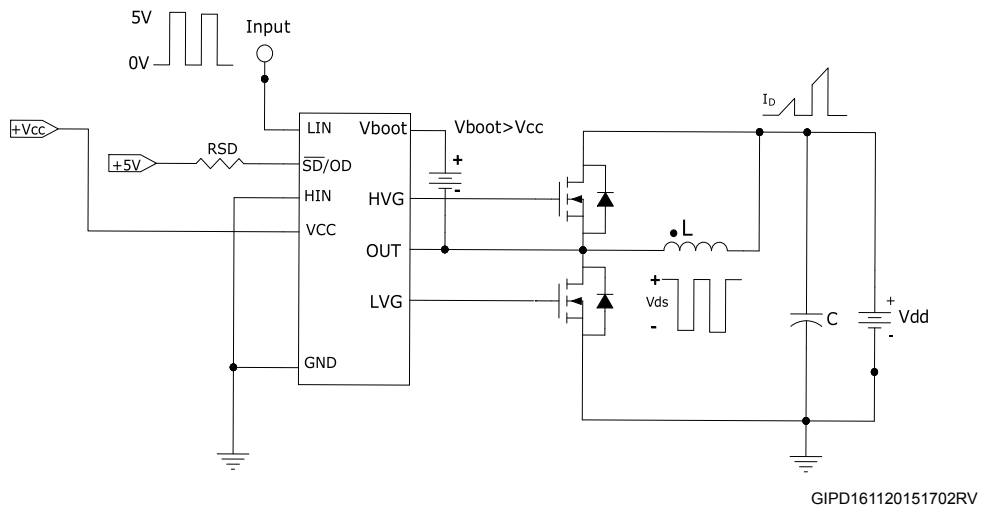
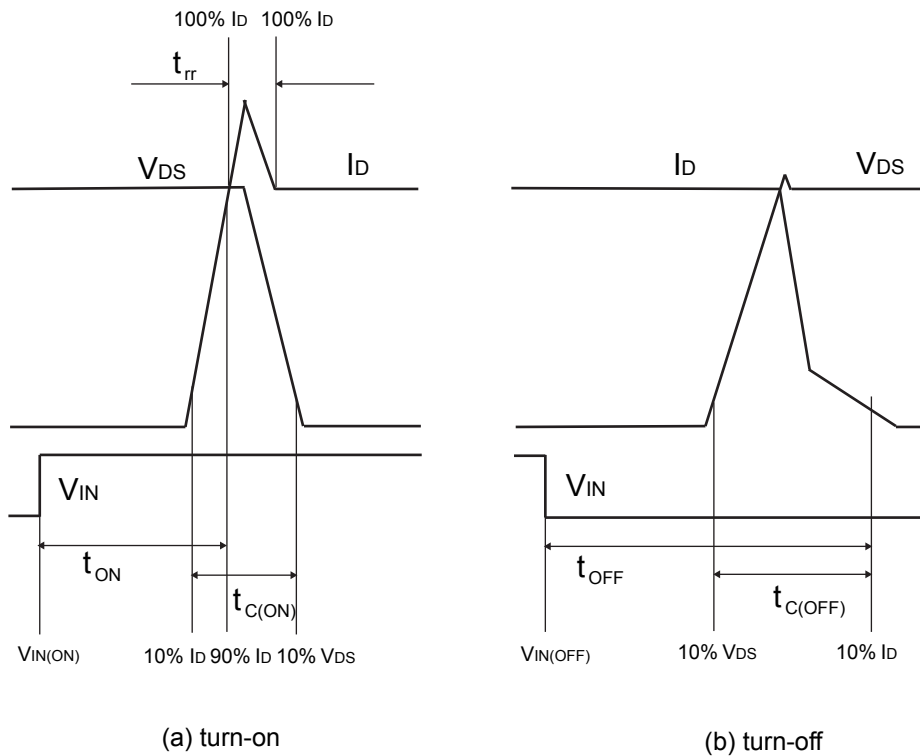


Figure 4. Switching time definition



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Figure 4. Switching time definition refers to HIN, LIN inputs (active high).



### 3.2 Control part

**Table 8. Low voltage power supply ( $V_{CC} = 15\text{ V}$  unless otherwise specified)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC\_hys}$	$V_{CC}$ UV hysteresis		1.2	1.5	1.8	V
$V_{CC\_thON}$	$V_{CC}$ UV turn ON threshold		11.5	12	12.5	V
$V_{CC\_thOFF}$	$V_{CC}$ UV turn OFF threshold		10	10.5	11	V
$I_{qccu}$	Undervoltage quiescent supply current	$V_{CC} = 15\text{ V}$ , $\overline{SD}/OD = 5\text{ V}$ ; LIN = 0 V; HIN = 0 V, CIN = 0 V			150	$\mu\text{A}$
$I_{qcc}$	Quiescent current	$V_{CC} = 15\text{ V}$ , $\overline{SD}/OD = 5\text{ V}$ ; LIN = 0 V; HIN = 0 V, CIN = 0 V			1	mA
$V_{ref}$	Internal comparator (CIN) reference voltage		0.5	0.54	0.58	V

**Table 9. Bootstrapped voltage ( $V_{CC} = 15\text{ V}$  unless otherwise specified)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BS\_hys}$	$V_{BS}$ UV hysteresis		1.2	1.5	1.8	V
$V_{BS\_thON}$	$V_{BS}$ UV turn-ON threshold		11.1	11.5	12.1	V
$V_{BS\_thOFF}$	$V_{BS}$ UV turn-OFF threshold		9.8	10	10.6	V
$I_{QBSU}$	Undervoltage $V_{BS}$ quiescent current	$V_{BS} < 9\text{ V}$ , $\overline{SD}/OD = 5\text{ V}$ ; LIN = 0 V and HIN = 5 V; CIN = 0 V		70	110	$\mu\text{A}$
$I_{QBS}$	$V_{BS}$ quiescent current	$V_{BS} = 15\text{ V}$ , $\overline{SD}/OD = 5\text{ V}$ ; LIN = 0 V and HIN = 5 V; CIN = 0 V		200	300	$\mu\text{A}$
$R_{DS(on)}$	Bootstrap driver on- resistance	LVG ON		120		$\Omega$

**Table 10. Logic inputs ( $V_{CC} = 15\text{ V}$  unless otherwise specified)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{il}$	Low logic level voltage				0.8	V
$V_{ih}$	High logic level voltage		2.25			V
$I_{HINh}$	HIN logic "1" input bias current	HIN = 15 V	20	40	100	$\mu\text{A}$
$I_{HINl}$	HIN logic "0" input bias current	HIN = 0 V			1	$\mu\text{A}$
$I_{LINh}$	LIN logic "1" input bias current	LIN = 15 V	20	40	100	$\mu\text{A}$
$I_{LINl}$	LIN logic "0" input bias current	LIN = 0 V			1	$\mu\text{A}$
$I_{SDh}$	$\overline{SD}$ logic "0" input bias current	$\overline{SD} = 15\text{ V}$	30	120	300	$\mu\text{A}$
$I_{SDl}$	$\overline{SD}$ logic "1" input bias current	$\overline{SD} = 0\text{ V}$			3	$\mu\text{A}$
Dt	Dead time	(see Figure 5. Dead time and interlocking waveform definitions)		180		ns

**Table 11. Op-amp characteristics ( $V_{CC} = 15\text{ V}$  unless otherwise specified)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{io}$	Input offset voltage	$V_{ic} = 0\text{ V}$ , $V_o = 7.5\text{ V}$			6	mV
$I_{io}$	Input offset current	$V_{ic} = 0\text{ V}$ , $V_o = 7.5\text{ V}$		4	40	nA
$I_{ib}$	Input bias current <sup>(1)</sup>			100	200	nA
$V_{OL}$	Low level output voltage	$R_L = 10\text{ k}\Omega$ to $V_{CC}$		75	150	mV
$V_{OH}$	High level output voltage	$R_L = 10\text{ k}\Omega$ to GND	14	14.7		V
$I_o$	Output short-circuit current	Source, $V_{id} = +1\text{ V}$ ; $V_o = 0\text{ V}$	16	30		mA
		Sink, $V_{id} = -1\text{ V}$ ; $V_o = V_{CC}$	50	80		mA
SR	Slew rate	$V_i = 1 - 4\text{ V}$ ; $C_L = 100\text{ pF}$ ; unity gain	2.5	3.8		V/ $\mu\text{s}$
GBWP	Gain bandwidth product	$V_o = 7.5\text{ V}$	8	12		MHz
$A_{vd}$	Large signal voltage gain	$R_L = 2\text{ k}\Omega$	70	85		dB
SVR	Supply voltage rejection ratio	vs. $V_{CC}$	60	75		dB
CMRR	Common mode rejection ratio		55	70		dB

1. The direction of input current is out of the IC.

**Table 12. Sense comparator characteristics ( $V_{CC} = 15\text{ V}$  unless otherwise specified)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{ib}$	Input bias current	$V_{CIN} = 1\text{ V}$			1	$\mu\text{A}$
$V_{od}$	Open-drain low level output voltage	$I_{od} = 3\text{ mA}$			0.5	V
$R_{ON\_OD}$	Open-drain low level output resistance	$I_{od} = 3\text{ mA}$		166		$\Omega$
$R_{PD\_SD}$	$\overline{SD}$ pull-down resistor <sup>(1)</sup>			125		$\text{k}\Omega$
$t_{d\_comp}$	Comparator delay	$\overline{SD}/OD$ pulled to 5 V through 100 $\text{k}\Omega$ resistor		90	130	ns
SR	Slew rate	$C_L = 180\text{ pF}$ ; $R_{pu} = 5\text{ k}\Omega$		60		$\text{V}/\mu\text{s}$
$t_{sd}$	Shutdown to high / low-side driver propagation delay	$V_{OUT} = 0$ , $V_{boot} = V_{CC}$ , $V_{IN} = 0$ to 3.3 V	50	125	200	ns
$t_{isd}$	Comparator triggering to high / low-side driver turn-off propagation delay	Measured applying a voltage step from 0 V to 3.3 V to pin CIN	50	200	250	

1. Equivalent values as a result of the resistances of three drivers in parallel.

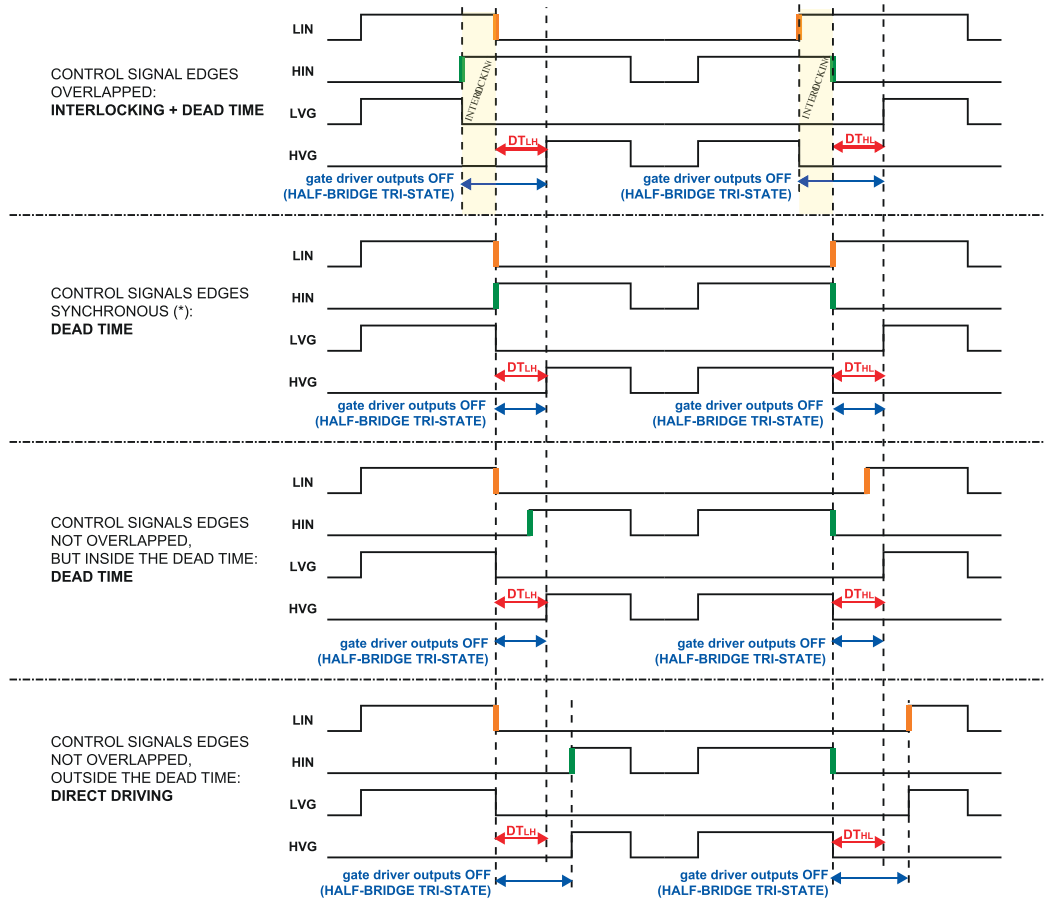
**Table 13. Truth table**

Condition	Logic input ( $V_i$ )			Output	
	$\overline{SD}/OD$	LIN	HIN	LVG	HVG
Shutdown enable half-bridge tri-state	L	X <sup>(1)</sup>	X <sup>(1)</sup>	L	L
Interlocking half-bridge tri-state	H	H	H	L	L
0 "logic state" half-bridge tri-state	H	L	L	L	L
1 "logic state" low-side direct driving	H	H	L	H	L
1 "logic state" high-side direct driving	H	L	H	L	H

1. X: don't care.

### 3.3 Waveform definitions

Figure 5. Dead time and interlocking waveform definitions



## 4 Shutdown function

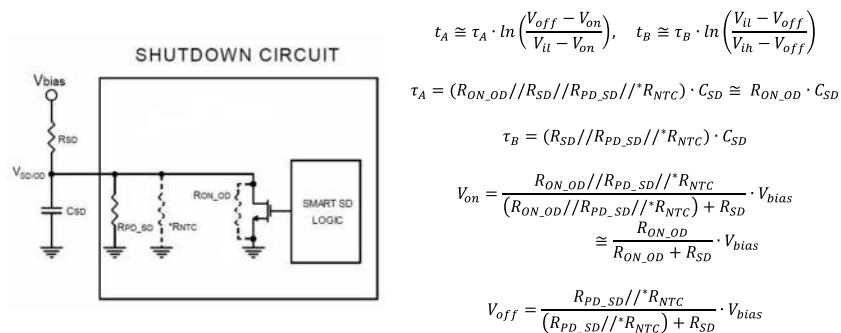
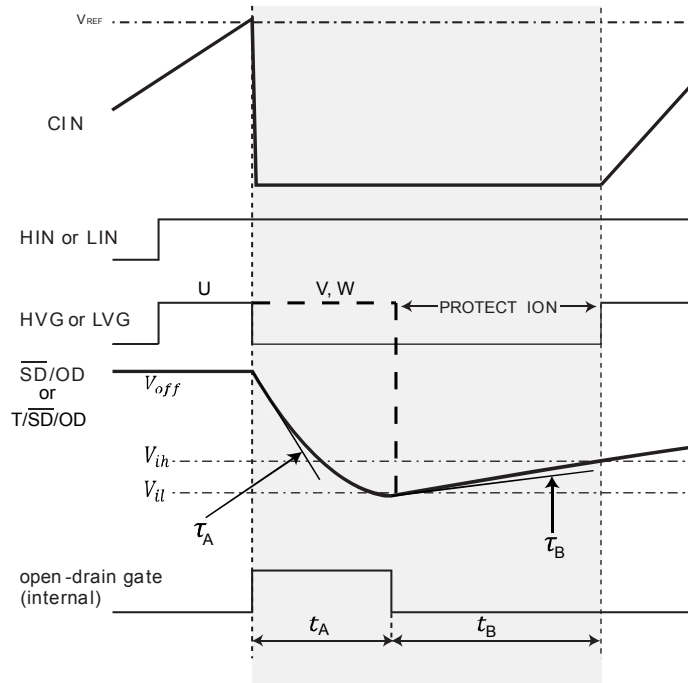
The device is equipped with three half-bridge IC gate drivers and integrates a comparator for fault detection. The comparator has an internal voltage reference  $V_{REF}$  connected to the inverting input, while the non-inverting input pin (CIN) can be connected to an external shunt resistor for current monitoring.

Since the comparator is embedded in the U IC gate driver, in case of fault it disables directly the U outputs, whereas the shutdown of V and W IC gate drivers depends on the RC value of the external SD circuitry, which fixes the disabling time.

For an effective design of the shutdown circuit, please refer to Application note AN4966.

**Figure 6. Shutdown timing waveforms**

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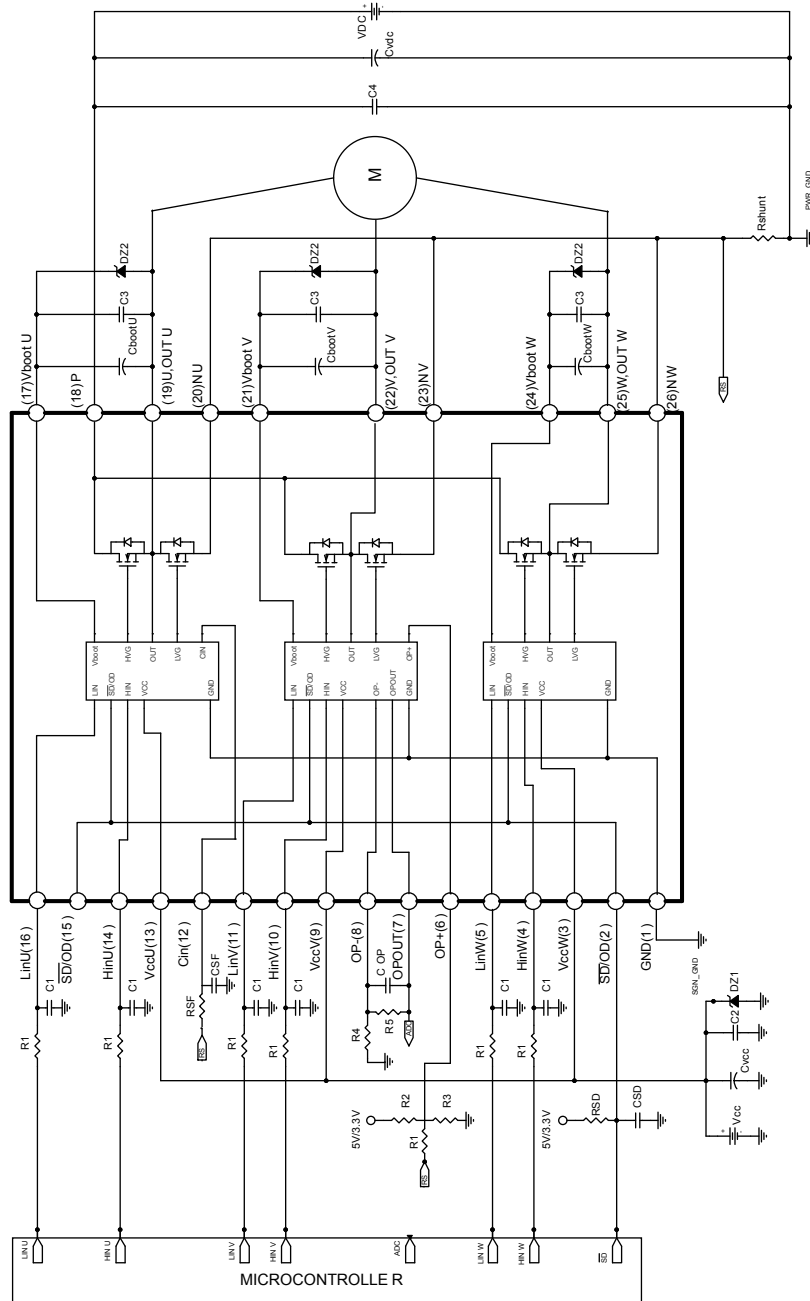
$R_{SD}$  and  $C_{SD}$  external circuitry must be designed to ensure  $V_{on} < V_{il}$  &  $V_{off} > V_{ih}$

Please refer to AN4966 for further details.

\*  $R_{NTC}$  to be considered only when the NTC is internally connected to the T/SD/OD pin.

## 5 Application circuit example

Figure 7. Application circuit example



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Application designers are free to use a different scheme according to the specifications of the device.

## 5.1 Guidelines

- Input signals HIN, LIN are active high logic. A 375 kΩ (typ.) pull-down resistor is built-in for each input. To avoid input signal oscillation, the wiring of each input should be as short as possible, and the use of RC filters ( $R_1$ ,  $C_1$ ) on each input signal is suggested. The filters should be with a time constant of about 100 ns and placed as close as possible to the IPM input pins.
- The use of a bypass capacitor  $C_{VCC}$  (aluminum or tantalum) can reduce the transient circuit demand on the power supply. Also, to reduce any high-frequency switching noise distributed on the power lines, a decoupling capacitor  $C_2$  (100 to 220 nF, with low ESR and low ESL) should be placed as close as possible to the  $V_{CC}$  pin and in parallel with the bypass capacitor.
- The use of an RC filter ( $R_{SF}$ ,  $C_{SF}$ ) is recommended to prevent protection circuit malfunction. The time constant ( $R_{SF} \times C_{SF}$ ) should be set to 1 μs and the filter must be placed as close as possible to the CIN pin.
- The  $\overline{SD}$  is an input/output pin (open-drain type if it is used as output). The capacitor  $C_{SD}$  of the filter on  $\overline{SD}$  should be fixed no higher than 3.3 nF in order to assure the  $\overline{SD}$  activation time  $\tau_A \leq 500$  ns. Besides, the filter should be placed as close as possible to the  $\overline{SD}$  pin.
- The decoupling capacitor  $C_3$  (from 100 to 220 nF, ceramic with low ESR and low ESL), in parallel with each  $C_{boot}$ , filters high-frequency disturbance. Both  $C_{boot}$  and  $C_3$  (if present) should be placed as close as possible to the U, V, W and  $V_{boot}$  pins. Bootstrap negative electrodes should be connected to U, V, W terminals directly and separated from the main output wires.
- To avoid overvoltage on the  $V_{CC}$  pin, a Zener diode (Dz1) can be used. Similarly on the  $V_{boot}$  pin, a Zener diode (Dz2) can be placed in parallel with each  $C_{boot}$ .
- The use of the decoupling capacitor  $C_4$  (100 to 220 nF, with low ESR and low ESL) in parallel with the electrolytic capacitor  $C_{Vdc}$  is useful to prevent surge destruction. Both capacitors  $C_4$  and  $C_{Vdc}$  should be placed as close as possible to the IPM ( $C_4$  has priority over  $C_{Vdc}$ ).
- By integrating an application-specific type HVIC inside the module, direct coupling to the MCU terminals without an opto-couplers is possible.
- Low-inductance shunt resistors have to be used for phase leg current sensing.
- In order to avoid malfunctions, the wiring on N pins, the shunt resistor and  $P_{WR\_GND}$  should be as short as possible.
- The connection of  $SGN\_GND$  to  $PWR\_GND$  on one point only (close to the shunt resistor terminal) can reduce the impact of power ground fluctuation.

These guidelines ensure the specifications of the device for application designs. For further details, please refer to the relevant application note.

**Table 14. Recommended operating conditions**

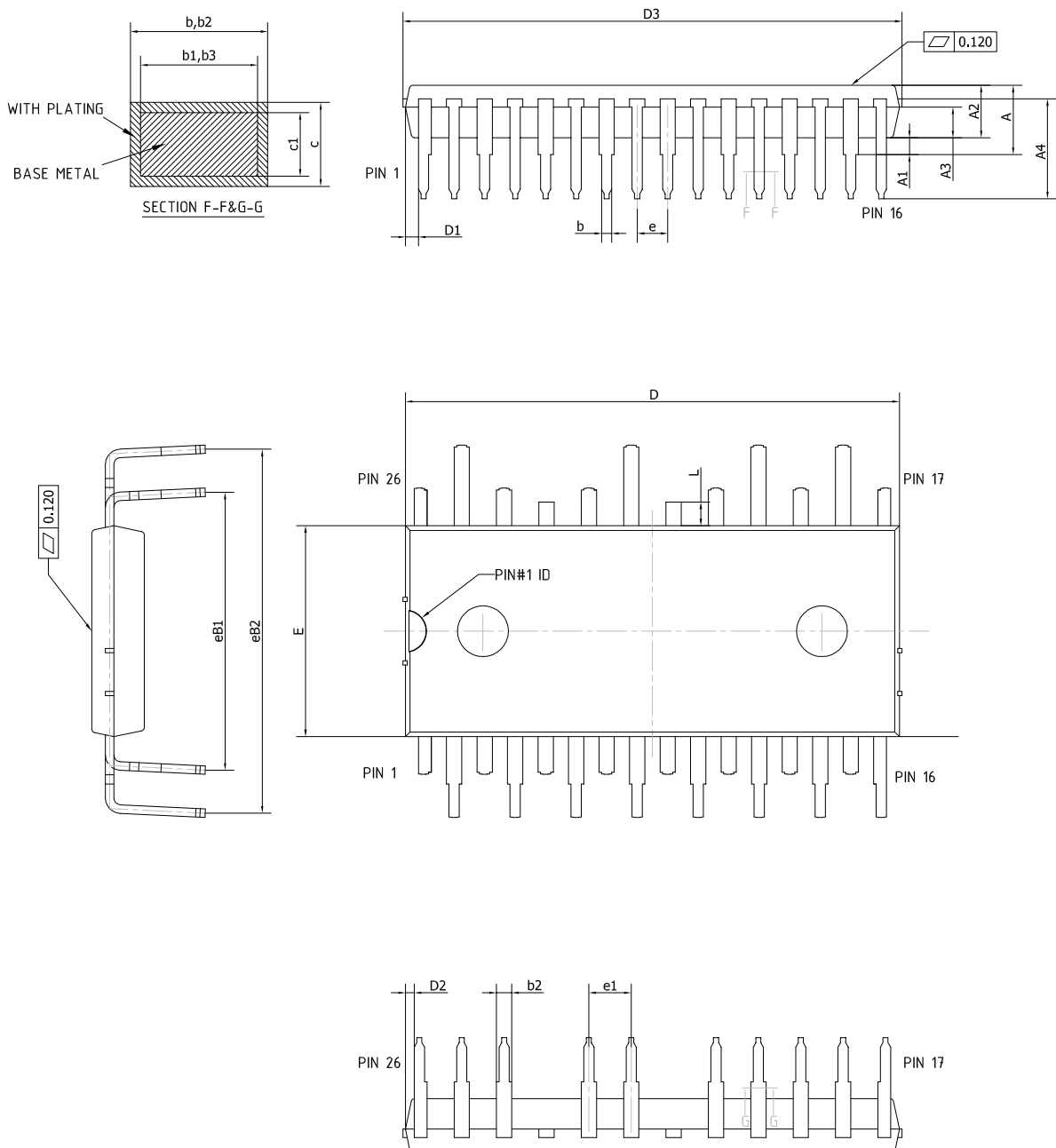
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{PN}$	Supply voltage	Applied between P-Nu, Nv, Nw		300	400	V
$V_{CC}$	Control supply voltage	Applied between $V_{CC}$ -GND	13.5	15	18	V
$V_{BS}$	High-side bias voltage	Applied between $V_{BOOTi}$ - $OUT_i$ for $i = U, V, W$	13		18	V
$t_{dead}$	Blanking time to prevent arm-short	For each input signal	1			μs
$f_{PWM}$	PWM input signal	$-40\text{ °C} < T_C < 100\text{ °C}$ $-40\text{ °C} < T_J < 125\text{ °C}$			25	kHz
$T_C$	Case operation temperature				100	°C

## 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 6.1 NDIP-26L type C package information

Figure 8. NDIP-26L type C package outline



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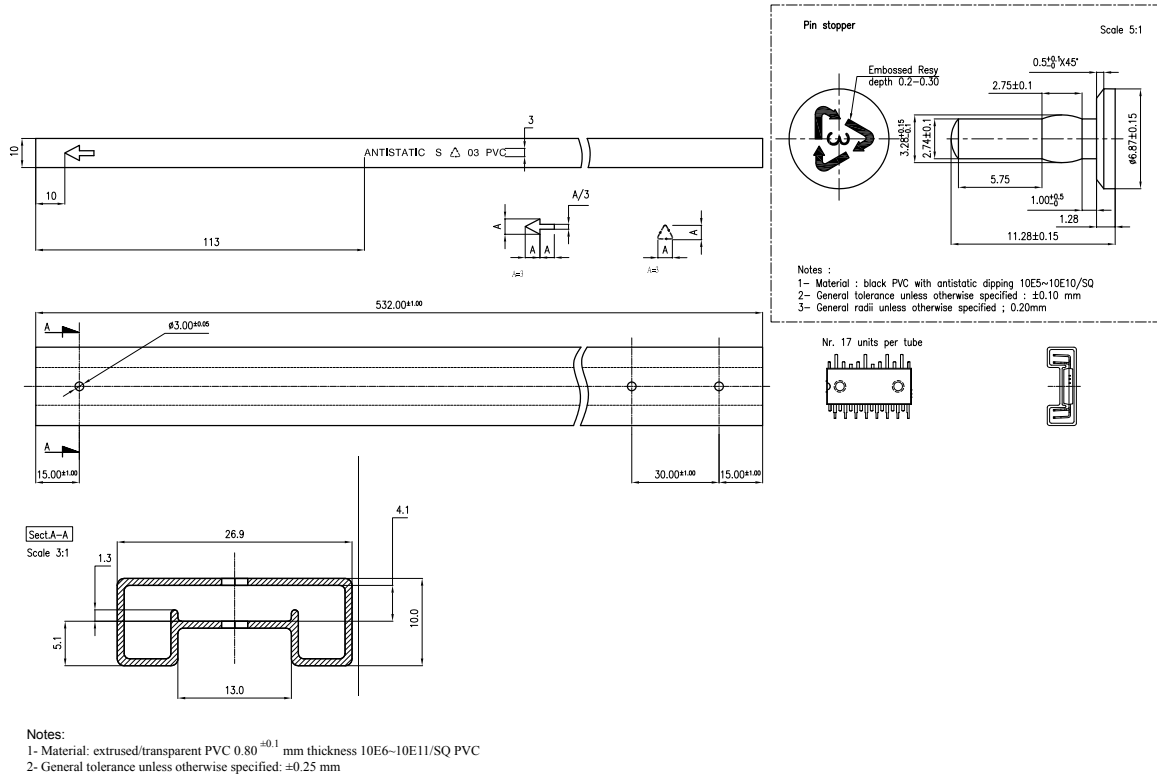


**Table 15. NDIP-26L type C mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			4.40
A1	0.80	1.00	1.20
A2	3.00	3.10	3.20
A3	1.70	1.80	1.90
A4	5.70	5.90	6.10
b	0.53		0.72
b1	0.52	0.60	0.68
b2	0.83		1.02
b3	0.82	0.90	0.98
c	0.46		0.59
c1	0.45	0.50	0.55
D	29.05	29.15	29.25
D1	0.50	0.77	1.00
D2	0.35	0.53	0.70
D3			29.55
E	12.35	12.45	12.55
e	1.70	1.80	1.90
e1	2.40	2.50	2.60
eB1	16.10	16.40	16.70
eB2	21.18	21.48	21.78
L	1.24	1.39	1.54

## 6.2 NDIP-26L packing information

Figure 9. NDIP-26L tube (dimensions are in mm)



8313150\_3

Table 16. Shipping details

Parameter	Value
Base quantity	17 pieces
Bulk quantity	476 pieces

## Revision history

**Table 17. Document revision history**

Date	Revision	Changes
18-Nov-2016	1	Initial release.
01-Feb-2017	2	Modified features and description on cover page. Modified <i>Table 15: "Recommended operating conditions"</i>
07-Jun-2017	3	Modified <i>Table 3: "Inverter part"</i> , <i>Table 6: "Thermal data"</i> and <i>Table 11: "Logic inputs (<math>V_{CC} = 15\text{ V}</math> unless otherwise specified)"</i> . Minor text changes.
28-Jan-2020	4	Modified title, features and applications in cover page. Updated <a href="#">Section 2 Electrical ratings</a> , <a href="#">Section 3 Electrical characteristics</a> , <a href="#">Section 4 Shutdown function</a> and <a href="#">Section 5.1 Guidelines</a> . Minor text changes.

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	<b>Revision history</b>	<b>19</b>

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