

N-Channel Power MOSFET

650V, 10A, 0.9Ω

FEATURES

- 100% UIS and R_g tested
- Advanced planar process
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

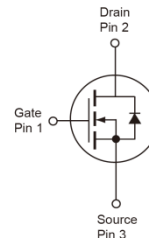
APPLICATIONS

- AC/DC LED Lighting
- Power Supply

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	650	V
$R_{DS(on)}$ (max)	0.9	Ω
Q_g	34	nC



ITO-220S



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	Limit	UNIT
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	±30	V
Continuous Drain Current (Note 1)	I_D	$T_C = 25^\circ\text{C}$	10
		$T_C = 100^\circ\text{C}$	6.3
Pulsed Drain Current (Note 2)	I_{DM}	30	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_{DTOT}	45	W
Single Pulse Avalanche Energy (Note 3)	E_{AS}	372	mJ
Single Pulse Avalanche Current (Note 3)	I_{AS}	6.1	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	Limit	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	2.8	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62	°C/W

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	650	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	2.5	3.4	4.5	V
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 650V, V_{GS} = 0V$	I_{DSS}	--	--	1	μA
Drain-Source On-State Resistance (Note 4)	$V_{GS} = 10V, I_D = 2A$	$R_{DS(on)}$	--	0.75	0.9	Ω
Forward Transconductance (Note 4)	$V_{DS} = 10V, I_D = 4A$	g_{fs}	--	6	--	S
Dynamic (Note 5)						
Total Gate Charge	$V_{DS} = 520V, I_D = 4A,$ $V_{GS} = 10V$	Q_g	--	34	--	nC
Gate-Source Charge		Q_{gs}	--	11	--	
Gate-Drain Charge		Q_{gd}	--	13	--	
Input Capacitance	$V_{DS} = 50V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	C_{iss}	--	1650	--	μF
Output Capacitance		C_{oss}	--	91	--	
Reverse Transfer Capacitance		C_{rss}	--	11	--	
Gate Resistance	$f = 1.0\text{MHz}, \text{open drain}$	R_g	0.6	2.1	4.2	Ω
Switching (Note 6)						
Turn-On Delay Time	$V_{DD} = 325V, R_G = 5\Omega,$ $I_D = 4A, V_{GS} = 10V$	$t_{d(on)}$	--	14	--	ns
Turn-On Rise Time		t_r	--	9	--	
Turn-Off Delay Time		$t_{d(off)}$	--	32	--	
Turn-Off Fall Time		t_f	--	15	--	
Source-Drain Diode						
Forward Voltage (Note 4)	$I_S = 4A, V_{GS} = 0V$	V_{SD}	--	--	1.4	V
Reverse Recovery Time	$I_S = 4A$	t_{rr}	--	307	--	ns
Reverse Recovery Charge		$di_F/dt = 100A/\mu s$	Q_{rr}	--	4.1	--

Notes:

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. $L = 20\text{mH}, I_{AS} = 6.1A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
4. Pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

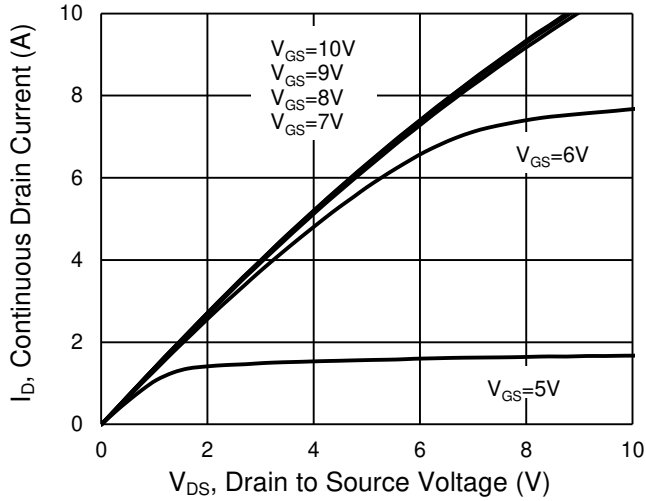
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM10NC65CF C0G	ITO-220S	50pcs / Tube

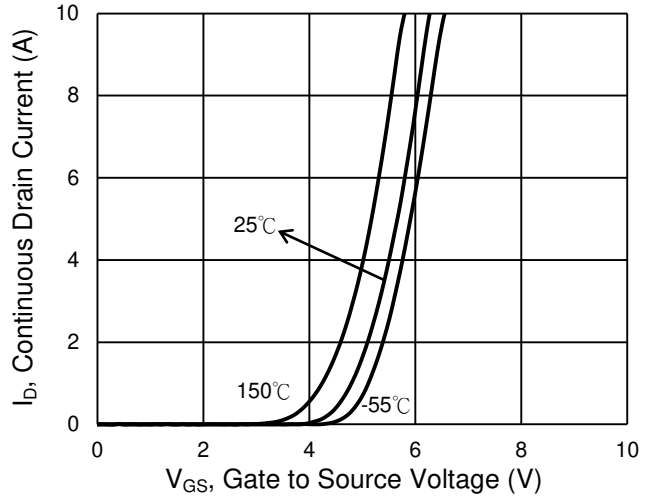
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

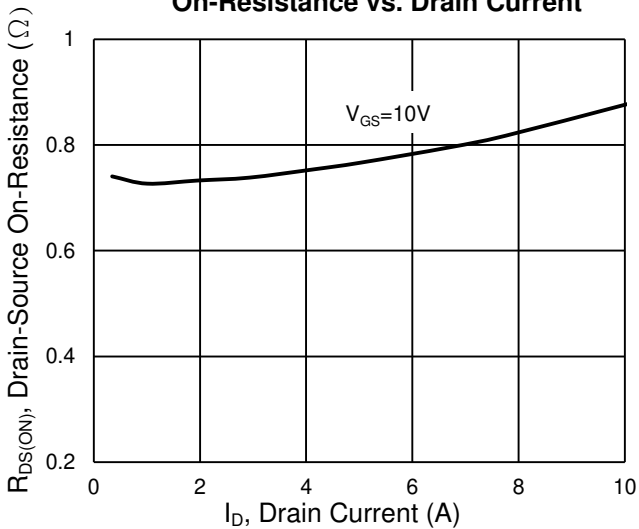
Output Characteristics



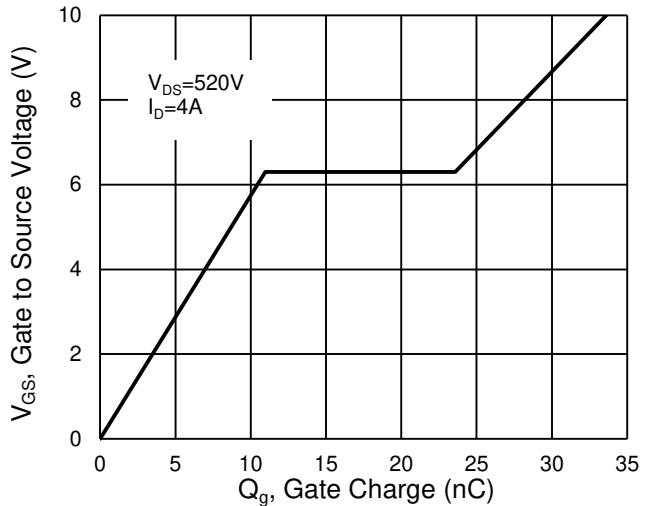
Transfer Characteristics



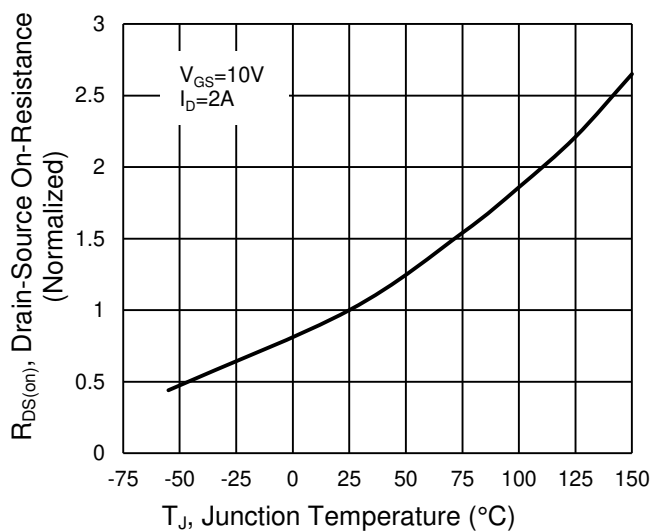
On-Resistance vs. Drain Current



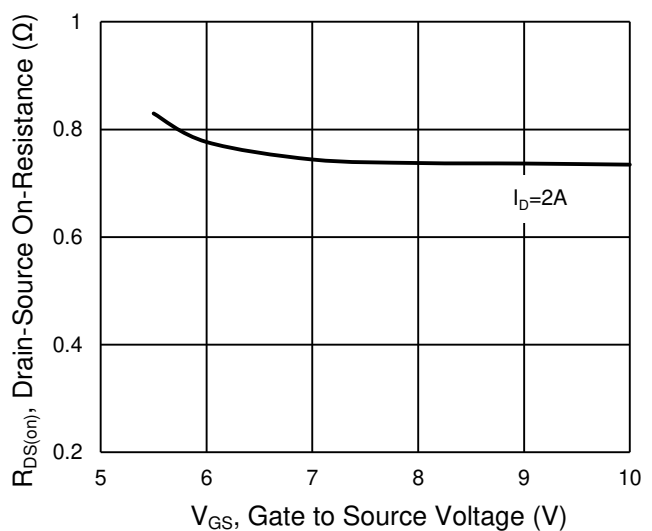
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



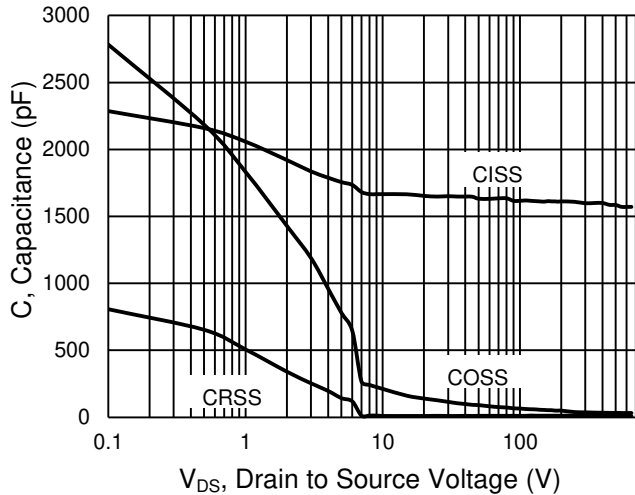
On-Resistance vs. Gate-Source Voltage



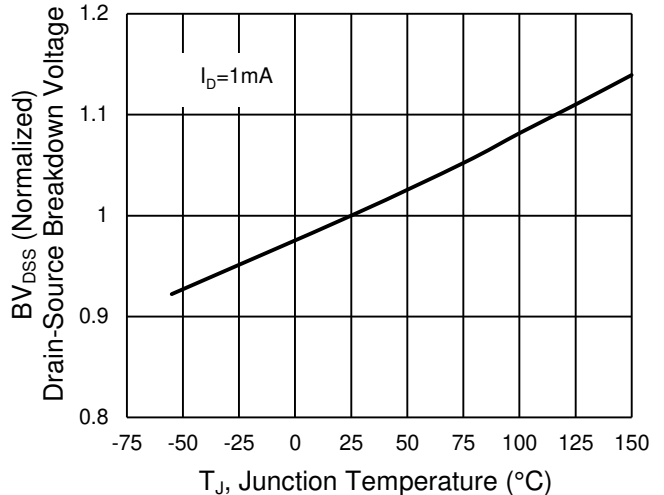
CHARACTERISTICS CURVES

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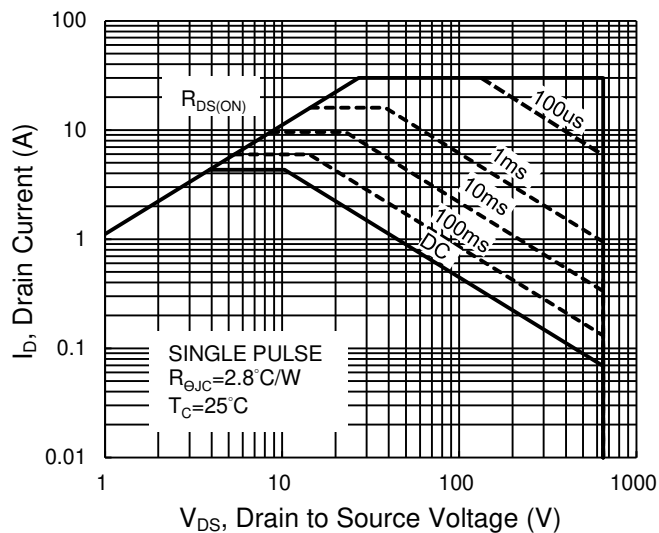
Capacitance vs. Drain-Source Voltage



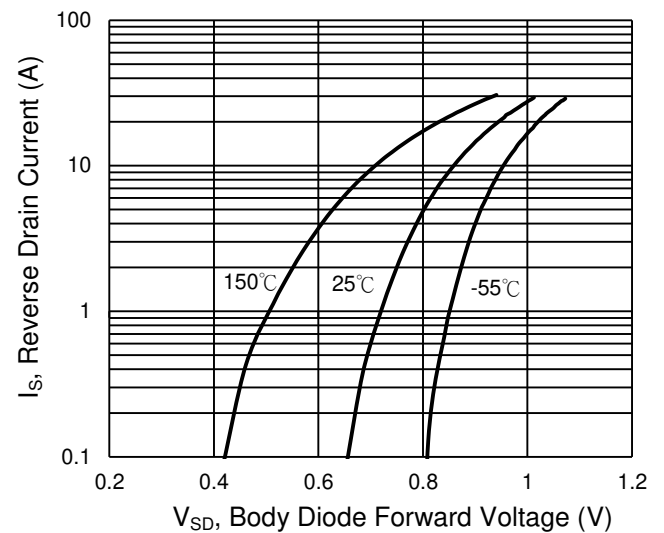
BV_{DSS} vs. Junction Temperature



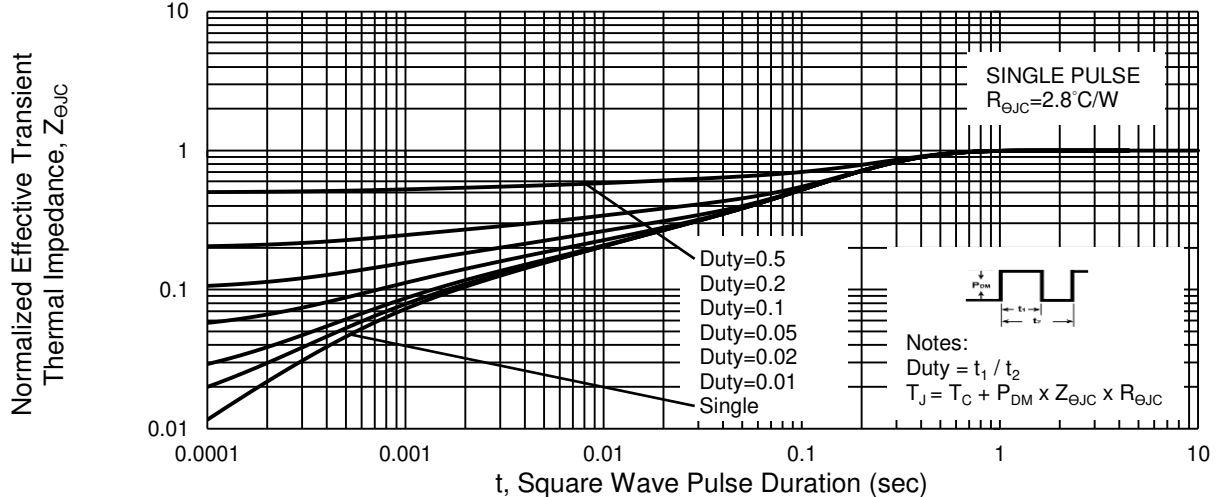
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage



Normalized Thermal Transient Impedance, Junction-to-Case



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