



# LOW SKEW, 1-TO-4 LVCMOS-TO-3.3V LVPECL FANOUT BUFFER

**IDT8535-01**

## FEATURES:

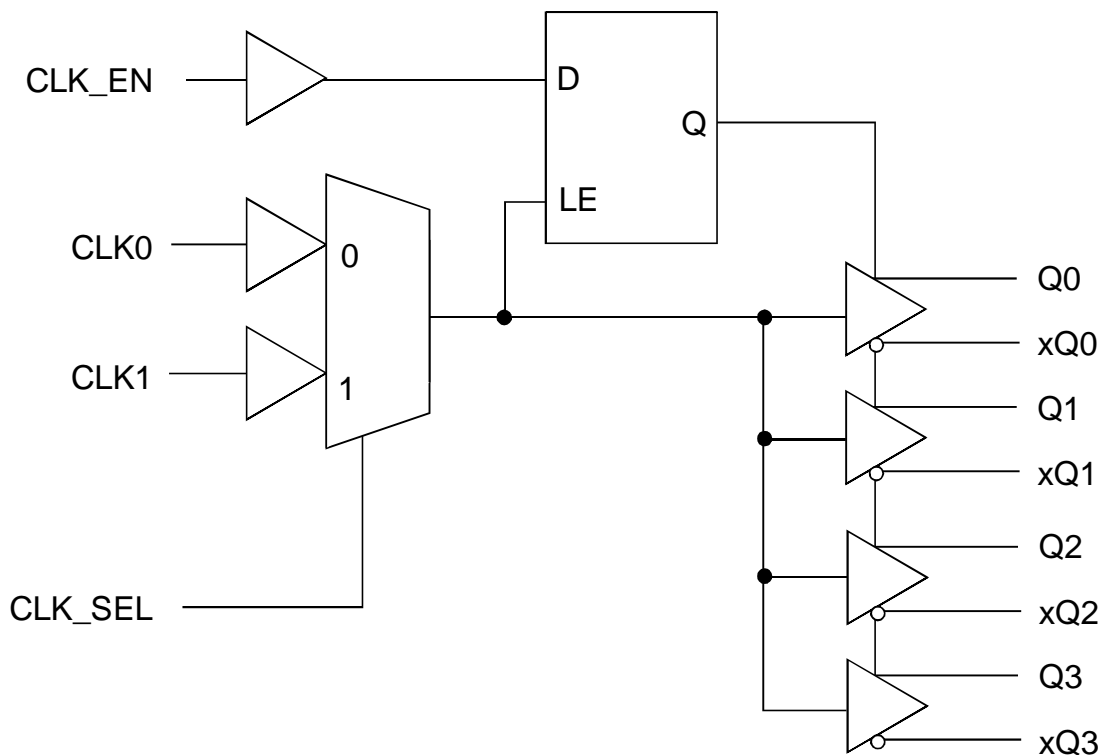
- Four differential 3.3V LVPECL outputs
- Selectable CLK0 or CLK1 inputs for redundant and multiple frequency fanout applications
- Maximum output frequency: 266MHz
- CLK0 or CLK1 can accept LVCMOS or LVTTTL input levels
- Translates LVCMOS and LVTTTL levels to 3.3V LVPECL levels
- Output skew: 30ps (max.)
- Part-to-part skew: as low as 150ps
- Propagation delay: 1.9ns (max.)
- 3.3V operating supply
- Available in TSSOP package

## DESCRIPTION:

The IDT8535-01 is a low skew, high performance 1-to-4 LVCMOS-to-3.3V LVPECL fanout buffer. It has two single-ended clock inputs. The single-ended clock input accepts LVCMOS or LVTTTL input levels and translates them to 3.3V LVPECL levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the IDT8535-01 ideal for those applications demanding well-defined performance and repeatability.

## FUNCTIONAL BLOCK DIAGRAM

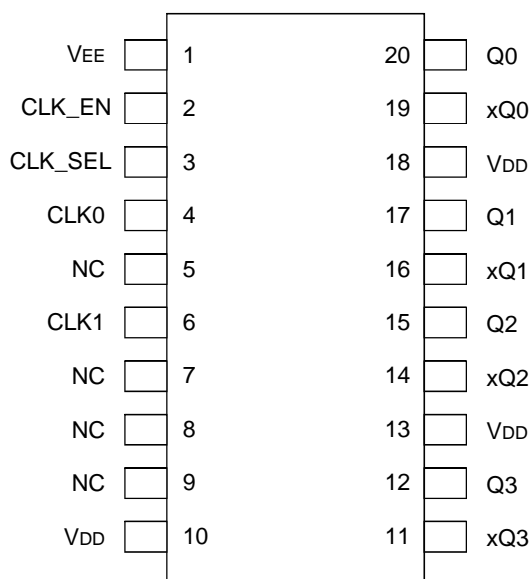


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COMMERCIAL AND INDUSTRIAL TEMPERATURE RANGES

AUGUST 2004

## PIN CONFIGURATION



TSSOP  
 TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
V <sub>DD</sub>	Power Supply Voltage	4.6	V
V <sub>I</sub>	Input Voltage	-0.5 to V <sub>DD</sub> +0.5	V
V <sub>O</sub>	Output Voltage	-0.5 to V <sub>DD</sub> +0.5	V
θ <sub>JA</sub>	Package Thermal Impedance (0 lfp/m)	92.6	°C/W
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C

NOTE:

- Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1MHz, V<sub>IN</sub> = 0V)

Parameter	Description	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	—	4	pF
R <sub>PULLUP</sub>	Input Pullup Resistor	51	—	KΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor	51	—	KΩ

## PIN DESCRIPTION<sup>(1)</sup>

Symbol	Number	Type	Description
V <sub>EE</sub>	1	Power	Negative Supply Pin
CLK_EN	2	Input Pullup	Synchronizing Clock Enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced LOW, xQ outputs are forced HIGH. LVCMOS / LVTTTL interface levels.
CLK_SEL	3	Input Pulldown	Clock Select Input. When HIGH, selects CLK1 input. When LOW, selects CLK0 input. LVCMOS / LVTTTL interface levels.
CLK0	4	Input Pulldown	LVCMOS / LVTTTL Clock Input
CLK1	6	Input Pulldown	LVCMOS / LVTTTL Clock Input
NC	5, 7, 8, 9	Unused	No Connection
V <sub>DD</sub>	10, 13, 18	Power	Positive Supply Pins
xQ3, Q3	11, 12	Output	Differential Output Pair. LVPECL interface levels.
xQ2, Q2	14, 15	Output	Differential Output Pair. LVPECL interface levels.
xQ1, Q1	16, 17	Output	Differential Output Pair. LVPECL interface levels.
xQ0, Q0	19, 20	Output	Differential Output Pair. LVPECL interface levels.

NOTE:

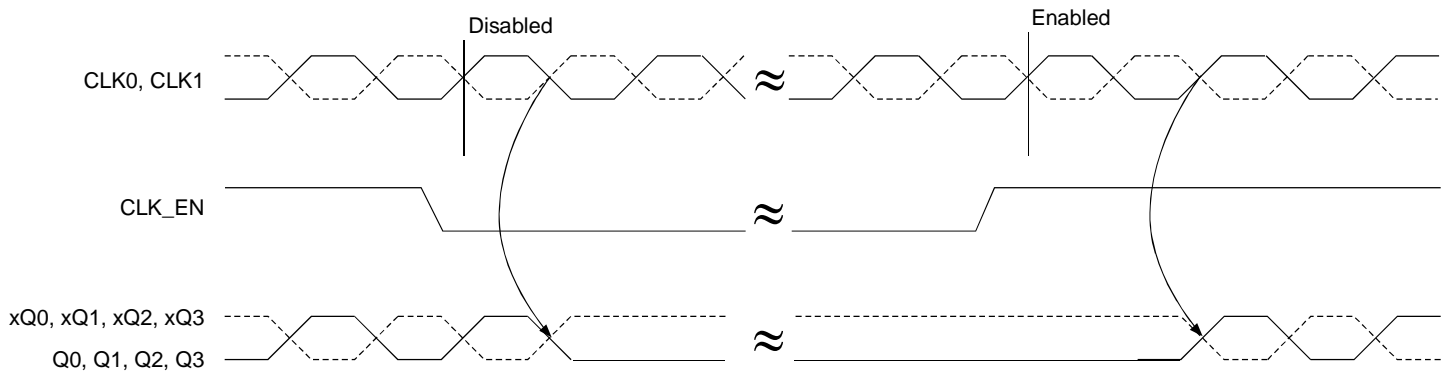
- Pullup and Pulldown refer to internal input resistors. See Capacitance table for typical values.

## CONTROL INPUT FUNCTION TABLE<sup>(1,2)</sup>

Inputs			Outputs	
CLK_EN	CLK_SEL	Selected Source	Q0 to Q3	xQ0 to xQ3
0	0	CLK0	Disabled; LOW	Disabled; HIGH
0	1	CLK1	Disabled; LOW	Disabled; HIGH
1	0	CLK0	Enabled	Enabled
1	1	CLK1	Enabled	Enabled

NOTES:

1. After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in the CLK\_EN Timing Diagram below.
2. In active mode, the state of the outputs is a function of the CLK / xCLK and PCLK / xPCLK inputs as described in the Clock Input Function table.



CLK\_EN Timing Diagram

## CLOCK INPUT FUNCTION TABLE<sup>(1)</sup>

Inputs	Outputs	
CLK0 or CLK1	Q0 to Q3	xQ0 to xQ3
0	L	H
1	H	L

NOTE:

1. H = HIGH  
 L = LOW

## POWER SUPPLY CHARACTERISTICS - COMMERCIAL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Positive Supply Voltage		3.135	3.3	3.465	V
I <sub>EE</sub>	Power Supply Current		—	—	50	mA

## DC ELECTRICAL CHARACTERISTICS, LVCMOS / LVTTTL - COMMERCIAL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>IH</sub>	Input Voltage HIGH		2		V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input Voltage LOW	CLK0, CLK1	-0.3		1.3	V
		CLK_EN, CLK_SEL	-0.3		0.8	
I <sub>IH</sub>	Input Current HIGH	CLK0, CLK1, CLK_SEL	V <sub>IN</sub> = V <sub>DD</sub> = 3.465V		150	μA
		CLK_EN	V <sub>IN</sub> = V <sub>DD</sub> = 3.465V		5	
I <sub>IL</sub>	Input Current LOW	CLK0, CLK1, CLK_SEL	V <sub>IN</sub> = 0V, V <sub>DD</sub> = 3.465V	-5		μA
		CLK_EN	V <sub>IN</sub> = 0V, V <sub>DD</sub> = 3.465V	-150		

## DC ELECTRICAL CHARACTERISTICS, LVPECL - COMMERCIAL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub>	Output Voltage HIGH <sup>(1)</sup>		V <sub>DD</sub> - 1.4		V <sub>DD</sub> - 1	V
V <sub>OL</sub>	Output Voltage LOW <sup>(1)</sup>		V <sub>DD</sub> - 2		V <sub>DD</sub> - 1.7	V
V <sub>SWING</sub>	Peak-to-Peak Output Voltage Swing		0.6		0.85	V

## NOTE:

1. Outputs terminated with 50Ω to V<sub>DD</sub> - 2V.

## AC ELECTRICAL CHARACTERISTICS - COMMERCIAL

All parameters measured at 266MHz unless noted otherwise;

Cycle-to-cycle jitter on input = jitter on output; the part does not add jitter

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
F <sub>MAX</sub>	Output Frequency				266	MHz
t <sub>PD</sub>	Propagation Delay <sup>(1)</sup>	f ≤ 266MHz	1		1.9	ns
t <sub>SK(O)</sub>	Output Skew <sup>(2,4)</sup>			11	30	ps
t <sub>SK(PP)</sub>	Part-to-Part Skew <sup>(3,4)</sup>				150	ps
t <sub>R</sub>	Output Rise Time	20 - 80% @ 50MHz	300		700	ps
t <sub>F</sub>	Output Fall Time	20 - 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		48	50	52	%

## NOTES:

1. Measured from the V<sub>DD</sub>/2 of the input to the differential output crossingpoint.
2. Defined as skew between outputs as the same supply voltage and with equal load conditions. Measured at the output differential crosspoints
3. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.
4. This parameter is defined in accordance with JEDEC Standard 65.

## POWER SUPPLY CHARACTERISTICS - INDUSTRIAL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Positive Supply Voltage		3.135	3.3	3.465	V
I <sub>EE</sub>	Power Supply Current		—	—	55	mA

## DC ELECTRICAL CHARACTERISTICS, LVCMOS / LVTTTL - INDUSTRIAL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>IH</sub>	Input Voltage HIGH		2		V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input Voltage LOW	CLK0, CLK1	-0.3		1.3	V
		CLK_EN, CLK_SEL	-0.3		0.8	
I <sub>IH</sub>	Input Current HIGH	CLK0, CLK1, CLK_SEL	V <sub>IN</sub> = V <sub>DD</sub> = 3.465V		150	μA
		CLK_EN	V <sub>IN</sub> = V <sub>DD</sub> = 3.465V		5	
I <sub>IL</sub>	Input Current LOW	CLK0, CLK1, CLK_SEL	V <sub>IN</sub> = 0V, V <sub>DD</sub> = 3.465V	-5		μA
		CLK_EN	V <sub>IN</sub> = 0V, V <sub>DD</sub> = 3.465V	-150		

## DC ELECTRICAL CHARACTERISTICS, LVPECL - INDUSTRIAL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub>	Output Voltage HIGH <sup>(1)</sup>		V <sub>DD</sub> - 1.4		V <sub>DD</sub> - 1	V
V <sub>OL</sub>	Output Voltage LOW <sup>(1)</sup>		V <sub>DD</sub> - 2		V <sub>DD</sub> - 1.7	V
V <sub>SWING</sub>	Peak-to-Peak Output Voltage Swing		0.6		0.85	V

## NOTE:

1. Outputs terminated with 50Ω to V<sub>DD</sub> - 2V.

## AC ELECTRICAL CHARACTERISTICS - INDUSTRIAL

All parameters measured at 266MHz unless noted otherwise;

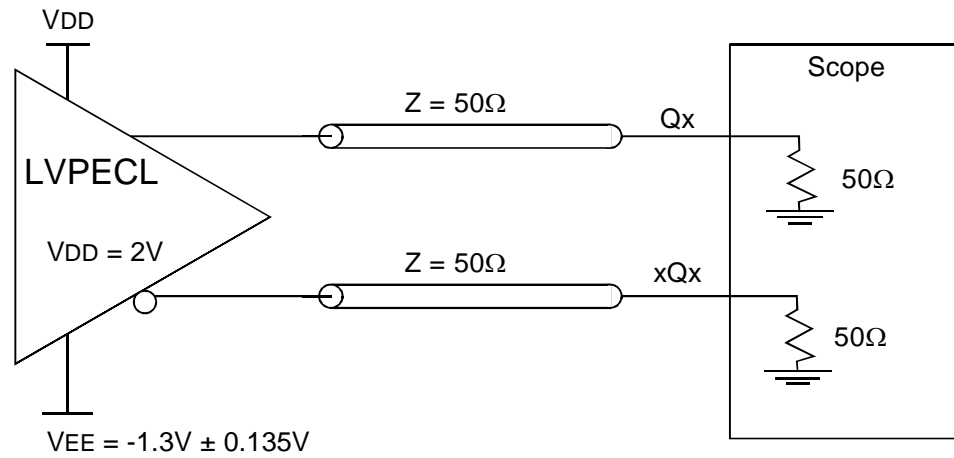
Cycle-to-cycle jitter on input = jitter on output; the part does not add jitter

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
F <sub>MAX</sub>	Output Frequency				266	MHz
t <sub>PD</sub>	Propagation Delay <sup>(1)</sup>	f ≤ 266MHz	1		1.9	ns
t <sub>SK(O)</sub>	Output Skew <sup>(2,4)</sup>				30	ps
t <sub>SK(PP)</sub>	Part-to-Part Skew <sup>(3,4)</sup>				200	ps
t <sub>R</sub>	Output Rise Time	20 - 80% @ 50MHz	300		700	ps
t <sub>F</sub>	Output Fall Time	20 - 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		48	50	52	%

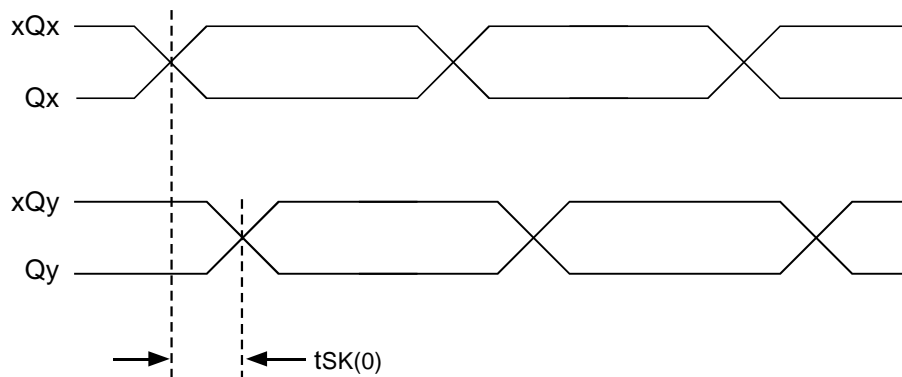
## NOTES:

1. Measured from the V<sub>DD</sub>/2 of the input to the differential output crossingpoint.
2. Defined as skew between outputs as the same supply voltage and with equal load conditions. Measured at the output differential crosspoints
3. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.
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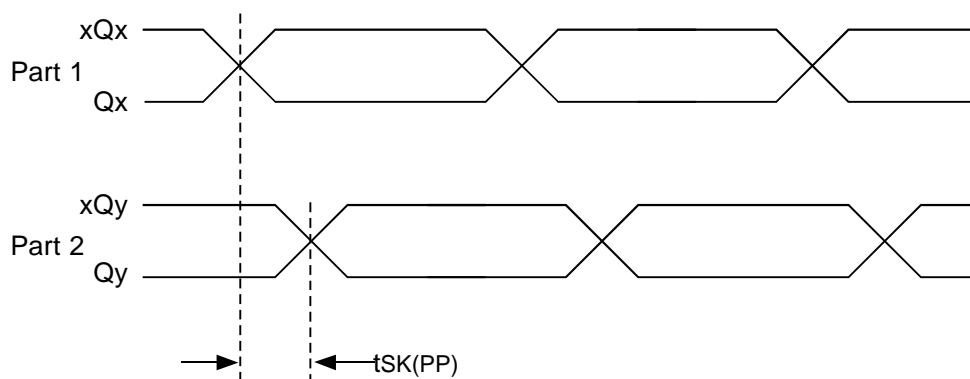
### PARAMETER MEASUREMENT INFORMATION



Output Load Test Circuit

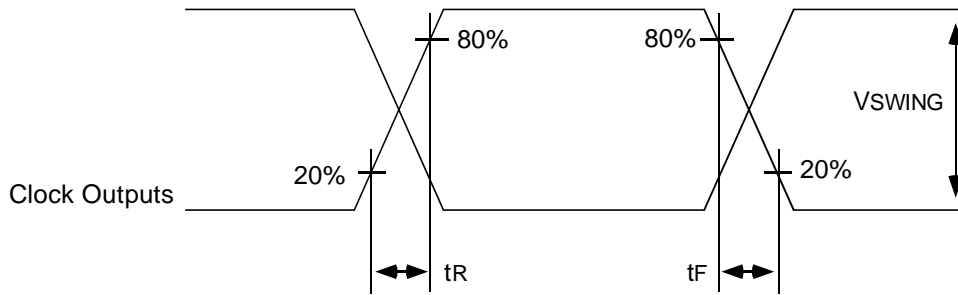


Output Skew

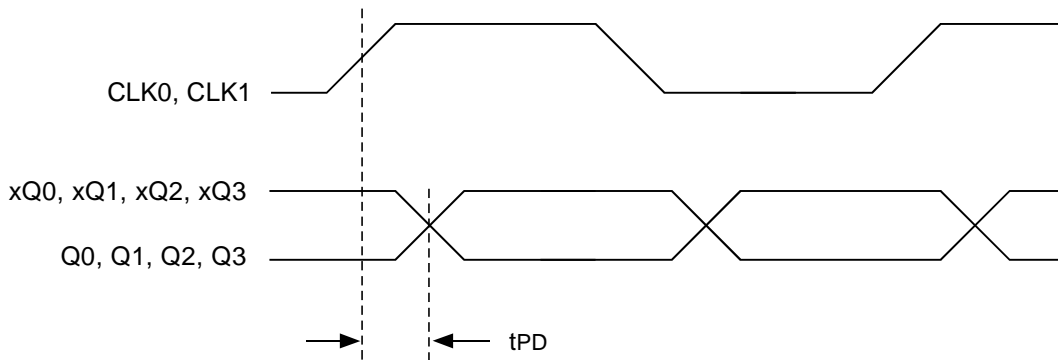


Part-to-Part Skew

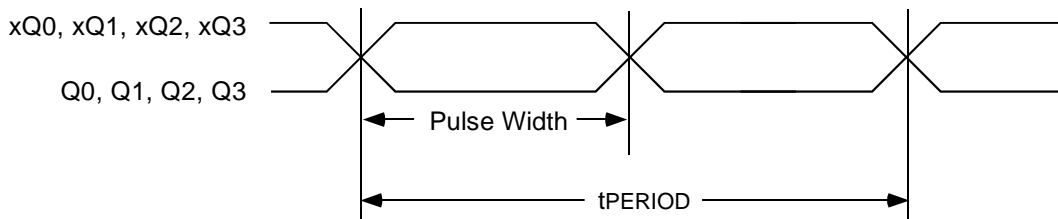
PARAMETER MEASUREMENT INFORMATION - CONTINUED



Output Rise and Fall Time



Propagation Delay



$$odc = \frac{tW}{t_{PERIOD}}$$

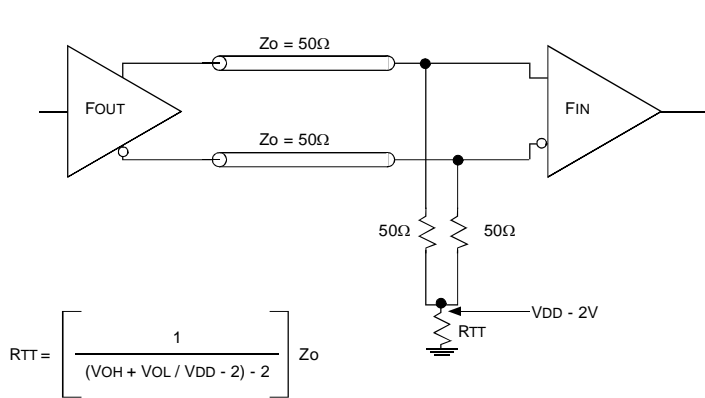
odc and  $t_{PERIOD}$

## APPLICATION INFORMATION

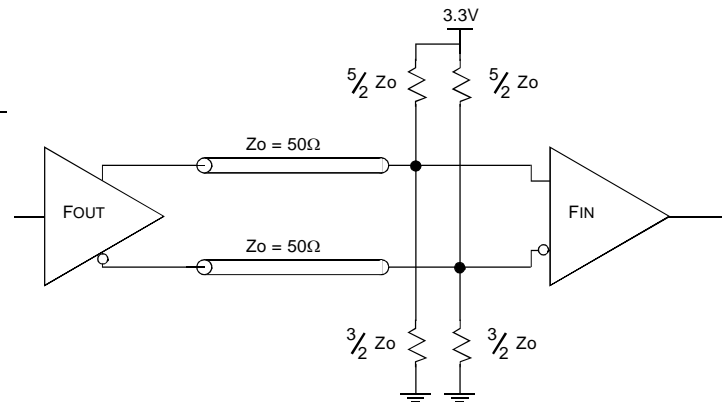
### TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

F<sub>OUT</sub> and xF<sub>OUT</sub> are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. The diagrams below show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist. It is recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.



LVPECL Output Termination, layout A



LVPECL Output Termination, layout B



## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the IDT8535-01. Equations and example calculations are also provided.

### POWER DISSIPATION:

The total power dissipation for the IDT8535-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for the  $V_{DD} = 3.3V + 5\% = 3.465V$  and Industrial Temperature grade, which gives worst case results. Please refer to the following section, Calculations and Equations, for details on calculating power dissipated in the load.

$$\text{Power (core)}_{MAX} = V_{DD\_MAX} * I_{CC\_MAX} = 3.465 * 55mA = 190.57mW$$

$$\text{Power (outputs)}_{MAX} = 30.2mW/\text{Loaded Output Pair}$$

$$\text{If all outputs are loaded, the total power is } 4 * 30.2mW = 120.8mW$$

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 190.57mW + 120.8mW = 311.37mW$$

### JUNCTION TEMPERATURE:

Junction temperature ( $t_J$ ) is the temperature at the junction of the bond wire and bond pad. It directly affects the reliability of the device. The maximum recommended junction temperature for this device is 125°C.

$$\text{The equation for } t_J \text{ is as follows: } t_J = \theta_{JA} * Pd_{total} + T_A$$

$t_J$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd_{total}$  = Total Device Power Dissipation (example calculation is in Power Dissipation, above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance ( $\theta_{JA}$ ) must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 77.6°C/W per the following Thermal Resistance table. Therefore,  $t_J$  for an ambient temperature of 85°C with all its outputs switching is:

$$85^\circ C + 0.311W * 77.6^\circ C/W = 109.16^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

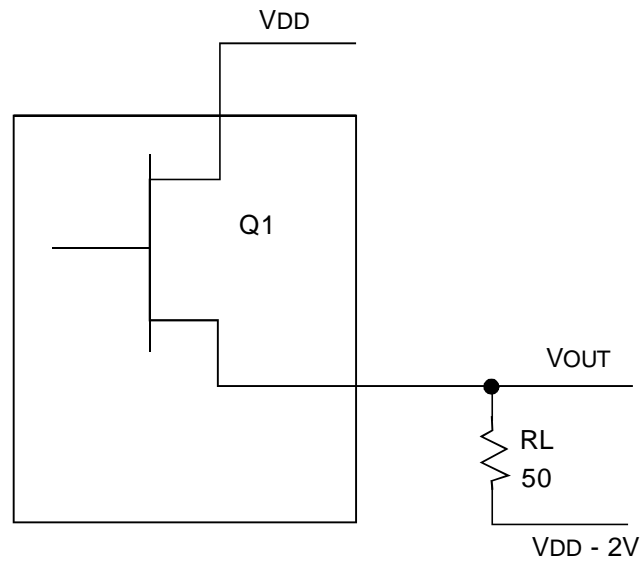
This calculation is only an example.  $t_J$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single-layer or multi-layer).

## THERMAL RESISTANCE

$\theta_{JA}$  for 20-pin TSSOP, forced convection

$\theta_{JA}$ by Velocity (Linear Feet per minute)				
	0	200	400	Unit
Multi-Layer PCB, JEDEC Standard Test boards	92.6	77.6	70.9	°C/W

## CALCULATIONS AND EQUATIONS



*LVPECL Output Driver Circuit and Termination*

To calculate worst case power dissipation into the load, use the following equations, which assume a  $50\Omega$  load and a termination voltage of  $V_{DD} - 2V$ .

For Logic HIGH:  $V_{OUT} = V_{OH\_MAX} = V_{DD\_MAX} - 1V$ .

$(V_{DD\_MAX} - V_{OH\_MAX}) = 1V$

For Logic LOW:  $V_{OUT} = V_{OL\_MAX} = V_{DD\_MAX} - 1.7V$ .

$(V_{DD\_MAX} - V_{OL\_MAX}) = 1.7V$

$Pd\_H$  is power dissipation when the output drives HIGH.

$Pd\_L$  is power dissipation when the output drives LOW.

$$Pd\_H = \left\{ \left[ \frac{V_{OH\_MAX} - (V_{DD\_MAX} - 2V)}{R_L} \right] * (V_{DD\_MAX} - V_{OH\_MAX}) \right\} = \left\{ \left[ \frac{2V - (V_{DD\_MAX} - V_{OH\_MAX})}{R_L} \right] * (V_{DD\_MAX} - V_{OH\_MAX}) \right\} = \left[ \frac{(2V - 1V)}{50\Omega} \right] * 1V = 20mW.$$

$$Pd\_L = \left\{ \left[ \frac{V_{OL\_MAX} - (V_{DD\_MAX} - 2V)}{R_L} \right] * (V_{DD\_MAX} - V_{OL\_MAX}) \right\} = \left\{ \left[ \frac{2V - (V_{DD\_MAX} - V_{OL\_MAX})}{R_L} \right] * (V_{DD\_MAX} - V_{OL\_MAX}) \right\} = \left[ \frac{(2V - 1.7V)}{50\Omega} \right] * 1.7V = 10.2mW.$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = 30.2mW$$

## ORDERING INFORMATION

IDT	XXXXX	XX	X		
Device Type	Package	Process			
				Blank	Commercial (0°C to +70°C) Industrial (-40°C to +85°C)
				I	
				PG	Thin Shrink Small Outline Package
				8535-01	Low Skew, 1-to-4 LVCMOS-to-3.3V LVPECL Fanout Buffer



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