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# NTE4503B
# Integrated Circuit
# CMOS, Hex 3−State Non−Inverting Buffer

**Description:**

The NTE4503B is a hex non−inverting buffer in a 16−Lead DIP type package with 3−state outputs and a high current source and sink capability. The 3−state outputs make it useful in common bussing applications. Two disable controls are provided. A high level on the Disable A input causes the outputs of buffers 1 through 4 to go into a high impedance state and a high level on the Disable B input causes the outputs of buffers 5 and 6 to go into a high impedance state.

**Features:**

- 3−State Outputs
- TTL Compatible − Will Drive One TTL Load Over Full Temperature Range
- Supply Voltage Range: 3Vdc to 18Vdc
- Symmetrical Turn−On and Turn−Off Delays
- Symmetrical Output Rise and Fall Times
- Two Disable Controls for Added Versatility

**Absolute Maximum Ratings:** (Voltages referenced to $V_{SS}$, Note 1)

DC Supply Voltage, $V_{DD}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −0.5 to +18.0V
Input Voltage (All Inputs), $V_{in}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −0.5 to $V_{DD}$ to +0.5V
DC Current Drain, I
Per Input Pin . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 10mA
Per Output Pin . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 25mA
Operating Temperature Range, $T_A$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −55° to +125°C
Storage Temperature Range, $T_{stg}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −65° to +150°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V9in9 and V9out9 be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic level (e.g., either $V_{SS}$ or $V_{DD}$).

## **Electrical Characteristics:** (Voltages referenced to $V_{SS}$, Note 2)

| Parameter | Symbol | $V_{DD}$ Vdc | −55°C | | +25°C | | | +125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| Output Voltage "0" Level | $V_{OL}$ | 5.0 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | Vdc |
| $V_{in}$ = $V_{DD}$ or 0 | | 10 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | Vdc |
| | | 15 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | Vdc |
| "1" Level | $V_{OH}$ | 5.0 | 4.95 | – | 4.95 | 5.0 | – | 4.95 | – | Vdc |
| $V_{in}$ = 0 or $V_{DD}$ | | 10 | 9.95 | – | 9.95 | 10 | – | 9.95 | – | Vdc |
| | | 15 | 14.95 | – | 14.95 | 15 | – | 14.95 | – | Vdc |
| Noise Immunity (Note 4) "0" Level ($V_O$ = 3.6 or 1.4Vdc) | $V_{IL}$ | 5.0 | – | 1.5 | – | 2.25 | 1.5 | – | 1.5 | Vdc |
| ($V_O$ = 7.2 or 2.8Vdc) | | 10 | – | 3.0 | – | 4.50 | 3.0 | – | 3.0 | Vdc |
| ($V_O$ = 11.5 or 3.5Vdc) | | 15 | – | 3.75 | – | 6.75 | 3.75 | – | 3.75 | Vdc |
| "1" Level ($V_O$ = 1.4 or 3.6Vdc) | $V_{IH}$ | 5.0 | 3.5 | – | 3.5 | 2.75 | – | 3.5 | – | Vdc |
| ($V_O$ = 2.8 or 7.2Vdc) | | 10 | 7.0 | – | 7.0 | 5.50 | – | 7.0 | – | Vdc |
| ($V_O$ = 3.5 or 11.5Vdc) | | 15 | 11.25 | – | 11.25 | 8.25 | – | 11.25 | – | Vdc |
| Output Drive Current Source ($V_{OH}$ = 2.5Vdc) | $I_{OH}$ | 4.5 | −4.3 | – | −3.6 | −5.0 | – | −2.5 | – | mAdc |
| ($V_{OH}$ = 2.5Vdc) | | 5.0 | −5.8 | – | −4.8 | −6.1 | – | −3.0 | – | mAdc |
| ($V_{OH}$ = 4.6Vdc) | | 5.0 | −1.2 | – | −1.02 | −1.4 | – | −0.7 | – | mAdc |
| ($V_{OH}$ = 9.5Vdc) | | 10 | −3.1 | – | −2.6 | −3.7 | – | −1.8 | – | mAdc |
| ($V_{OH}$ = 13.5Vdc) | | 15 | −8.2 | – | −6.8 | −14.1 | – | −4.8 | – | mAdc |
| Sink ($V_{OL}$ = 0.4Vdc) | $I_{OL}$ | 4.5 | 2.2 | – | 1.8 | 2.1 | – | 1.2 | – | mAdc |
| ($V_{OL}$ = 0.4Vdc) | | 5.0 | 2.6 | – | 2.1 | 2.3 | – | 1.3 | – | mAdc |
| ($V_{OL}$ = 0.5Vdc) | | 10 | 6.5 | – | 5.5 | 6.2 | – | 3.8 | – | mAdc |
| ($V_{OL}$ = 1.5Vdc) | | 15 | 19.2 | – | 16.1 | 25.0 | – | 11.2 | – | mAdc |
| Input Current | $I_{in}$ | 15 | – | ±0.1 | – | ±0.00001 | ±0.1 | – | ±0.1 | µAdc |
| Input Capacitance ($V_{IN}$ = 0) | $C_{in}$ | – | – | – | – | 5.0 | 7.5 | – | – | pF |
| Quiescent Current (Per Package) | $I_{DD}$ | 5.0 | – | 1.0 | – | 0.002 | 1.0 | – | 30 | µAdc |
| | | 10 | – | 2.0 | – | 0.004 | 2.0 | – | 60 | µAdc |
| | | 15 | – | 4.0 | – | 0.006 | 4.0 | – | 120 | µAdc |
| Total Supply Current (Dynamic plus Quiescent, Per Package, $C_L$ = 50pF on all outputs, all outputs switching, 50% Duty Cycle, Note 3, Note 5) | $I_T$ | 5.0 | $I_T$ = (2.5µA/kHz) f + $I_{DD}$ | | | | | | | µAdc |
| | | 10 | $I_T$ = (6.0µA/kHz) f + $I_{DD}$ | | | | | | | µAdc |
| | | 15 | $I_T$ = (10µA/kHz) f + $I_{DD}$ | | | | | | | µAdc |
| Three State Leakage Current | $I_{TL}$ | 15 | – | ±0.1 | – | ±0.00001 | ±0.1 | – | ±3.0 | µAdc |

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. Noise immunity specified for worst−case input combination.
Noise margin for both "1" and "0" = 1.0Vdc min @ $V_{DD}$ = 5Vdc
2.0Vdc min @ $V_{DD}$ = 10Vdc
2.5Vdc min @ $V_{DD}$ = 15Vdc

Note 5. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 6 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: $I_T$ is in µA (per package), $C_L$ in pF, $V_{DD}$ in Vdc, f in kHz is input frequency.

**Switching Characteristics:** ($C_L$ = 50pF, $T_A$ = +25°C, Note 2)

| Parameter | Symbol | $V_{DD}$ Vdc | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise Time | $t_{TLH}$ | | | | | |
| $t_{TLH}$ = (0.5ns/pf) $C_L$ + 20ns | | 5.0 | – | 45 | 90 | ns |
| $t_{TLH}$ = (0.3ns/pf) $C_L$ + 8ns | | 10 | – | 23 | 45 | ns |
| $t_{TLH}$ = (0.2ns/pf) $C_L$ + 8ns | | 15 | – | 18 | 35 | ns |
| Output Fall Time | $t_{THL}$ | | | | | |
| $t_{THL}$ = (0.5ns/pf) $C_L$ + 20ns | | 5.0 | – | 45 | 90 | ns |
| $t_{THL}$ = (0.3ns/pf) $C_L$ + 8ns | | 10 | – | 23 | 45 | ns |
| $t_{THL}$ = (0.2ns/pf) $C_L$ + 8ns | | 15 | – | 18 | 35 | ns |
| Turn−Off Delay Time, All Outputs | $t_{PLH}$ | | | | | |
| $t_{PLH}$ = (0.3ns/pf) $C_L$ + 60ns | | 5.0 | – | 75 | 150 | ns |
| $t_{PLH}$ = (0.15ns/pf) $C_L$ + 27ns | | 10 | – | 35 | 70 | ns |
| $t_{PLH}$ = (0.1ns/pf) $C_L$ + 20ns | | 15 | – | 25 | 50 | ns |
| Turn−On Delay Time, All Outputs | $t_{PHL}$ | | | | | |
| $t_{PHL}$ = (0.3ns/pf) $C_L$ + 60ns | | 5.0 | – | 75 | 150 | ns |
| $t_{PHL}$ = (0.15ns/pf) $C_L$ + 27ns | | 10 | – | 35 | 70 | ns |
| $t_{PHL}$ = (0.1ns/pf) $C_L$ + 20ns | | 15 | – | 25 | 50 | ns |
| 3−State Propagation Delay, Output “1” to High Impedance | $t_{PHZ}$ | 5.0 | – | 75 | 150 | ns |
| | | 10 | – | 40 | 80 | ns |
| | | 15 | – | 35 | 70 | ns |
| 3−State Propagation Delay, High Impedance to Output “1” | $t_{PZH}$ | 5.0 | – | 65 | 130 | ns |
| | | 10 | – | 25 | 50 | ns |
| | | 15 | – | 20 | 40 | ns |
| 3−State Propagation Delay, Output “0” to High Impedance | $t_{PLZ}$ | 5.0 | – | 80 | 160 | ns |
| | | 10 | – | 40 | 80 | ns |
| | | 15 | – | 35 | 70 | ns |
| 3−State Propagation Delay, High Impedance to Output “0” | $t_{PZL}$ | 5.0 | – | 100 | 200 | ns |
| | | 10 | – | 35 | 70 | ns |
| | | 15 | – | 25 | 50 | ns |

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

**Truth Table**

| $In_n$ | Appropriate Disable Input | $Out_n$ |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| X | 1 | High Impedance |

X = Don’t Care

**Pin Connection Diagram**