

Photolink- Fiber Optic Receiver PLR155 SERIES



Features

- High PD sensitivity optimized for red light
- Data : NRZ signal
- Low power consumption for extended battery life
- Built-in threshold control for improved noise Margin
- The product itself will remain within RoHS compliant version.
- Receiver sensitivity: up to -27dBm (Min. for 16Mbps)
- The product itself will remain within RoHS compliant version.
- Compliance with EU REACH
- Compliance Halogen Free(Br<900ppm,Cl<900ppm,Br+Cl<1500ppm)

Description

The optical receiver is packaged with custom optic data link interface, integrated on a proprietary CMOS PDIC process.

The unit functions by converting optical signals into electric ones.

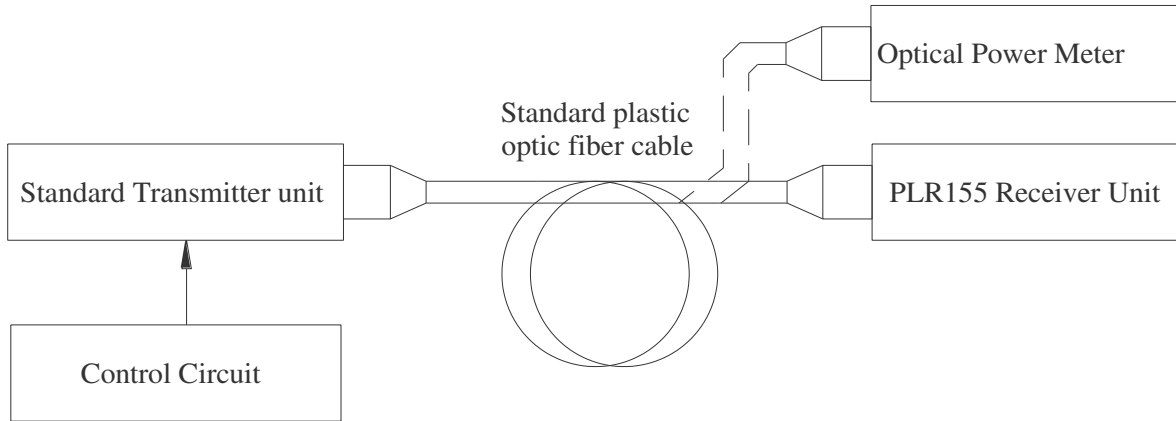
The unit is operated at 2.4 ~ 5.5 V and the signal output interface is TTL compatible with high performance at low power consumption.

Applications

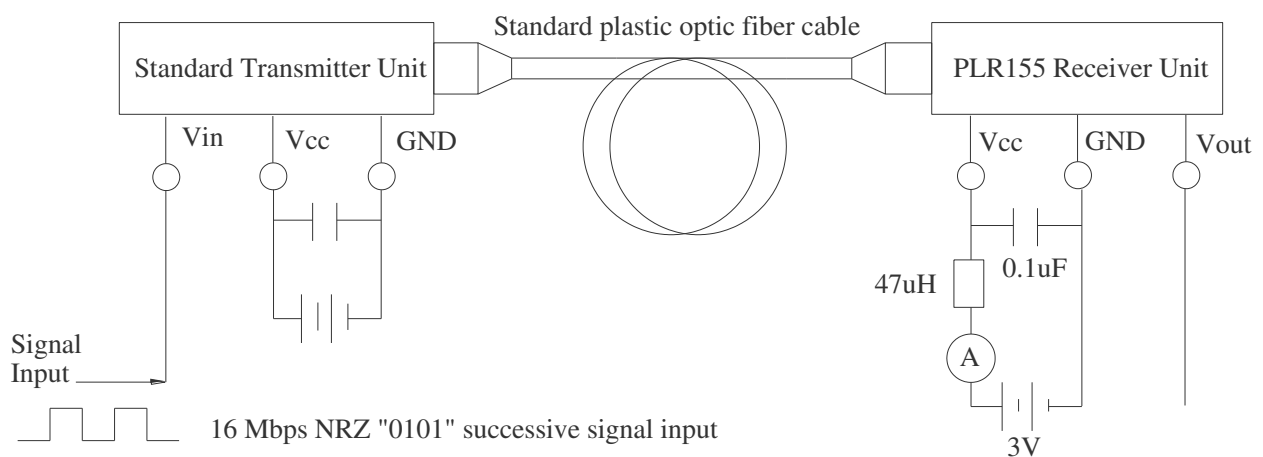
- Digital Optical Data-Link
- Dolby AC-3 Digital Audio Interface

Measuring Method

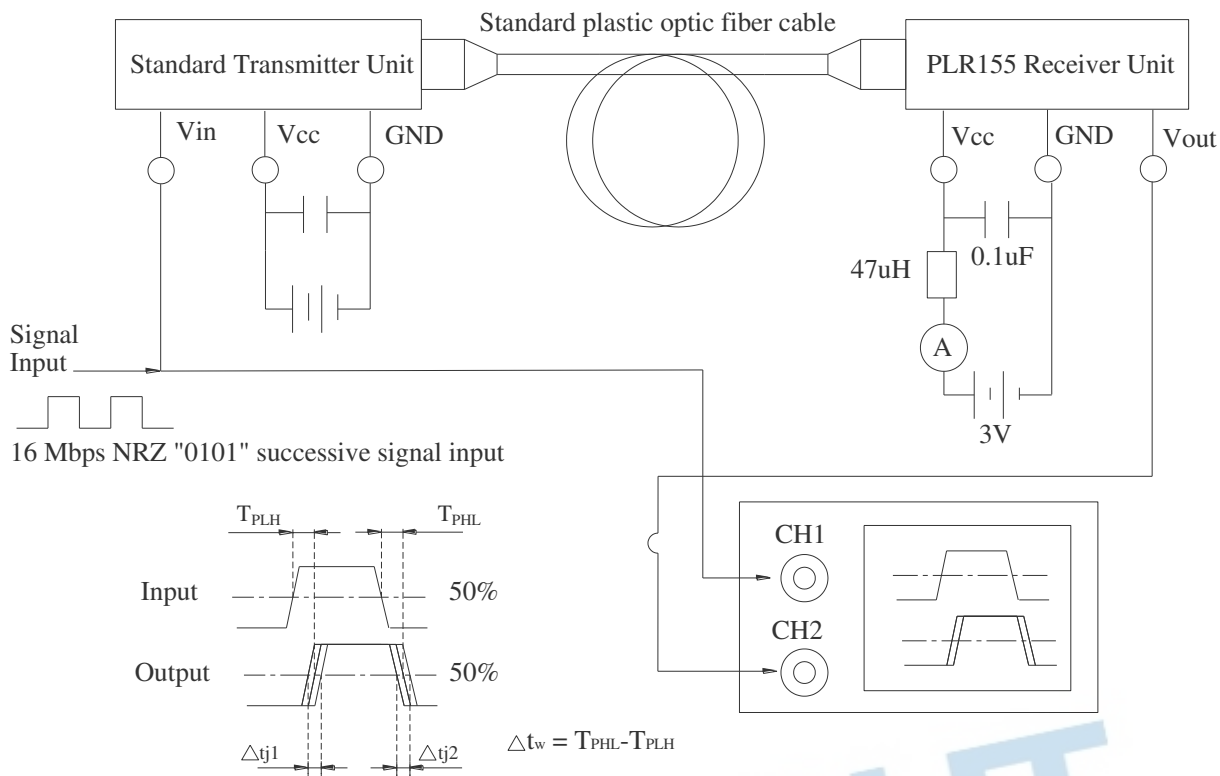
*Fig.1 Measuring Method of Maximum and Minimum Input Power that Receiver Unit Need



*Fig.2 Measuring Method of Dissipation Current



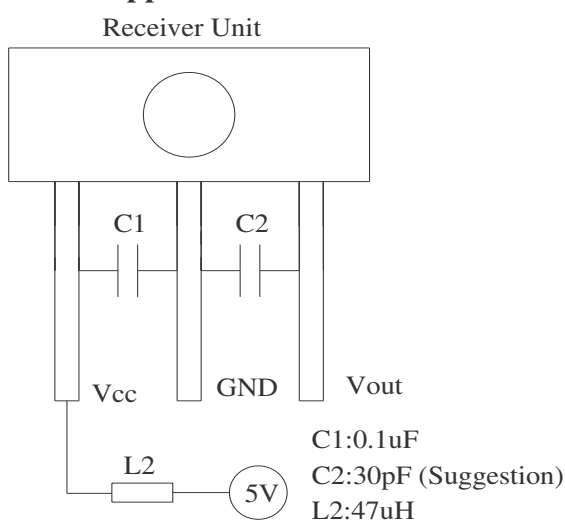
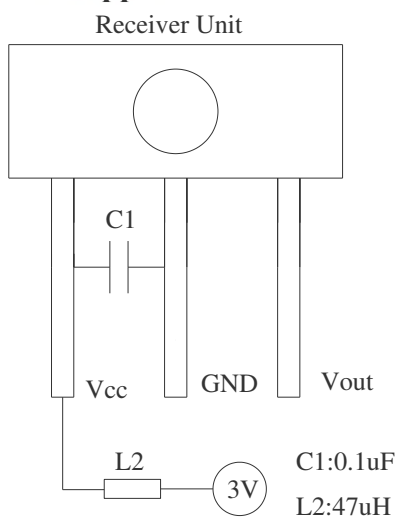
*Fig.3 Measuring Method of Output Voltage, Pulse and Jitter



Application Circuit

(1) General application circuit for Vcc=3V

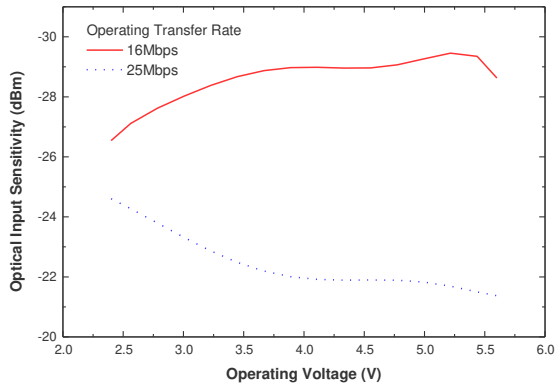
(2) General application circuit for Vcc=5V



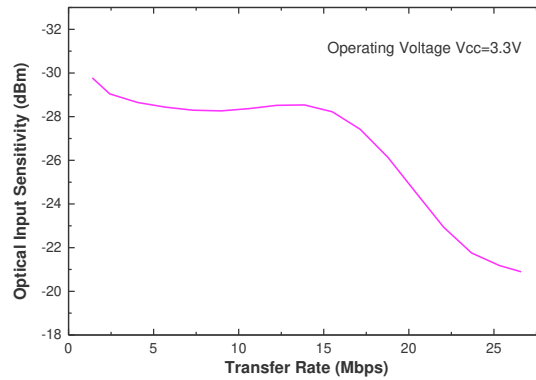
Note: For having good coupling, the C1,C2 capacitor must be placed within 7mm

Typical Electro-Optical Characteristics Curves

*Fig.4 Power supply voltage vs. Minimum receiver power



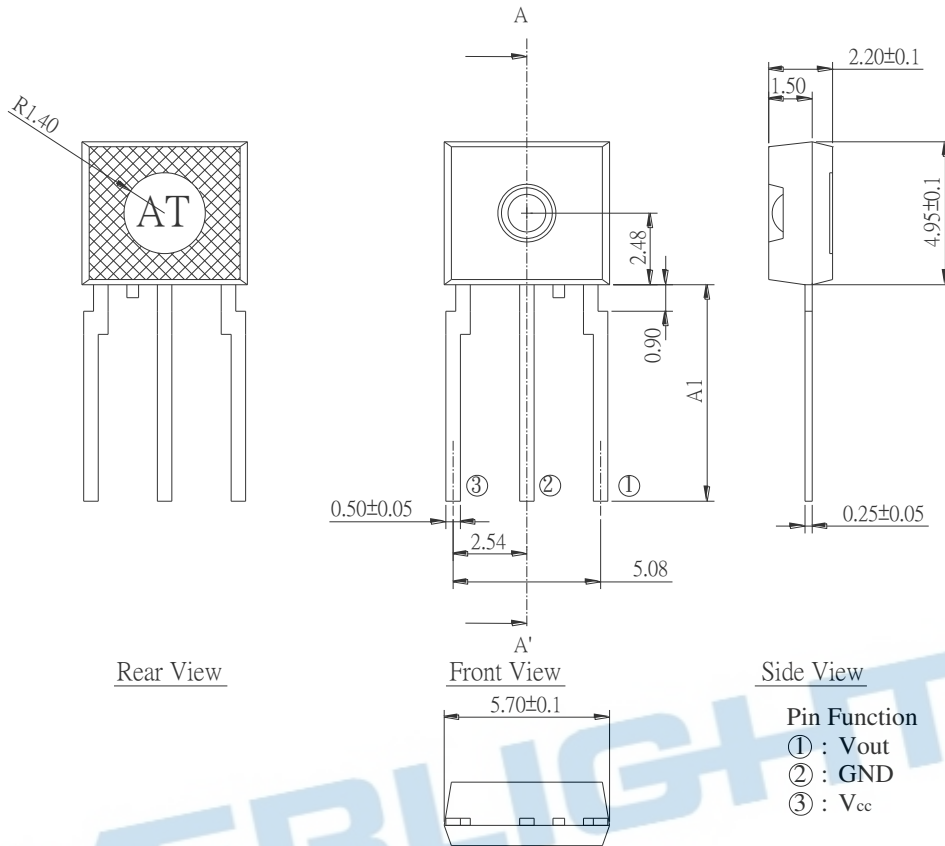
*Fig.5 Transfer rate vs. Minimum receiver power



Note: Before using the PLR155 device, please confirm the minimum sensitivity at different operating voltage and transmission rate.

EVERLIGHT

Package Dimension



Notes:

1. All dimensions are in mm.
2. General Tolerance: ±0.10 mm
3. Device Selection Table:

Device Name	Pin Length A1 (mm)
PLR155	12.55±0.25
PLR155/S1	7.50±0.25
PLR155/S2	5.22±0.25
PLR155/S3	10.20±0.25
PLR155/S5	16.50 Min

Application Notes: PLR155 Series PCB layout for motherboard integration

To achieve better jitter and low input optical power performances, several PCB layout guidelines must be followed. These guidelines ensure the most reliable PLR155 POF performance for the motherboard integration. Failed to implement these PCB guidelines may affect the PLR155 jitter and low input power performances.

1. Careful decoupling of the power supplies is very important. Place a 0.1uf surface mount (size 805 or smaller) capacitor as close as (less than 2cm) to the POF Vdd and Gnd leads. The 0.1uf act as a low impedance path to ground for any stray high frequency transient noises.
2. To reduce the digital noises form the digital IC on the motherboard, the planar capacitance formed by an isolated Vcc and Gnd planes is critical. The POF device must be mounted directly on these two planes to reduce the lead parasitic inductance.
3. The isolated Vdd and Gnd planes must be connected to the main Vcc and Gnd (digital) planes at a single point using ferrite beads. The beads are used to block the high frequency noises from the digital planes while still allowing the DC connections between the planes

