

## FEATURES

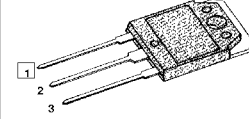
- ◆ Avalanche Rugged Technology
- ◆ Rugged Gate Oxide Technology
- ◆ Lower Input Capacitance
- ◆ Improved Gate Charge
- ◆ Extended Safe Operating Area
- ◆ Lower Leakage Current: 10 $\mu$ A (Max.) @  $V_{DS} = 400V$
- ◆ Low  $R_{DS(ON)}$ : 0.254 $\Omega$  (Typ.)

$$BV_{DSS} = 400 \text{ V}$$

$$R_{DS(on)} = 0.3\Omega$$

$$I_D = 17 \text{ A}$$

TO-3P



1. Gate 2. Drain 3. Source

## Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
$V_{DSS}$	Drain-to-Source Voltage	400	V
$I_D$	Continuous Drain Current ( $T_C=25^\circ\text{C}$ )	17	A
	Continuous Drain Current ( $T_C=100^\circ\text{C}$ )	10.8	
$I_{DM}$	Drain Current-Pulsed (1)	68	A
$V_{GS}$	Gate-to-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (2)	1156	mJ
$I_{AR}$	Avalanche Current (1)	17	A
$E_{AR}$	Repetitive Avalanche Energy (1)	20.2	mJ
dv/dt	Peak Diode Recovery dv/dt (3)	4.0	V/ns
$P_D$	Total Power Dissipation ( $T_C=25^\circ\text{C}$ )	202	W
	Linear Derating Factor	1.61	
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temp. for Soldering Purposes, 1/8. from case for 5-seconds	300	

## Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	0.62	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Case-to-Sink	0.24	--	
$R_{\theta JA}$	Junction-to-Ambient	--	40	

**Electrical Characteristics** ( $T_C=25^\circ\text{C}$  unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$BV_{DSS}$	Drain-Source Breakdown Voltage	400	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.46	--	V/°C	$I_D=250\mu A$ <b>See Fig 7</b>
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	4.0	V	$V_{DS}=5V, I_D=250\mu A$
$I_{GSS}$	Gate-Source Leakage, Forward	--	--	100	nA	$V_{GS}=30V$
	Gate-Source Leakage, Reverse	--	--	-100		$V_{GS}=-30V$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	10	$\mu A$	$V_{DS}=400V$
		--	--	100		$V_{DS}=320V, T_C=125^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.3	$\Omega$	$V_{GS}=10V, I_D=8.5A$ (4)
$g_{fs}$	Forward Transconductance	--	11.65	--	$\text{S}$	$V_{DS}=50V, I_D=8.5A$ (4)
$C_{iss}$	Input Capacitance	--	2140	2780	pF	$V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$ <b>See Fig 5</b>
$C_{oss}$	Output Capacitance	--	305	350		
$C_{rss}$	Reverse Transfer Capacitance	--	134	155		
$t_{d(on)}$	Turn-On Delay Time	--	20	50	ns	$V_{DD}=200V, I_D=17A,$ $R_G=6.2\Omega$ <b>See Fig 13</b> (4) (5)
$t_r$	Rise Time	--	22	55		
$t_{d(off)}$	Turn-Off Delay Time	--	100	210		
$t_f$	Fall Time	--	32	75		
$Q_g$	Total Gate Charge	--	101	131	nC	$V_{DS}=320V, V_{GS}=10V,$ $I_D=17A$ <b>See Fig 6 &amp; Fig 12</b> (4) (5)
$Q_{gs}$	Gate-Source Charge	--	14	--		
$Q_{gd}$	Gate-Drain (. Miller. ) Charge	--	51.5	--		

**Source-Drain Diode Ratings and Characteristics**

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$I_S$	Continuous Source Current	--	--	17	A	Integral reverse pn-diode in the MOSFET
$I_{SM}$	Pulsed-Source Current (1)	--	--	68		
$V_{SD}$	Diode Forward Voltage (4)	--	--	1.5	V	$T_J=25^\circ\text{C}, I_S=17A, V_{GS}=0V$
$t_{rr}$	Reverse Recovery Time	--	385	--	ns	$T_J=25^\circ\text{C}, I_F=17A$
$Q_{rr}$	Reverse Recovery Charge	--	4.85	--	$\mu\text{C}$	$di_F/dt=100A/\mu\text{s}$ (4)

**Notes;**

- (1) Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
- (2)  $L=7\text{mH}, I_{AS}=17A, V_{DD}=50V, R_G=27\Omega,$  Starting  $T_J=25^\circ\text{C}$
- (3)  $I_{SD} \leq 17A, di/dt \leq 250A/\mu\text{s}, V_{DD} \leq BV_{DSS},$  Starting  $T_J=25^\circ\text{C}$
- (4) Pulse Test: Pulse Width =  $250\mu\text{s},$  Duty Cycle  $\leq 2\%$
- (5) Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

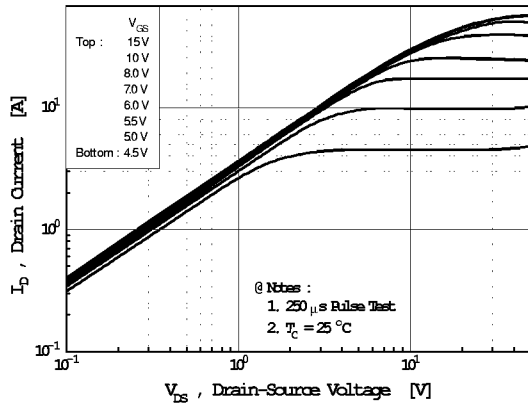


Fig 2. Transfer Characteristics

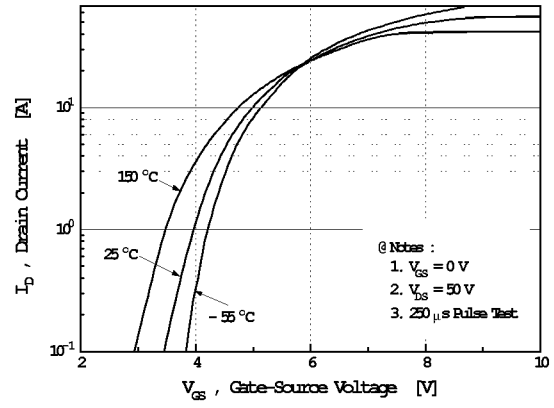


Fig 3. On-Resistance vs. Drain Current

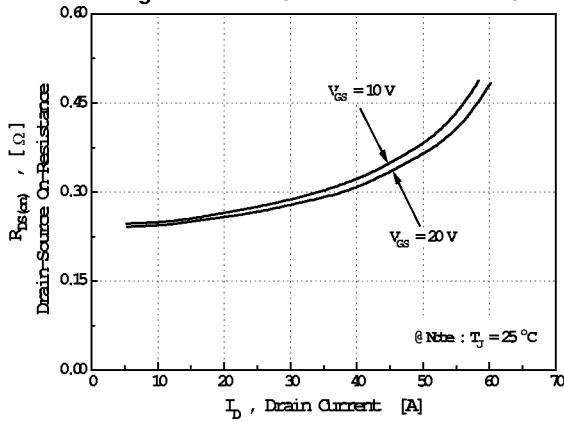


Fig 4. Source-Drain Diode Forward Voltage

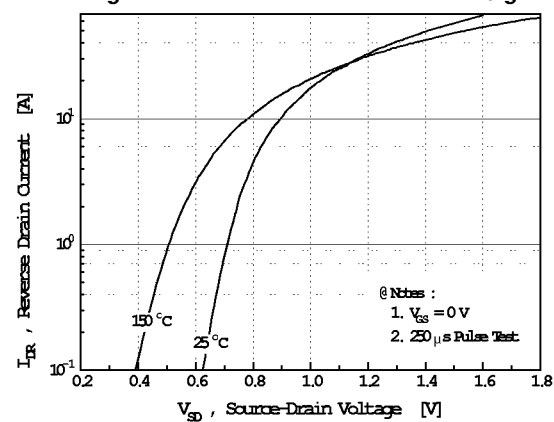


Fig 5. Capacitance vs. Drain-Source Voltage

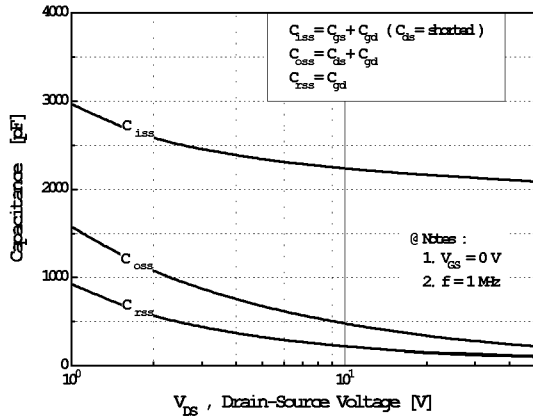
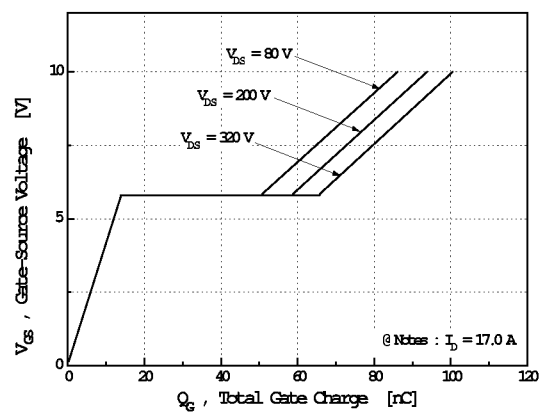
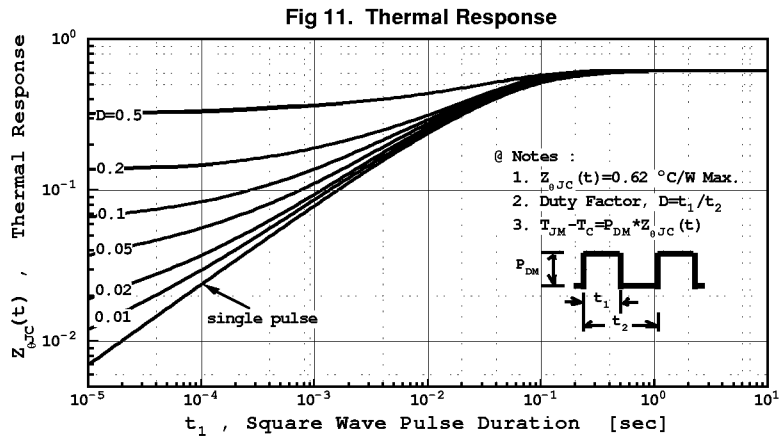
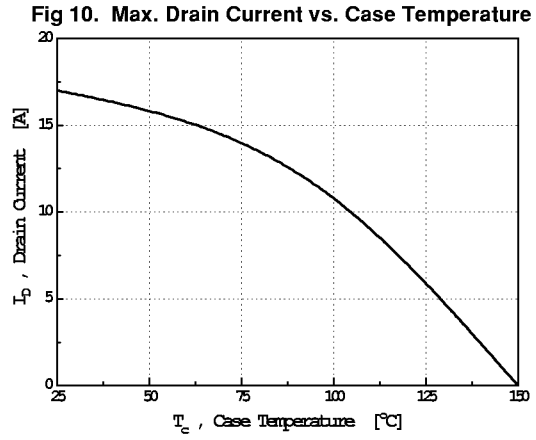
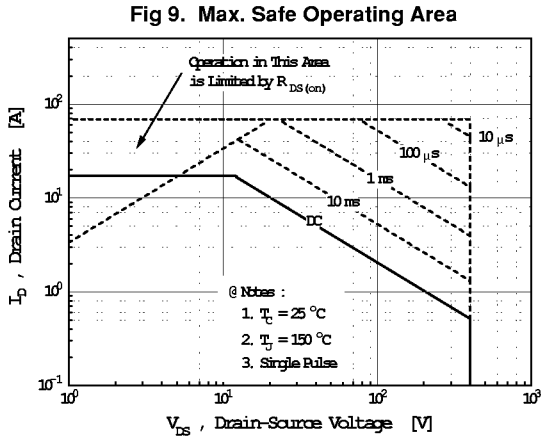
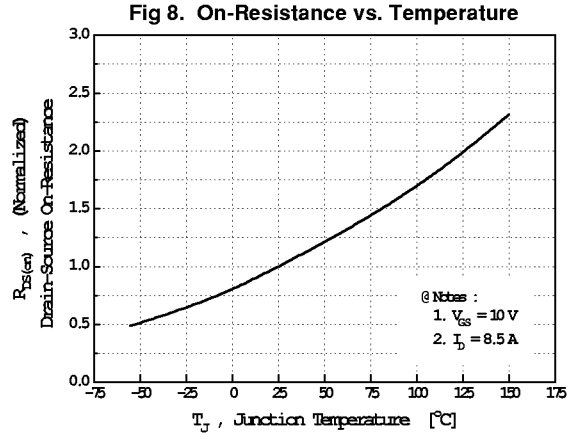
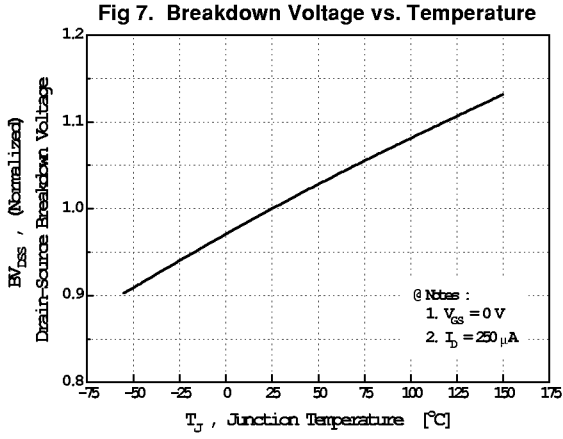
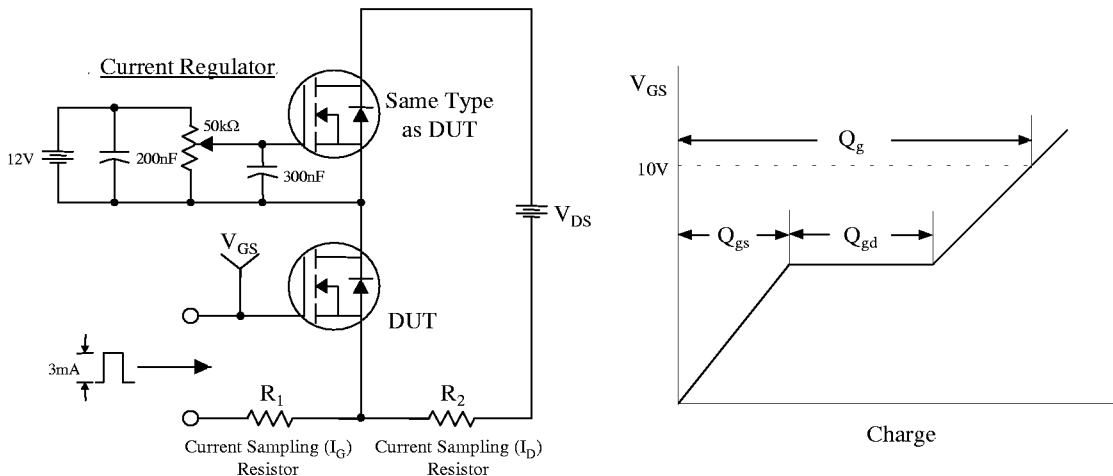


Fig 6. Gate Charge vs. Gate-Source Voltage

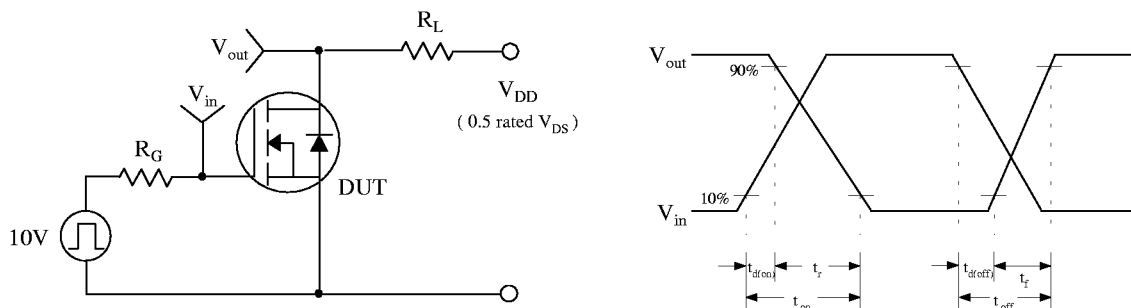




**Fig 12. Gate Charge Test Circuit & Waveform**



**Fig 13. Resistive Switching Test Circuit & Waveforms**



**Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms**

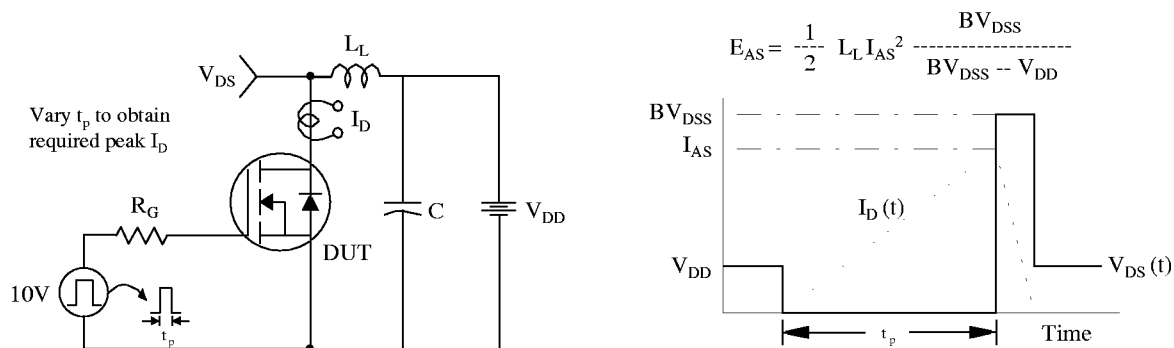
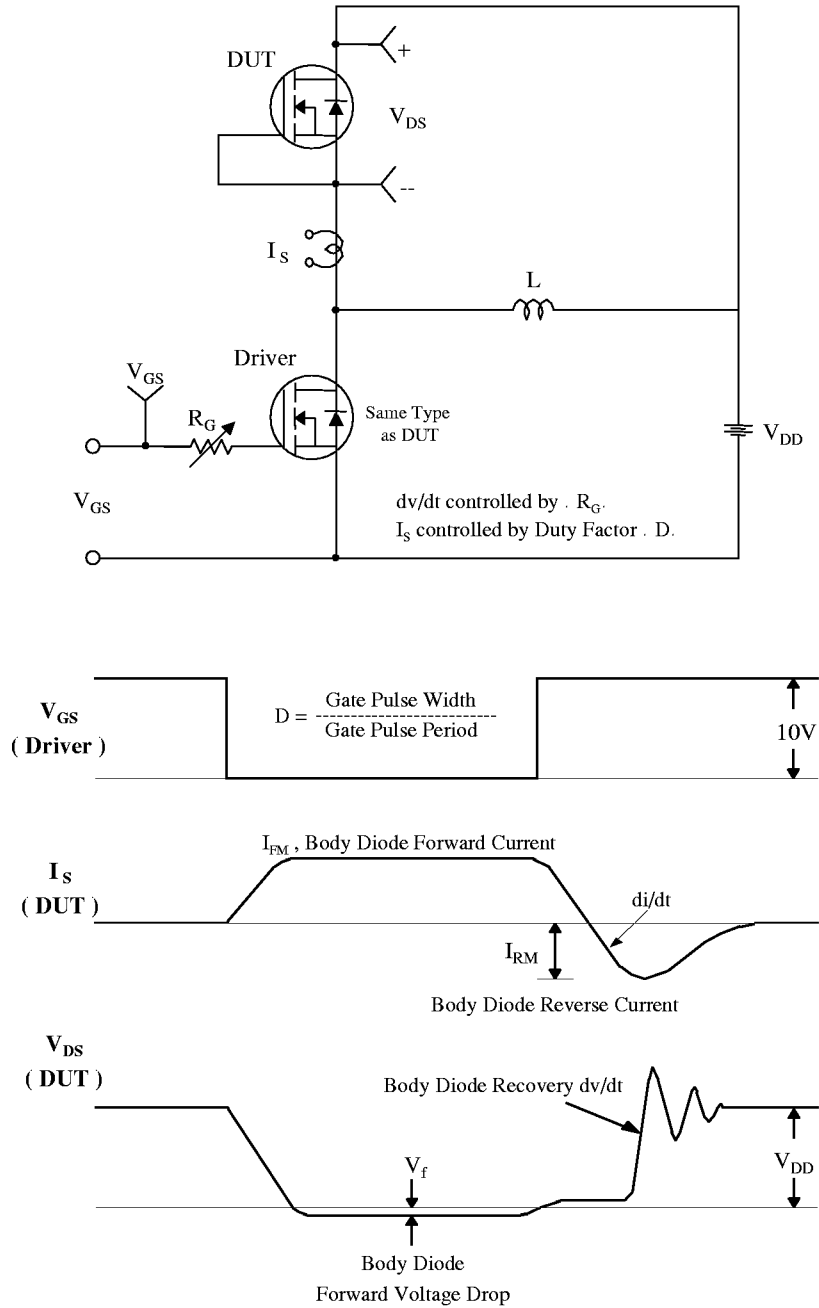


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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