βt866/867

YCrCb to NTSC/PAL Digital Video Encoder with Overlays

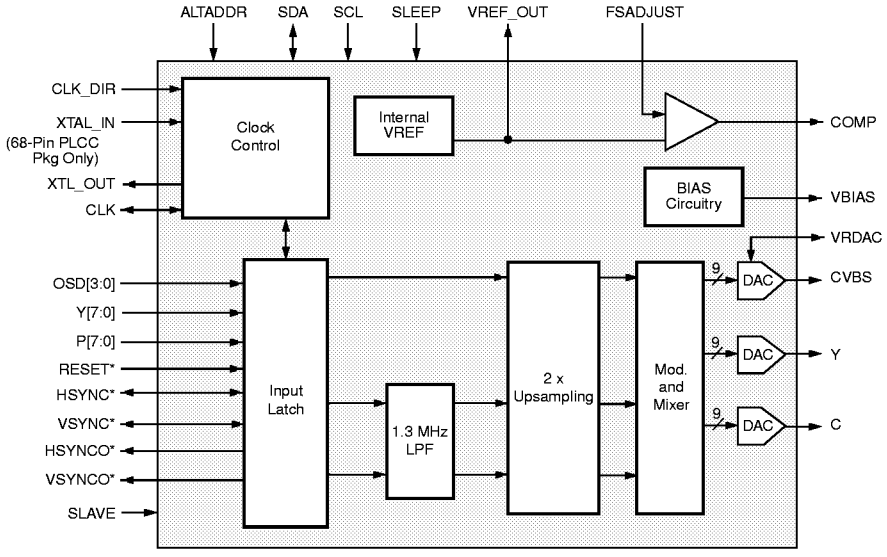
The βt866/867 is designed specifically for video systems requiring the generation of composite or Y/C (S-Video) signals from an 8-bit or 16-bit YCrCb digital video stream. Worldwide video standards are supported, including NTSC (North America and Japan), PAL-β, D, G, H, I (Europe, Asia), PAL-M (βrazil), PAL-N (Uruguay, Paraguay), and PAL-N_c (Argentina). The βt866 and βt867 are functionally identical, except the βt867 can output Macrovision level 6.x anticopy algorithm.

Horizontal Sync (HSYNC*) and Vertical Sync (VSYNC*) can be configured as inputs (slave mode) or outputs (master mode). HSYNCO* and VSYNCO* are dedicated outputs which can be programmed to simplify system interface. The device is configured with a single 2x clock. The rise and fall times of sync, burst envelope, and closed caption data are internally controlled.

An on-board 15-color, 24-bit lookup table provides graphics support for use with On-Screen Displays (OSDs). In addition, an optional test mode cycles through the last upper OSD colors for creation of custom test patterns.

Analog luminance (Y) and chrominance (C) information is available on the Y and C outputs for interfacing to S-Video equipment. The composite analog video signal is output simultaneously onto the CVβS output.

Functional βlock Diagram



Distinguishing Features

- 8-bit or 16-bit 4:2:2 YCrCb inputs
- NTSC/PAL, PAL–M, PAL–N_c (Argentina) composite video outputs
- Simultaneous CVβS and S-Video outputs
- CCIR 601 or square pixel operation
- 60 Hz operation for M-systems
- 15-color 24-bit overlay with optional 8-segment test mode
- 2x oversampling
- 9-bit DACs
- Master or slave video timing
- Interlaced and noninterlaced operation
- Macrovision 6.x support (βt867 only)
- Closed Caption encoding
- I^2C interface with two slave addresses
- On-board voltage reference
- Two power-down modes
- 52-pin MQFP and 68-pin PLCC packages
- βuilt-in crystal oscillator ports (68-pin PLCC only)

Applications

- Digital Satellite Set Top βox(DVβ/DSS/DβS)
- Digital cable television receiving (DβS)
- Digital VCR (DVC/DVHS)
- Video CD
- Digital cameras
- Video conferencing systems

Related Products

- βt852
- βt856/857
- βt864A/865A
- βt868/869

Rockwell
Semiconductor Systems

Ordering Information

Model Number	RSS Part Number	Package	Ambient Temperature Range
Bt866KPF(1)	25866-11	52-Pin Metric Quad Flatpack (MQFP)	0° to +70°C
Bt866KPF(2)	25866-13	52-Pin Metric Quad Flatpack (MQFP)	0° to +70°C
Bt867KPF	25867-11	52-Pin Metric Quad Flatpack (MQFP)	0° to +70°C
Bt866KPJ	25866-12	68-Pin Plastic Leaded Chip Carrier (PLCC)	0° to +70°C
Bt867KPJ	25867-12	68-Pin Plastic Leaded Chip Carrier (PLCC)	0° to +70°C

Notes: (1) Package effective until date code 9749.
(2) Package effective beginning date code 9827.

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1.0 Circuit Description

1.1 Pin Descriptions

Table 1-1 describes each Bt866/867 pin and its function. Pinout diagrams of each package are provided in Figures 1-1 and 1-2. Figure 1-3 depicts a functional block diagram.

Table 1-1. Pin Descriptions *(1 of 3)*

Pin Name	I/O	68 PLCC Pin #	52 MQFP Pin #	Description
CLK	I		49	Pixel clock input (TTL compatible). A clock frequency two times the luminance sample rate should be applied (see Table 1-2). Only available on the 52-pin MQFP.
CLK	I/O	38		Pixel clock input/output (TTL compatible). If driven as an input, a clock frequency two times the luminance sample rate should be applied (see Table 1-2). If configured as an output, it generates two times the luma sample frequency. Loading should be limited to one TTL or 1 CMOS load. Only available on the 68-pin PLCC. See "Clock Timing" on page 6 for details.
CLK_DIR	I	36		Clock direction pin (TTL compatible). A logical 1 configures the CLK pin as an input; a logical 0 enables CLK as an output. Only available on the 68-pin PLCC. See "Clock Timing" on page 6 for details.
XTAL_IN, XTAL_OUT	I	41, 40		Crystal input pins. A crystal can be connected directly to XTAL_IN and XTAL_OUT to provide the 2x pixel clock. A TTL version of this clock is output onto the CLK pin if CLK_DIR is a logical 0. Only available on the 68-pin PLCC. See "Clock Timing" on page 6 for details.
RESET*	I	57	11	Reset control input (TTL compatible). Must be a logical 1 for normal operation. A logical 0 for one CLK cycle resets video timing (horizontal, vertical, and subcarrier counters to the start of VSYNC of first field).
VSYNC*	I/O	6	25	Vertical synchronization input/output (TTL compatible). VSYNC* is registered by the rising edge of CLK.
HSYNC*	I/O	7	26	Horizontal synchronization input/output (TTL compatible). HSYNC* is registered by the rising edge of CLK.

Table 1-1. Pin Descriptions *(2 of 3)*

Pin Name	I/O	68 PLCC Pin #	52 MQFP Pin #	Description
VSYNCO*	O	29	41	Field synchronization output or vertical sync output (TTL compatible). VSYNCO* transitions on the rising edge of CLK. VSYNCO* can output vertical sync or a field signal, depending on the setting of the SYNC[1] bit.
HSYNCO*	O	30	42	Horizontal synchronization output (TTL compatible). HSYNCO* transitions on the rising edge of CLK. HSYNCO* can output a pulse which transitions high and low at any specified time during a video line, depending on the setting of the SYNC[0] bit.
Y[7:0]	I	63–66, 2–5	15–18, 21–24	Y pixel inputs (TTL compatible). In 16-bit mode, these pins serve as the luminance pixel inputs, and are registered on the rising edge of every other CLK period. When configured for 8-bit mode, these pins are not used and should be connected to ground. A higher index corresponds to a greater significance. See Figure 1-4.
P[7:0]	I	20–27	33–40	Y, Cb, Cr inputs (TTL compatible). In 16-bit mode, these pins serve as the Cb and Cr inputs. In 8 bit mode, they serve as inputs for multiplexed Y, Cb, and Cr data. These signals are registered on the rising edge of CLK. A higher index corresponds to a greater significance. See Figure 1-4.
OSD[3:0]	I	31–34	43–46	Overlay pins (TTL compatible). The OSD[3:0] inputs are registered on the rising edge of CLK when Y pixels are normally valid.
SLAVE	I	14	29	Timing mode input (TTL compatible). SLAVE is registered by the rising edge of CLK. A logical 1 configures the device to accept synchronization signals on the HSYNC* and VSYNC* pins (slave mode); a logical 0 allows the device to output synchronization signals on these pins (master mode).
SLEEP	I	16	30	Powerdown control input (TTL compatible). A logical 1 configures the device for power-down mode. A logical 0 configures the device for normal operation. This pin can be connected directly to VAA or GND. Do not assert this pin on powerup.
SDA	I/O	60	13	I^2C serial data line (TTL compatible).
SCL	I	59	12	I^2C serial clock line (TTL compatible). Maximum clock rate is 100 kHz.
ALTADDR	I	61	14	Alternative I^2C address input (TTL compatible). A logical 1 configures the device to respond to an address of 0x8A; a logical 0 configures the device to respond to an I^2C address of 0x88.
CVβS	O	53	8	Composite video output.
C	O	49	4	Modulated chrominance output.
Y	O	51	6	Luminance output.
FSADJUST		46	1	Full-scale adjust control pin. A resistor (RSET) connected between this pin and GND controls the full-scale output current on the analog video outputs. For standard operation, use the nominal RSET values shown under Table 4-2, “Recommended Operating Conditions,” on page 53.

Table 1-1. Pin Descriptions *(3 of 3)*

Pin Name	I/O	68 PLCC Pin #	52 MQFP Pin #	Description
VβIAS			10	DAC bias voltage. A 0.1 µF ceramic capacitor must be used to bypass this pin to AGND. The capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Only available on the 52-pin MQFP.
VRDAC	I	55		Voltage reference input. VRDAC must be connected directly to VREF_OUT. A 0.1 µF ceramic capacitor must be used to decouple this input to GND, as shown in Figure 3-2 in the PC βoard Considerations section. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Only available on the 68-pin PLCC.
VREF_OUT	O	54	9	Voltage reference output. This pin should be used only to drive the VRDAC pin. (See Figure 3-2.) For the 52-pin MQFP, this pin is internally connected to VRDAC and must be decoupled in the same manner as VRDAC.
COMP		47	2	Compensation pin. A 0.1 µF ceramic capacitor must be used to bypass this pin to VAA. The capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VAA		48, 50	3, 5	Analog power. Refer to PC βoard Considerations section of this document.
AGND		12, 13, 42–44, 52	7, 27, 28, 50–52	Analog ground. Refer to PC βoard Considerations section of this document.
VDD		17, 37, 67	19, 31, 48	Digital power. Refer to PC βoard Considerations section of this document.
GND		1, 19, 35	20, 32, 47	Digital ground. Refer to PC βoard Considerations section of this document.

Figure 1-1. βt866/867 68-Pin PLCC Pinout Diagram

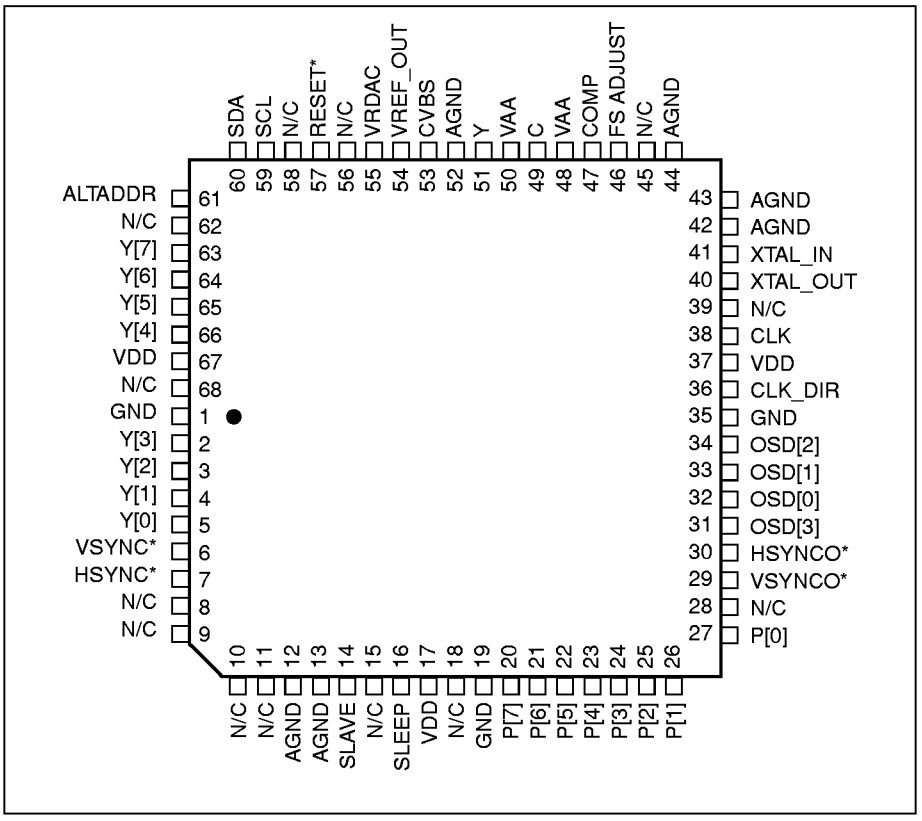


Figure 1-2. βt866/867 52-Pin MQFP Pinout Diagram

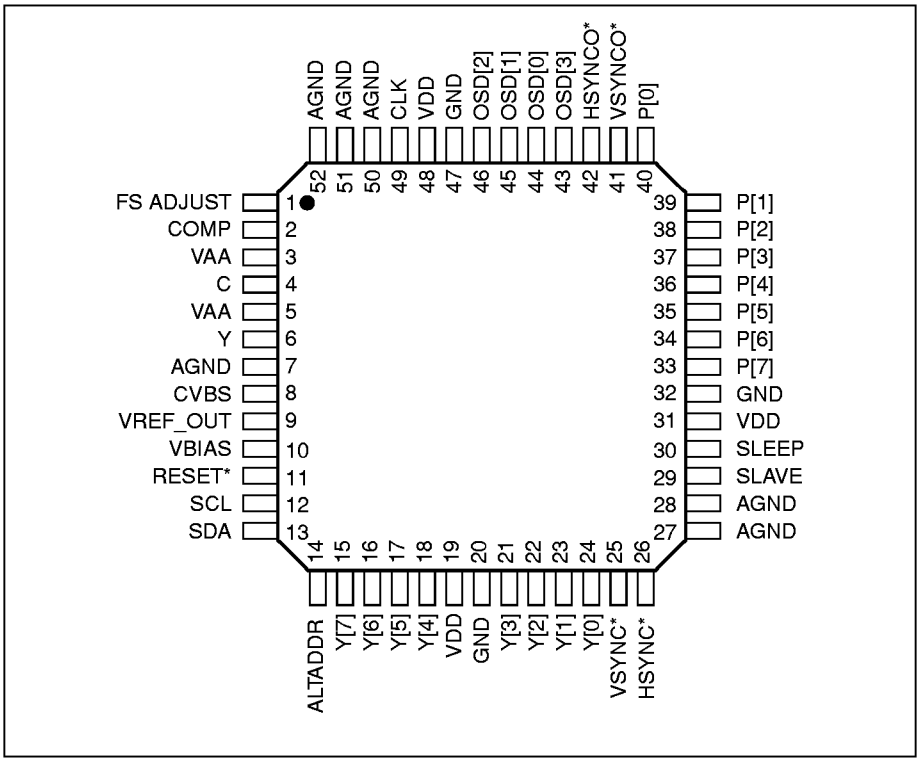
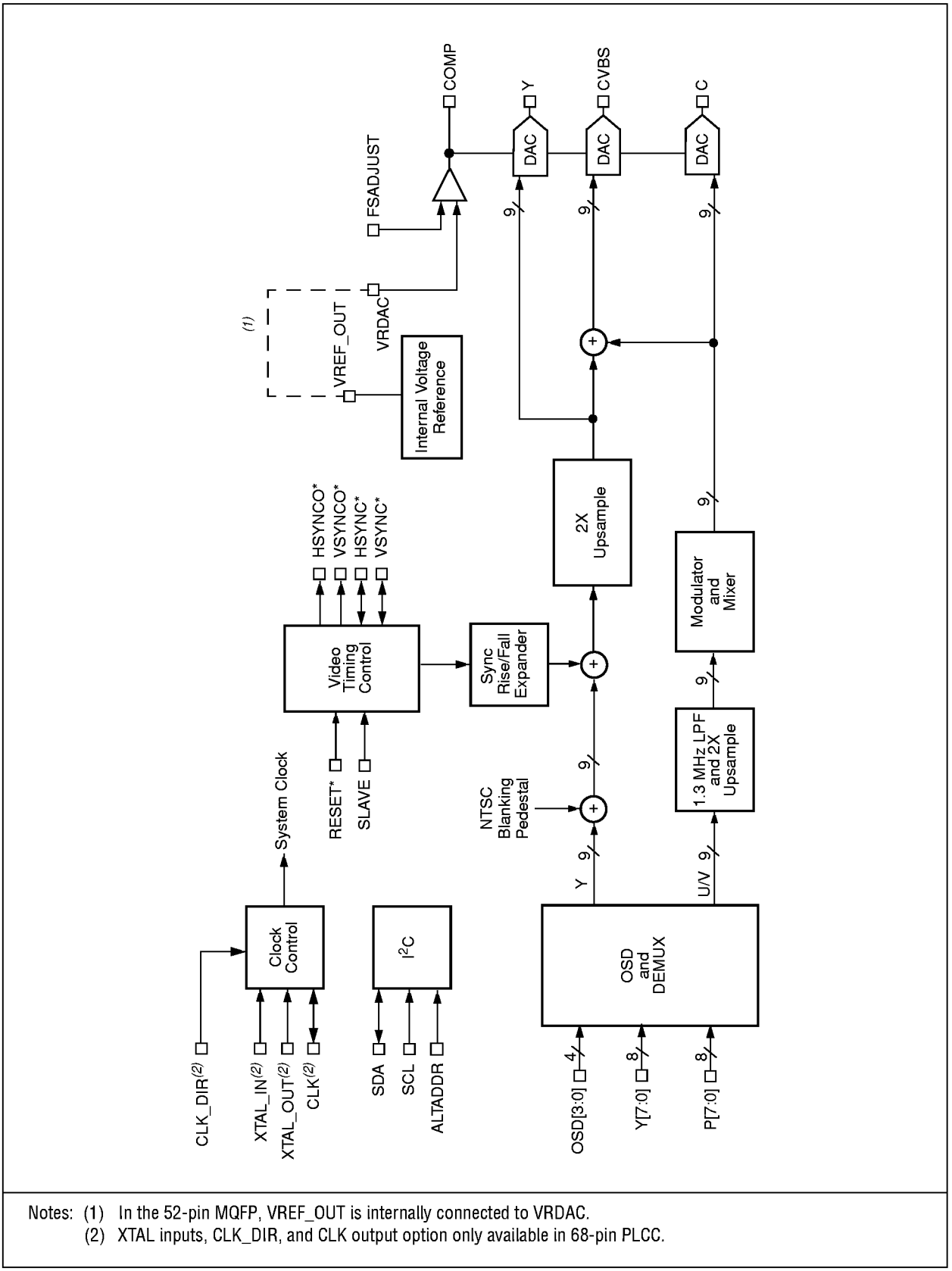


Figure 1-3. Detailed βlock Diagram



Notes: (1) In the 52-pin MQFP, VREF_OUT is internally connected to VRDAC.
(2) XTAL inputs, CLK_DIR, and CLK output option only available in 68-pin PLCC.

1.2 Clock Timing

In the 52-pin MQFP, a clock signal of twice the pixel rate must be supplied to the CLK pin. In the 68-pin PLCC, however, either the CLK input or XTAL inputs can be used. When the CLK_DIR pin is set high, the CLK is an input and the XTAL inputs are not used. If not used, XTAL_IN should be grounded, and XTAL_OUT should be left floating. If CLK_DIR is set low, then the XTAL inputs are used as the clock source, and a TTL version of the crystal clock is available as an output on CLK.

The device generates an internal pixel counter which is synchronized to the HSYNC* signal. This clock signal increments the horizontal and vertical counters to latch the pixel and VSYNC* inputs. All setup and hold timing specifications are measured with respect to the rising edge of the CLK signal.

1.3 Pixel Input Timing

1.3.1 8-βit YCrCb Input Mode

The 8-bit YCrCb multiplexed input mode is selected by default. Multiplexed Y, Cb, and Cr data is input through the P[7:0] inputs. Unused inputs should be grounded. The default input-pixel sequence for active video is Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3, etc., in accordance with CCIR 656. See Figure 1-4.

1.3.2 16-βit YCrCb Input Mode

The 16-bit mode is selected by asserting the YC16 bit in register 0xCC. Y[7:0] data is input via the Y[7:0] inputs; multiplexed Cb[7:0] and Cr[7:0] data is input via the P[7:0] inputs. See Figure 1-4.

1.3.3 Pixel Synchronization

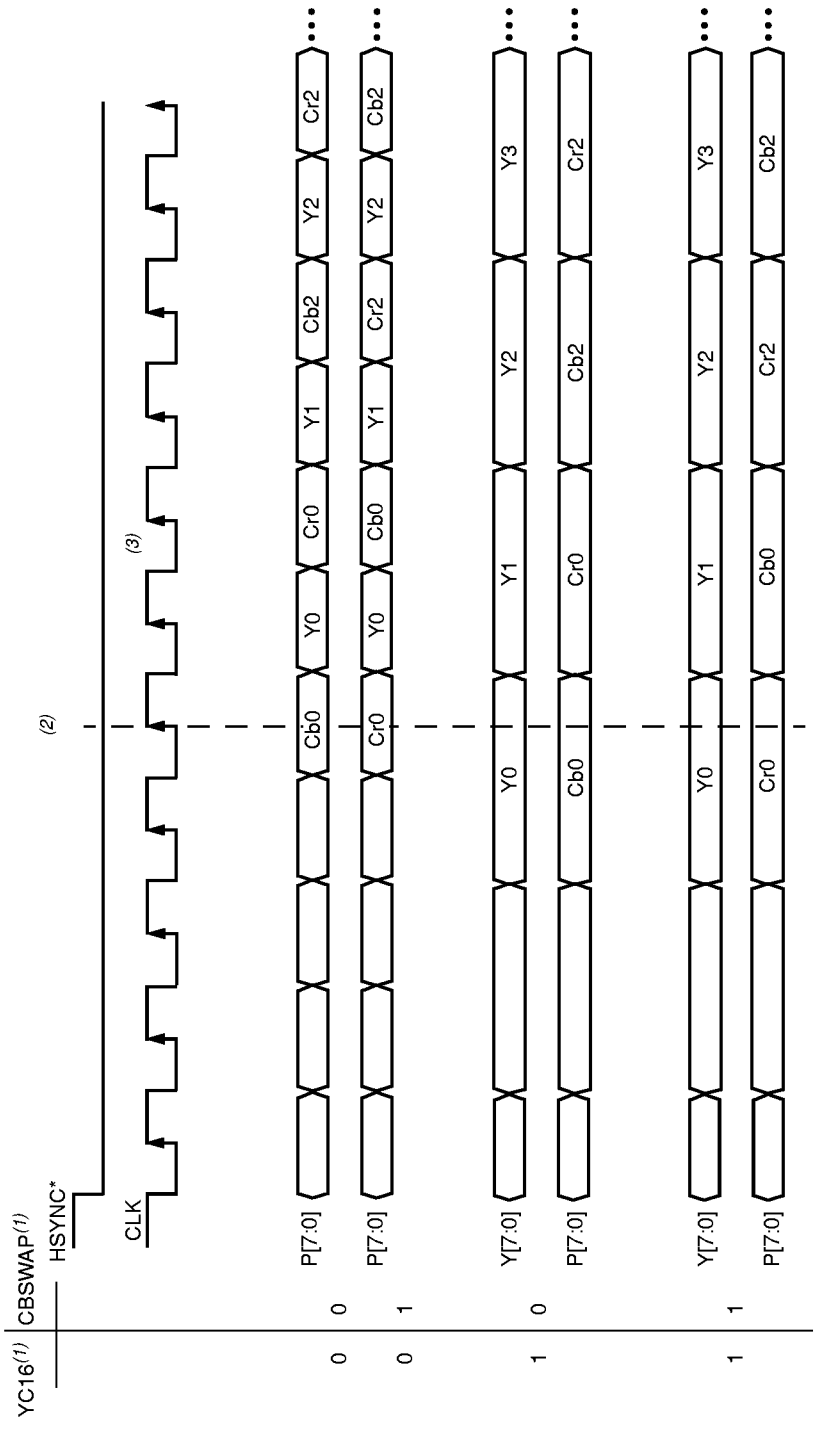
In 8-bit mode after HSYNC* goes low, the first pixel following CLK will be the start of the 4-byte Cb/Y/Cr/Y sequence. In 16-bit mode after HSYNC* goes low, the first pixel following CLK will be the Y/Cb sample pair. See Figure 1-4.

The CBSWAP bit will switch the Cb/Cr order; i.e., Cr will be first. The relationship between the HSYNC* signal and the analog output is unaffected, as is the pixel to analog out timing.

In slave mode, the pipeline delay from HSYNC* to analog sync out is 50 CLK cycles if SYNCDLY = 0, and 49 CLK cycles if SYNCDLY = 1. In master mode, the pipeline delay for HSYNC* is 42 CLK cycles if SYNCDLY = 0, and 43 CLK cycles if SYNCDLY = 1.

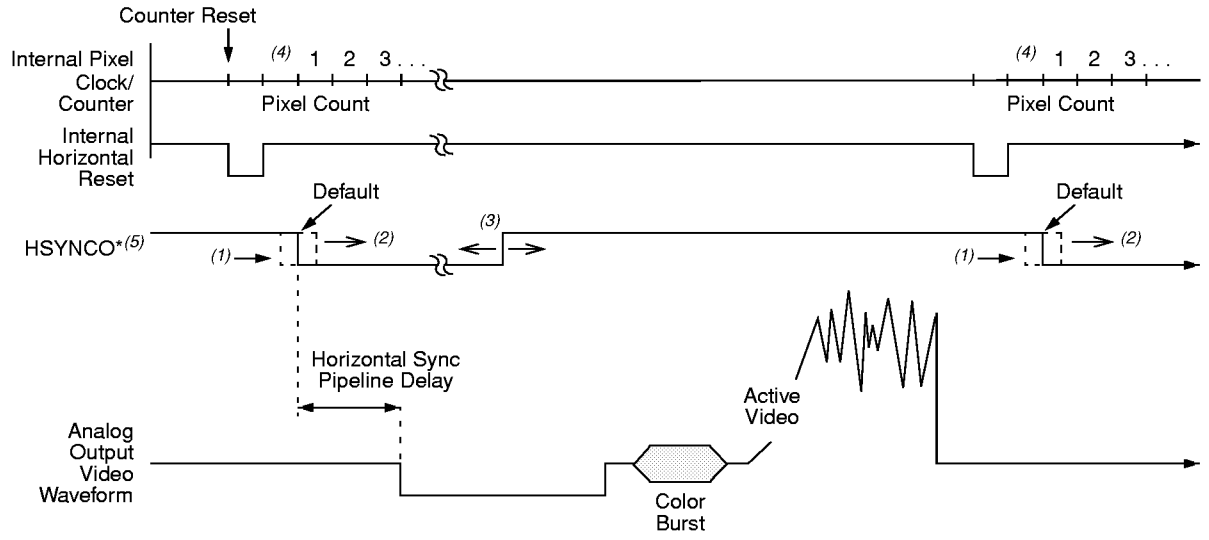
In master mode, the default HSYNCO* timing is identical to the HSYNC* timing regardless of the SYNCDLY value. In slave mode, there is an 8 CLK delay from the falling edge of HSYNC* to the falling edge of HSYNCO* if SYNCDLY = 0 (default), and a 6 CLK delay from the falling edge of HSYNC* to the falling edge of HSYNCO* setting if SYNCDLY = 1. The pipeline delay from pixel input to analog output is 49 CLK cycles. See Figure 1-5. The width of the HSYNCO* pulse is fixed.

Figure 1-4. Pixel Sequence and Timing



Notes: (1) YC16 and CBSWAP are programmable register bits.
(2) Pixel transitions must observe proper set-up and hold timing, relative to the rising edge of CLK.
(3) The first component of the pixel sequence (default = Cb0) must occur 4N+1 rising CLK edges after the falling edge of HSYNC*, where N is an integer.

Figure 1-5. HSYNCO* Timing in Master Mode



Notes: (1) SYNCDLY will change the position of the falling edge of HSYNC* (and HSYNCO*) by 1 CLK period.
(2) Falling edge of HSYNCO* is definable in variable HSYNCO* timing mode, using the register HSYNCF[9:0] and bit SYNC[0].
(3) Rising edge of HSYNCO* is definable in variable HSYNCO* timing mode, using the register HSYNCR[9:0] and bit SYNC[0].
(4) Maximum horizontal resolution (see Table 1-2).
(5) In master mode, HSYNC* and default HSYNCO* are identical.
6. Waveforms not to scale.

1.4 Video Timing

The width of the analog horizontal sync pulses and the start and end of color burst are automatically calculated and inserted for each mode according to CCIR 624-4. Color burst is disabled on appropriate scan lines. Serration and equalization pulses are generated on appropriate scan lines. In addition, rise and fall times of sync, Closed Caption data transitions, and the burst envelope are internally controlled. Video timing figures follow the text in this section. Figures 1-6 through 1-12 show the timing characteristics for various Bt866/867 operating modes.

Figure 1-6. Noninterlaced 262-Line (NTSC) Video Timing (EVβI = 0)

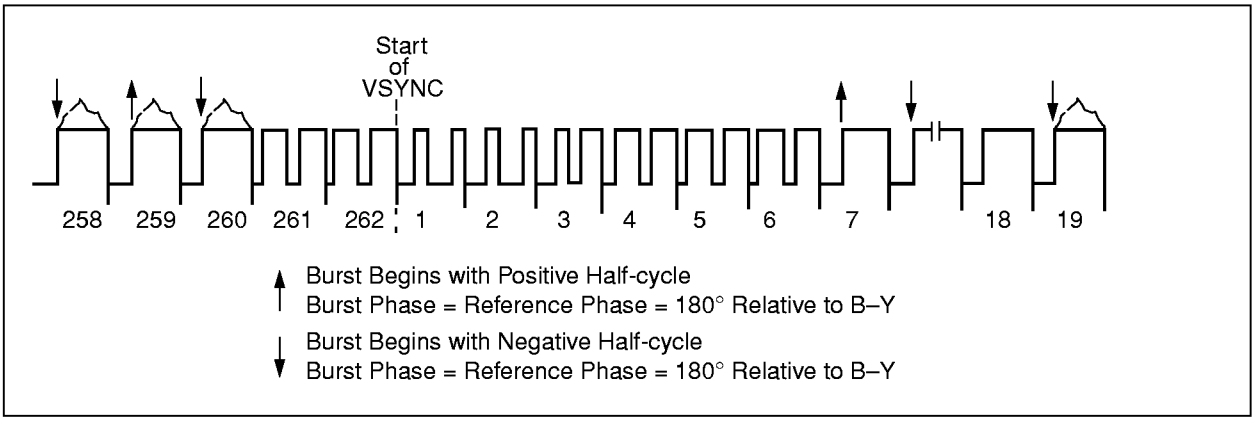
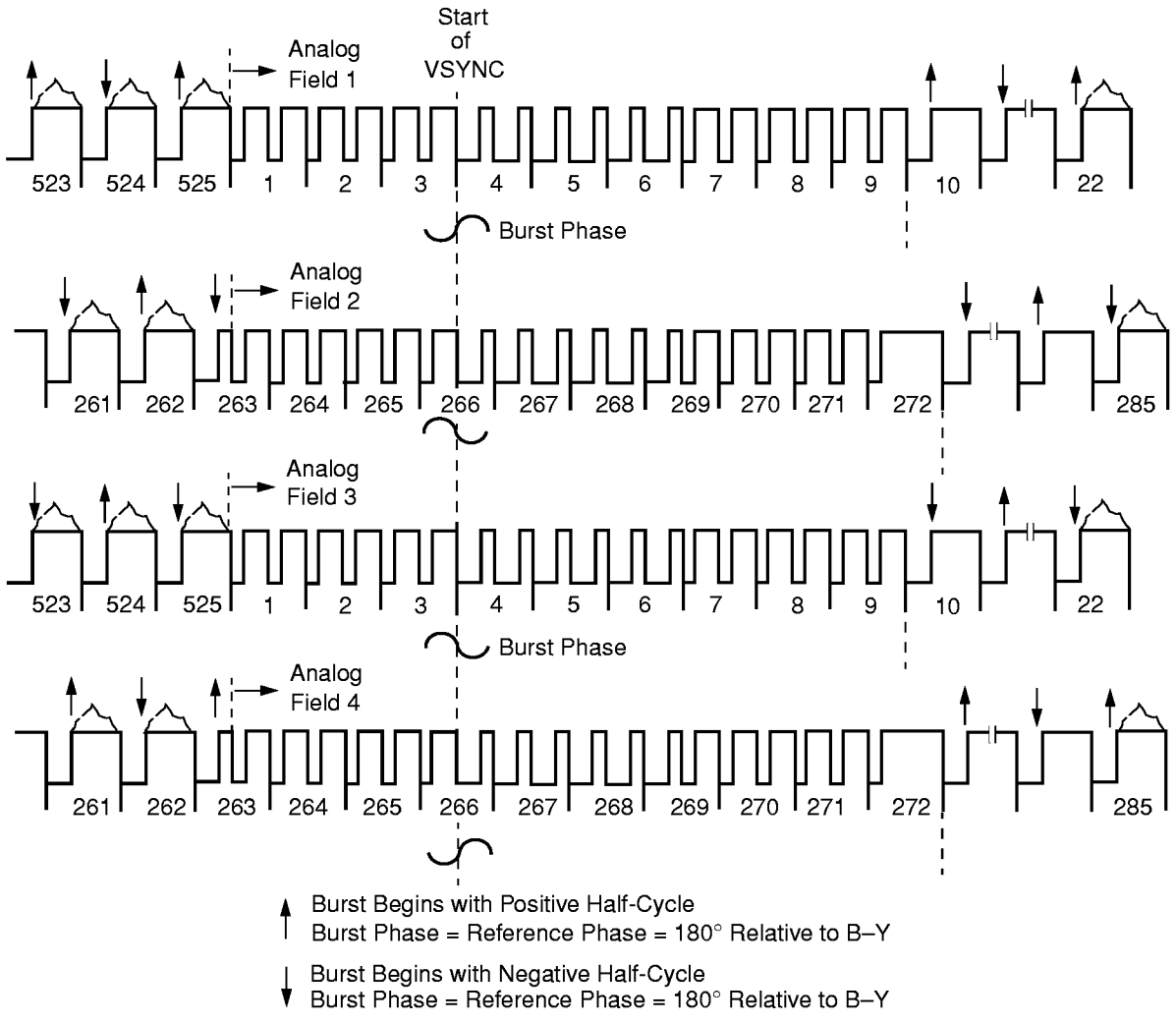
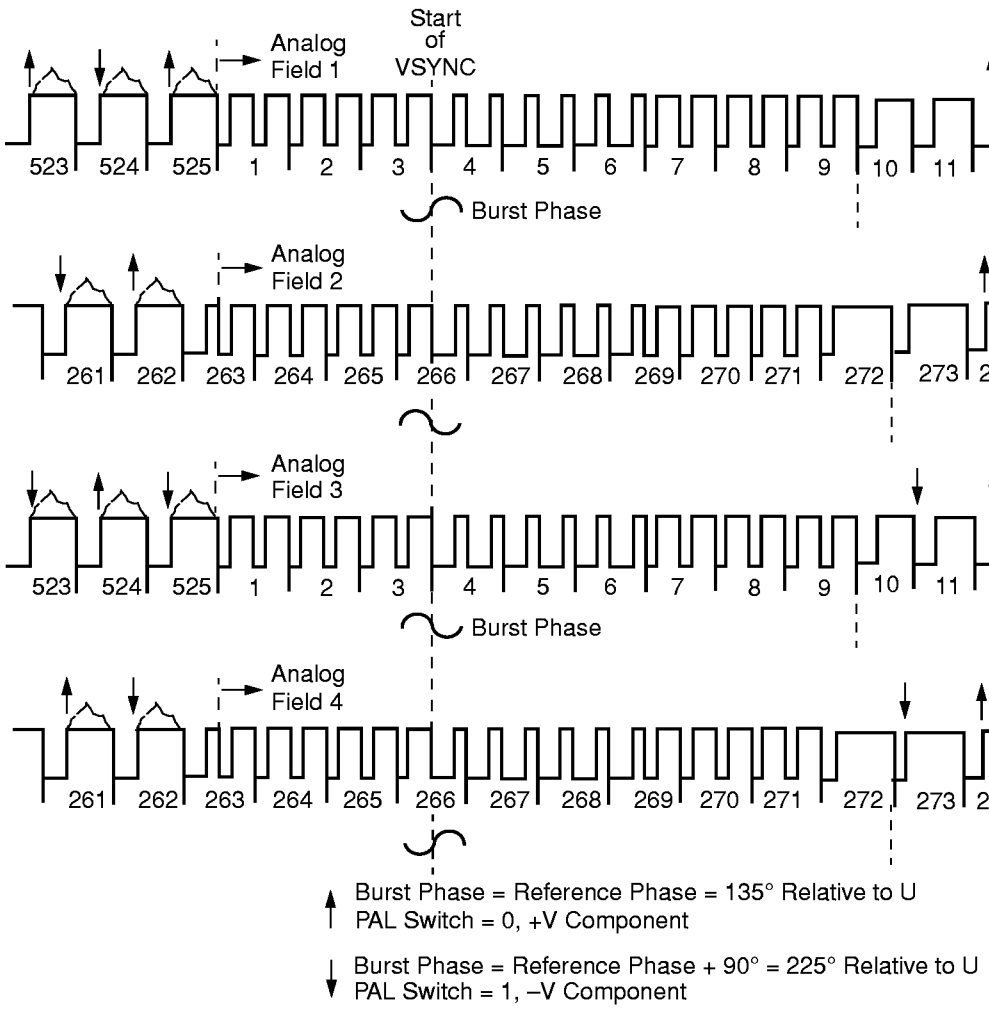


Figure 1-7. Interlaced 525-Line (NTSC) Video Timing (EVβI = 0)



Notes: 1. SMPTE line numbering convention is used rather than CCIR 624.
2. SC-H phasing not maintained for 60 Hz modes since SCRESET must be 1 (see Table 2-5).

Figure 1-8. Interlaced 525-Line (PAL-M) Video Timing (EVBI = 0)



Note: SMPTE line numbering convention is used.

Figure 1-9. Noninterlaced 262-Line (PAL-M) Video Timing (EVβI = 0)

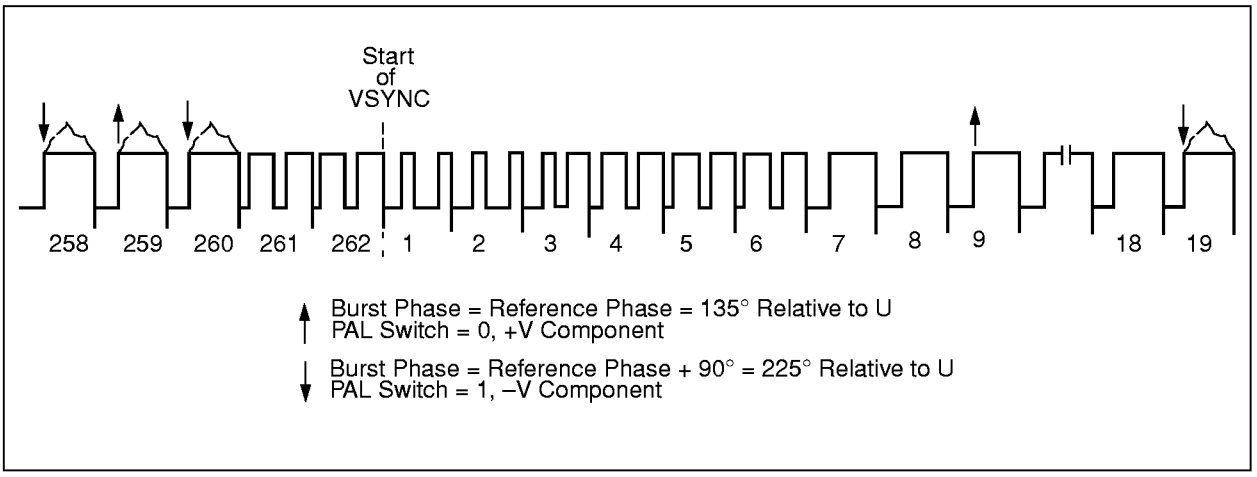


Figure 1-10. Noninterlaced 312-Line (PAL-β, D, G, H, I, N, N_c) Video Timing (EVβI = 0)

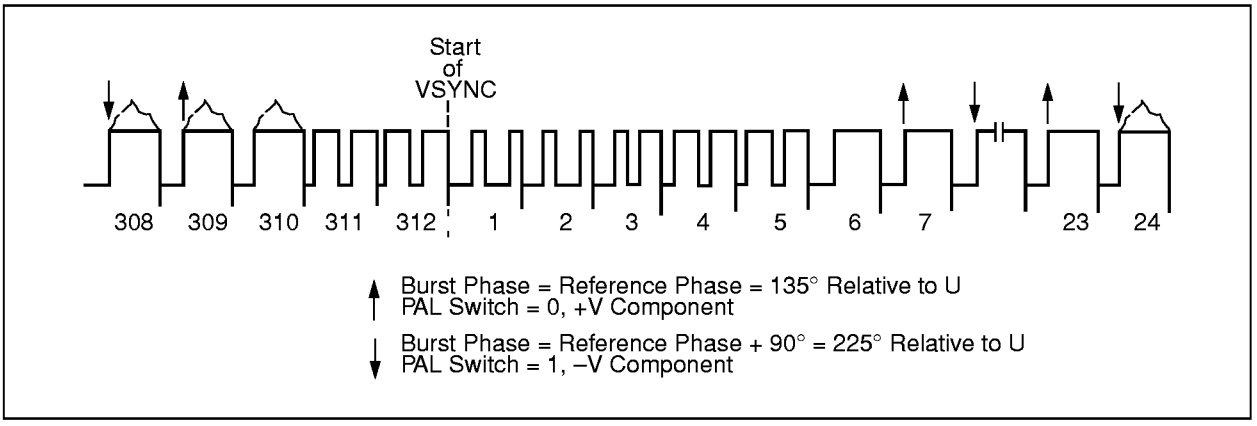


Figure 1-11. Interlaced 625-Line (PAL-β, D, G, H, I, N, N_c) Video Timing (Field 1–4)

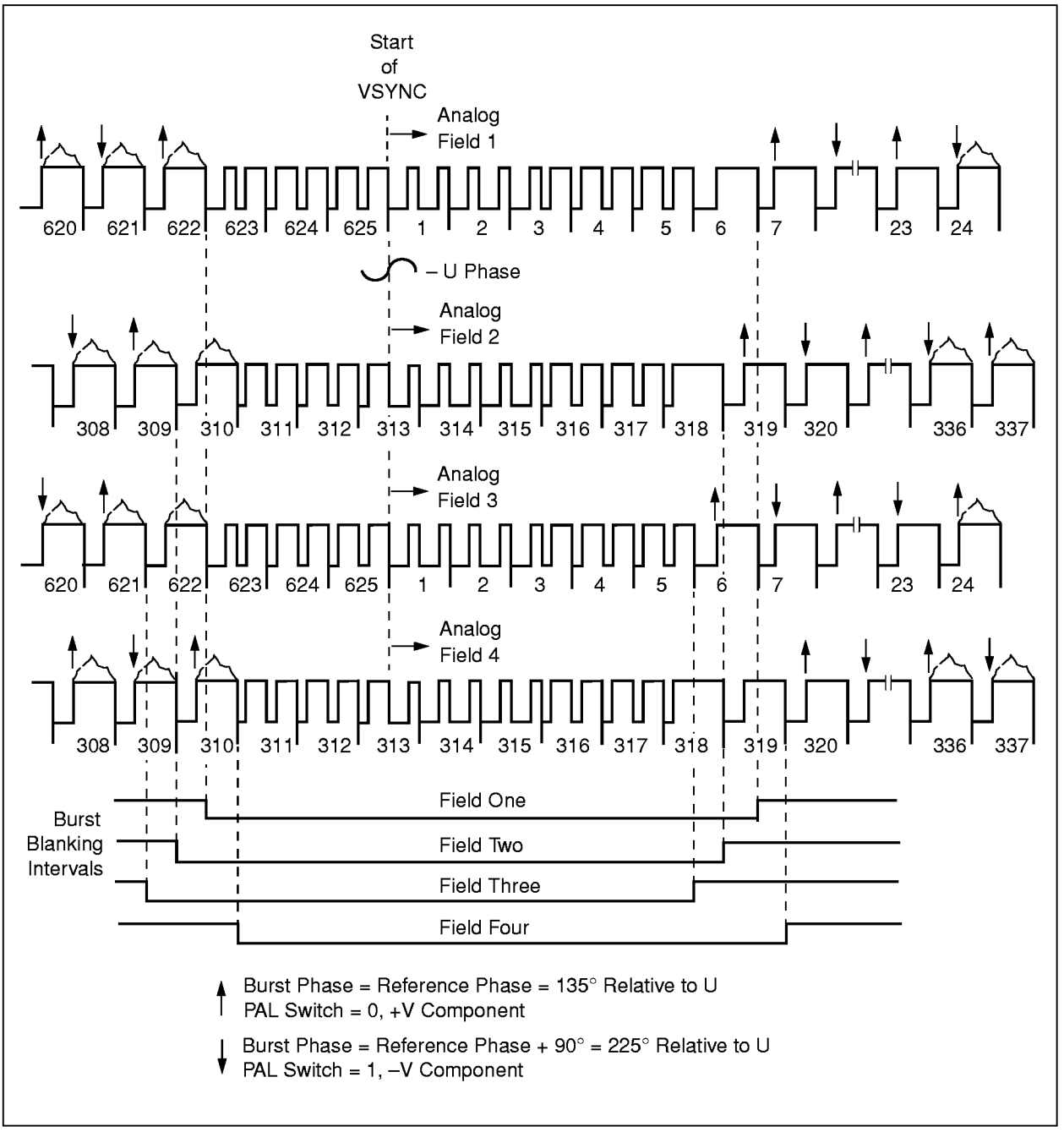
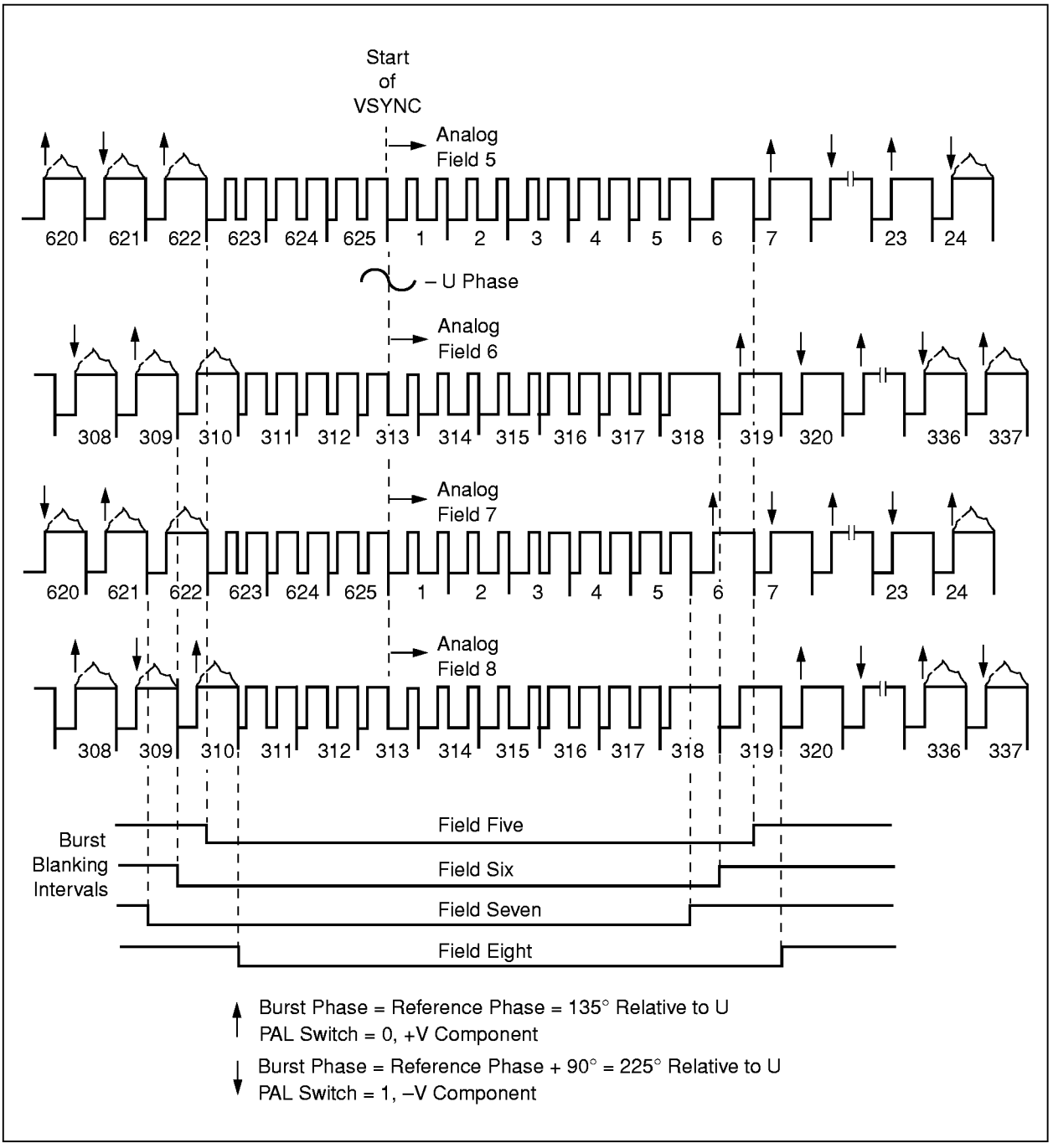


Figure 1-12. Interlaced 625-Line (PAL-β, D, G, H, I, N, N_c) Video Timing (Field 5–8)



1.4.1 Reset

A hardware reset must be asserted immediately after power-up to ensure proper operation. If the RESET* pin is held low during a single rising edge of CLK, the subcarrier phase is reset, and the horizontal and vertical counters are held to the first pixel and second line of FIELD1. Counting resumes on the first rising edge of CLK after rising RESET*; a software reset will occur immediately after writing a 1 to register bit SRESET. This will reset all software-programmable register bits to zero.

The software reset state has the following configuration: interlaced, NTSC CCIR 601 black burst (no active video), and zero chroma scaling. Setting register EACTIVE will enable active video.

1.4.2 Variable HSYNCO* Time Mode

HSYNCO* has two timing modes in master mode: default mode and variable HSYNCO* timing mode.

The variable HSYNCO* timing mode is enabled by setting SYNC[0] high. This mode allows the user to specify the placement of the falling and rising edges of HSYNCO* by using the HSYNCF and HSYNCR registers, respectively.

The values of registers HSYNCF and HSYNCR correspond to the pixel count of the internal pixel counter (see Figure 1-5). HSYNCF and HSYNCR cannot be zero and cannot be equal. Values must also be less than or equal to the total horizontal resolution given in Table 1-2.

If the internal pixel counter resets before the rising edge occurs, the part will not automatically reset, but will wait until the pixel counter reaches the specified HSYNCR value.

The placement of the analog sync pulse is fixed relative to the internal pixel counter. This means that the rising and falling edges of HSYNCO* are moved, and the pipeline delay between the HSYNCO* pulse and the analog horizontal sync pulse is altered.

In master mode, HSYNC* is fixed, except it can be given a 1-clock cycle delay by setting SYNCDLY = 1. It does not change when HSYNCO* is altered using SYNC[0].

Table 1-2. Field Resolutions and Clock Rates for Various Modes of Operation

Operating Mode	Active Field Resolution				Total Field Resolution		Luminance Sample Frequency (MHz)
	Horizontal (Pixels)		Vertical (Lines)		Horizontal (Pixels)	Vertical (Lines)	
	Porch = 0	Porch = 1	EVβI = 0	EVβI = 1			
NTSC/PAL-M CCIR 601	715	720	241	253	858	262	13.5000
PAL-β, D, G, H, I, N, N_c CCIR 601	711	720	287	304/305	864	312	13.5000
NTSC/PAL-M Square Pixel	647	645	241	253	780	262	12.2727
PAL-β, D, G, H, I, N, N_c Square Pixel	767	767	287	304/305	944	312	14.7500

1.4.3 HSYNCO* and VSYNCO* Output Pins

In either slave or master timing mode, HSYNCO* and VSYNCO* are always available as synchronization outputs. HSYNCO* normally outputs a 4.7 µs pulse, exactly like HSYNC* in master mode.

To offer a glueless interface to certain MPEG decoders, HSYNCO* can be used as a programmable composite blanking signal by setting the start and end times to specify the active pixel region. To help accomplish this, register SYNC[2] will disable the falling edge of HSYNCO* during the vertical blanking interval. This bit also inverts the field signal on VSYNCO* (if the field signal is enabled).

The VSYNCO* pin will default to a field signal after software reset (SYNC[2:0] = 000). The VSYNCO* pin in this configuration will transition to low two CLK periods following the coincident falling edges of HSYNC* and VSYNC*, denoting the beginning of Field 1. The VSYNCO* signal will transition to high two CLK periods following the falling VSYNC* edge at the beginning of Field 2. The polarity of the field signal on VSYNC* can be inverted by setting SYNC[2:0] = 10x.

VSYNCO* can also be programmed to output a vertical sync pulse by setting register SYNC[1]. The pulse has a duration of 3 lines for NTSC/PAL–M or 2.5 lines for PAL–B, D, G, H, I, N, N_c exactly like VSYNC* in master mode.

1.4.4 Horizontal Timing

Table 1-2 lists the resolutions and clock rates for the various modes of operation. Table 1-3 lists the horizontal counter values for the end of horizontal sync, start of color burst, end of color burst, front porch, back porch, and the first active pixel for the various modes of operation. During active lines, the encoder will automatically blank during the horizontal blanking interval (front porch and back porch). Enabling the PORCH register bit will alter the horizontal blanking interval as expressed in Table 1-3.

The horizontal sync width is measured between the 50% points of the falling and rising edges of horizontal sync. The start of color burst is measured between the 50% point of the falling edge of horizontal sync and the first 50% point of the color burst amplitude (nominally +20 IRE for NTSC/PAL–M and 150 mV for PAL–B, D, G, H, I, N, N_c above the blanking level). The end of color burst is measured between the 50% point of the falling edge of horizontal sync and the last 50% point of the color burst envelope (nominally +20 IRE for NTSC/PAL–M and 150 mV for PAL–B, D, G, H, I, N, N_c above the blanking level).

NOTE: PAL-N_c refers to "Combination N," the PAL format used in Argentina.

Table 1-3. Horizontal Counter Values for Various Video Timings

Operating Mode	Horizontal Counter Value Relative to Falling Edge of Horizontal Sync										
	Rising Edge of Horizontal Sync		Start of βurst		End of βurst		βack Porch		Front Porch(1)		PORCH βit
	CNT(4)	µs	CNT	µs	CNT	µs	CNT	µs	CNT	µs(3)	
NTSC CCIR 601	63	4.67	72	5.33	105	7.78	127 123	9.41 9.11	835 843	1.48 1.11	0 1
PAL-M CCIR 601	63	4.67	78	5.78	111	8.22	127 123	9.41 9.11	844 849	1.48 1.11	0 1
NTSC Square	58	4.73	65	5.30	96	7.82	115 117	9.37 9.53	762	1.47	0 1
PAL-M Square	58	4.73	78	6.36	111	9.04	115 117	9.37 9.53	762	1.47	0 1
PAL-β, D, G, H, I, N CCIR 601	63	4.67	76	5.63	106	7.85	142 133	10.52 9.85	844 853	1.48 0.81	0 1
PAL-N_C(2) CCIR 601	63	4.67	76	5.63	111	8.22	142 133	10.52 9.85	844 853	1.48 0.81	0 1
PAL-β, D, G, H, I, N Square	69	4.68	83	5.63	116	7.86	155	10.51	922	1.49	0 1
PAL-N_C (2) Square	69	4.68	83	5.63	111	7.53	155	10.51	922	1.49	0 1

Notes: (1) In Slave mode, Front Porch timing is triggered by the previous HSYNC pulse. Any deviation from nominal line length can affect the front porch duration.
(2) PAL-N_C refers to the PAL format used in Argentina (Combination N).
(3) This value is measured from the blanked video at the end of a line to the midpoint of the Horizontal sync falling edge on the next line.
(4) CNT refers to the number of luminance pixel periods. With respect to the CLK pin, there are twice as many CLK periods as CNT periods. Pixels on porch boundaries occurring on odd counts can have attenuated chrominance.

1.4.5 Master Mode

Horizontal Sync (HSYNC*) and Vertical Sync (VSYNC*) are generated from internal timing and optional software bits. HSYNC*, HSYNCO*, VSYNC*, and VSYNCO* are output following the rising edge of CLK.

The horizontal counter is incremented on every other rising edge of CLK. After reaching the appropriate value determined by the mode of operation, it is reset to one, indicating the start of a new line.

The vertical line counter is incremented at the start of each new line. After reaching the appropriate value, determined by the mode of operation, it is reset to one, indicating the start of a new field (interlaced operation) or frame (noninterlaced operation). VSYNC* is asserted for 3 scan lines for 262/525 line video, and is asserted for 2.5 scan lines for 312/625 line video.

HSYNC* falling indicates the beginning of a new scan line. The beginning of Field 1 is indicated by coincident falling edges of VSYNC* and HSYNC*; the beginning of Field 2 is indicated when VSYNC* falls in the middle of two falling edges of HSYNC*.

1.4.6 Slave Mode

The Horizontal Sync (HSYNC*) and Vertical Sync (VSYNC*) inputs are registered on the rising edge of CLK. The horizontal pixel counter is incremented on the rising edge of CLK. Two CLK cycles after a falling edge of HSYNC*, the counter is reset to one, indicating the start of a new line. The vertical line counter is incremented on the falling edge of HSYNC*. A falling edge of VSYNC* resets it to one, indicating the start of a new field (interlaced operation) or frame (noninterlaced operation).

A falling edge of VSYNC* occurring within ±1/4 line of the falling edge of HSYNC* indicates the beginning of Field 1. The next line after a falling transition on VSYNC* will be the first line of the appropriate field. The start of VSYNC* occurs on the falling HSYNC* at the beginning of the next expected Field 1 and halfway between expected falling HSYNC* edges. (Refer to Figures 1-6 through 1-12.)

The operating mode (NTSC/PAL, interlaced/noninterlaced, Square Pixel/CCIR 601) can be programmed with the MODE[4:0] bits when the SETMODE bit is set high. Alternatively, when SETMODE is low, the mode is automatically detected (only available in slave mode). For example, 525-line CCIR 601 NTSC operation is assumed, and 625-line operation is detected by the number of HSYNC* edges between VSYNC* edges. Interlaced operation is detected by observing the sequence of Field 1 or Field 2; if the field timing is repeated, then noninterlaced mode is assumed. The frequency of operation (square pixels or CCIR 601) for both PAL and NTSC is detected by counting the number of clocks per line. The pixel rate is assumed to be 13.5 MHz unless the exact total pixel count for square pixels, ±1 count, is detected in between two successive falling edges of HSYNC* (see Table 1-2).

NOTE: Square pixel 625-line operation with this sequence requires one frame to stabilize.

1.4.7 Burst Blanking

Color burst information is automatically disabled for video modes as follows:

Interlaced NTSC:	On scan lines 1–11 and 263–273 inclusive (SMPTE line numbering convention).
Interlaced PAL-B, D, G, H, I, N, N_c:	On scan lines 1–6, 310–318, and 623–625 inclusive, for fields 1, 2, 5, and 6. During fields 3, 4, 7, and 8: on scan lines 1–5, 311–319, and 622–625 inclusive.
Noninterlaced NTSC:	On scan lines 1–6 and 261–262 inclusive.
Noninterlaced PAL-M:	On scan lines 1–8 and 260–262 inclusive.
Noninterlaced PAL-B, D, G, H, I, N, N_c:	On scan lines 1–6 and 310–312 inclusive.

See Figures 1-6 through 1-12.

1.4.8 Vertical Blanking Intervals

For interlaced NTSC/PAL-M, scan lines 1–9 and 263–272, inclusive, are always blanked. There is no setup on scan lines 10–21 and 273–284, inclusive, allowing the generation of video test signals, timecode, and other information by controlling the pixel inputs appropriately (except for lines controlled by Closed Caption or Macrovision generation). With setup enabled, the sync amplitude in PAL–M is slightly higher than normal for the VBI lines. Without setup enabled, all lines are slightly high.

For interlaced PAL-B, D, G, H, I, N, N_c, scan lines 1–6, 311–318, and 624–625, inclusive, during fields 1, 2, 5, and 6, are always blanked. During fields 3, 4, 7, and 8, scan lines 1–5, 311–319, and 624–625, inclusive, are always blanked. The remaining scan lines during the vertical blanking interval can be used for the generation of video test signals, timecode, and other information by controlling the pixel inputs appropriately.

By default (EVBI = 0), all displayed lines in the vertical blanking interval (10–21 and 273–284 for interlaced NTSC/PAL-M; 7–23 and 320–335 for interlaced PAL-B, D, G, H, I, N, N_c) are forced to blank. It is possible to enable active video during the vertical blanking interval by setting the EVBI bit high (Register 0xDE).

For noninterlaced NTSC/PAL-M, scan lines 1–6, inclusive, are always blanked. For noninterlaced PAL-B, D, G, H, I, N, N_c, scan lines 1–6 and 311–312, inclusive, are always blanked. Other lines in the vertical blanking interval (VBI) will be blanked by default (EVBI = 0), as described for the interlaced condition. In Figure 1-6, line numbering is offset by three from SMPTE conversion used in Figure 1-7.

NOTE: If the EVBI bit is set and Closed Caption encoding is enabled, the pixel data will be passed through the encoder on the Closed Caption line prior to the clock run-in.

1.4.9 Digital Filtering

Once the input data is converted into internal YUV format, the UV components are low-pass filtered with the filter response shown in Figure 1-13 (linearly scalable by CLK frequency). The Y and filtered UV components are upsampled to CLK frequency by a digital filter whose response is shown in Figure 1-14.

Figure 1-13. Internal Three-Stage Chroma Filter

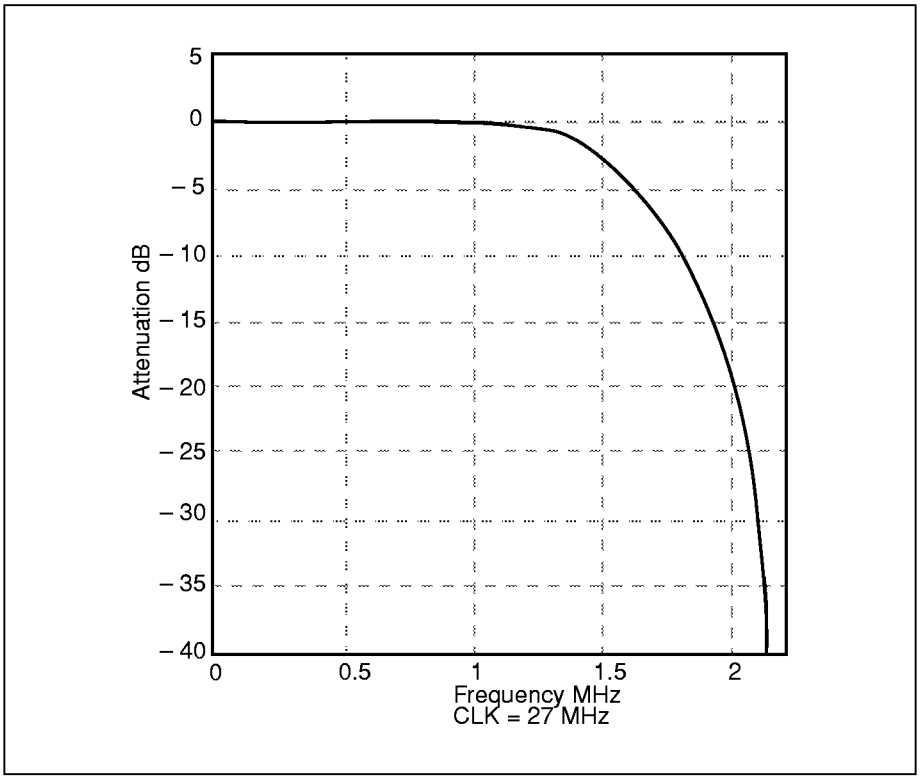
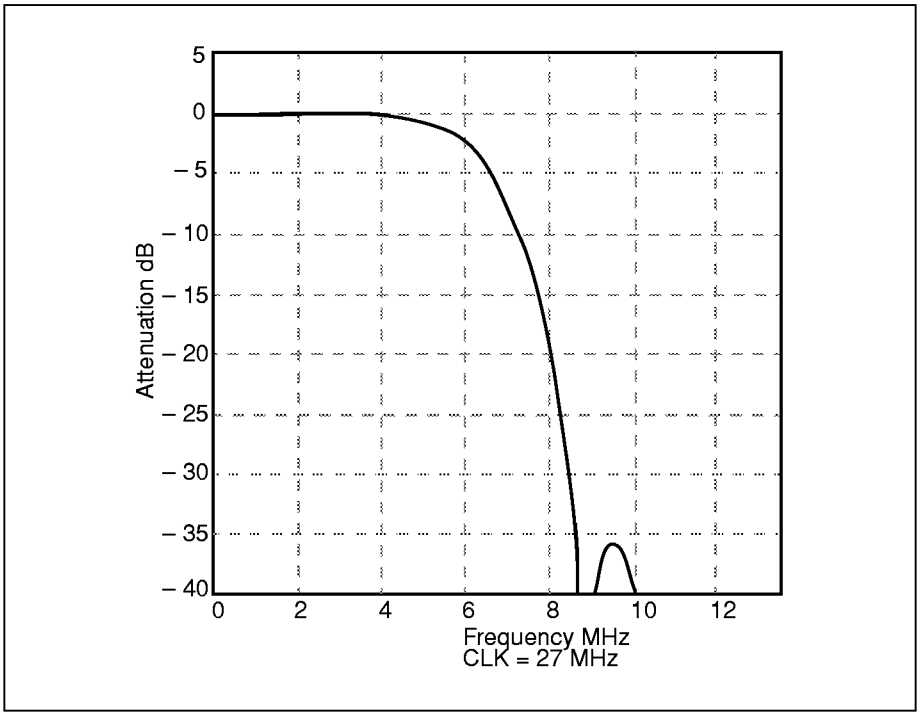


Figure 1-14. Internal 2x Upsampling Filter Response



1.4.10 Chrominance Disable

The chrominance subcarrier can be turned off by setting register DCHROMA to a logical 1. This kills burst as well, providing luminance-only signals on the CVBS outputs and a static blank level on the C output.

1.4.11 Subcarrier Phasing

SC-H phasing is reset on the falling edge of HSYNC* at the beginning of Field 1 (line 4 for NTSC, line 1 for PAL), unless subcarrier reset is disabled through software (register SCRESET). SC-H phase is non-zero and depends upon the clock rate and the video standard chosen.

Setting the SCRESET bit to 1 can be useful in situations where the ratio of CLK/2 to HSYNC* edges in a color frame is non-integer, which could produce a significant phase impulse by resetting to 0.

Subcarrier frequencies are shown in Table 2-5.

1.4.12 Noninterlaced Operation

The device can be operated in noninterlaced mode by setting register bit MODE1 high. When in noninterlaced master mode, the Bt866/867 always displays Field 1, meaning that the falling edges of HSYNC* and VSYNC* will be output coincidentally.

A 30 Hz offset will be added to the color subcarrier frequency while in NTSC mode so that the color subcarrier phase will be inverted from field to field. Subcarrier phase is reset to 0 upon rising RESET* and every four fields for NTSC or eight fields for PAL.

In master mode, transition from interlaced to noninterlaced occurs during Field 1 to prevent synchronization disturbance. In slave mode, transition occurs after a subsequent falling edge of VSYNC*.

NOTE: Consumer VCRs can record noninterlaced video with minor noise artifacts, but special effects (e.g., scan > 2x) may not function properly.

1.4.13 Power-Down Mode

Register states are preserved in power-down mode (SLEEP pin set to 1), but other chip functionality (including I^2C communication) is disabled. This mode should be set when the Bt866/867 could be subjected to clock and data frequencies outside its functional range.

Register bit DACOFF will power-down the DACs when set high. This will result in the analog current being reduced almost to zero. It will have no effect on the digital current.

1.5 Pixel Input Ranges and Colorspace Conversion

1.5.1 YC Inputs (4:2:2 YCrCb)

Chrominance scaling is programmable. Based on the recommended values found in Table 2-3, Y has a nominal range of 16–235; Cb and Cr have a nominal range of 16–240 with 128 equal to zero. Values of 0 and 255 are interpreted as 1 and 254, respectively. Y values of 1–15 and 236–254, and CrCb values of 1–15 and 241–254, are interpreted as valid linear values.

The U and V components are calculated as follows:

U[8:0] = (((CBSCALE[7:0]*(CB[7:0]–0X80))>>6) + 1) >>1
V[8:0] = (((CRSCALE[7:0]*(CR[7:0]–0X80))>>6) + 1) >>1

Register bit SETUP will alter luma scaling (as shown in Figures 1-15 through 1-20) and disable or enable the 7.5 IRE setup. Chroma scaling must be programmed with CRSCALE and CBSCALE registers. When the SETUP bit is enabled, PAL-B, D, G, H, I, N, N_c video can be generated using NTSC/PAL-M blanking levels and 7.5 IRE setup. NTSC/PAL-M pixel scaling is performed (Y range of 16–235 represents 7.5-100 IRE); or NTSC/PAL-M video can be generated using PAL-B, D, G, H, I, N, N_c scaling (Y range of 16–235 represents 0-100 IRE) without the 7.5 IRE setup. With setup disabled, NTSC/PAL-M mode has 2% less black-to-white range than NTSC/PAL-M mode with setup enabled.

1.5.2 OSD and Overlays

Fifteen 24-bit colors can be written through the serial I^2C port. These lookup tables can then be selected on a pixel-by-pixel basis to control graphics overlays. Internally, overlays are inserted before any video processing, including color space conversion, sync insertion, and modulation. Therefore, all essential registers must be programmed to produce graphics or color bars, just as for normal video. Registers OSDY, OSDCR, and OSDCB contain the LUT values for Y, Cr, and Cb.

Two modes of accessibility for the LUTs are available: 8-color and 15-color. The default mode allows access to only 8 colors. In this mode, overlays are enabled only when OSD[3] is high, and are disabled when OSD[3] is low. Pins OSD[2:0] select between 8 different overlay colors, numbered between 8 and 15; an overlay color can be selected during any pixel period. For example, if OSD[2:0] is set to 7, colors OSDY15, OSDCR15 and OSDCB15 will be selected.

The 15-color mode is enabled by setting register bit OSDEXT high. In 15-color mode, any nonzero setting of the OSD[3:0] pins will select an overlay color numbered between 1 and 15. Overlays are disabled (transparent mode) whenever all OSD[3:0] pins are set to zero. For example, if OSD[3:0] is set to 1, colors OSDY1, OSDCR1, and OSDCB1 will be selected.

By default, LUT values for Cr and Cb are 2's complement. Setting register bit OSDNUM high will cause these LUTs to be interpreted as straight binary values.

1.5.3 Internal Color Bars

By setting register bit OSDBAR high, the Bt866/867 can be configured to generate color bars, using the overlay lookup tables.

In this mode, the OSD and data pins are ignored, while the Bt866/867 cycles through colors 8–15. This allows the creation of custom 8-segment color bars, where the width of each color is exactly 1/8th of the active pixel region. Depending on the input data and power supply level, there can be some insertion artifacts in the transition regions between colors. This mode is often useful for diagnostics.

Color bars can also be generated by setting Y[7] = 1, while in 8-bit mode. This method cannot be used in 16-bit mode, and setting OSDBAR high will always enable color bars, regardless of the value of Y[7].

1.6 Closed Captioning

The Bt866/867 encodes Closed Captioning (CC) for NTSC/PAL-M on scan line 21 and Extended Data Services (XDS) on scan line 284. Four 8-bit registers (CCF1B1, CCF1B2, CCF2B1, and CCF2B2) provide the data, while register bits ECCF1 and ECCF2 enable display of the data.

Closed Captioning for PAL-B, D, G, H, I, N, N_c is similar to that for NTSC. Closed Caption encoding is performed for 625-line systems according to the system proposed by the National Captioning Institute; clock and data timing is identical to that of NTSC, except that encoding is provided on lines 22 and 335.

When the ECCGATE bit is set high, encoding is forced to 00 until a new complete pair of data bytes has been written to the CC data registers.

The Bt866/867 generates the clock run-in and appropriate timing automatically. Pixel inputs are ignored during CC encoding. See FCC Code of Federal Regulations (CFR) 47, Section 15.119 (10/91 edition or later), for programming information. EIA608 describes ancillary data applications for Field 2, line 21 (line 284).

NOTE: Register contents are transferred immediately following the clock run-in; therefore, no register modifications should occur during the line being encoded.

1.7 Anticopy Process (βt867 Only)

The anticopy process inside the Bt867 is implemented according to the Macrovision revision 6.1 specification developed by Macrovision Corporation in Sunnyvale, California. All luminance, chrominance, and composite video waveforms include the Macrovision anticopy process. The Macrovision anticopy process technology is protected by U.S. patents and other intellectual property rights. The anticopy process is licensed for non-commercial, home use only. Reverse engineering or disassembly is prohibited.

Rockwell cannot ship Bt867 units to any customer until that customer has obtained a "Macrovision Proprietary Material License Agreement" from Macrovision Corporation. Contact Macrovision Corporation to facilitate this agreement.

1.8 Outputs

All video DACs are designed to drive standard video levels into an equivalent 37.5 Ω load. Unused outputs should be connected directly to ground to minimize supply switching currents. One composite video output plus S-Video (Y/C) outputs are available. If the SLEEP pin is high, the DACs are turned off, and only leakage current is present. The D/A converter values for 100% saturation, 100% amplitude color bars are shown in Figures 1-15 through 1-20.

1.8.1 Luminance (Y) Analog Output

Digital luminance information drives the 9-bit D/A converter that generates the analog Y video output (Figures 1-15 and 1-16 and Tables 1-4 and 1-5).

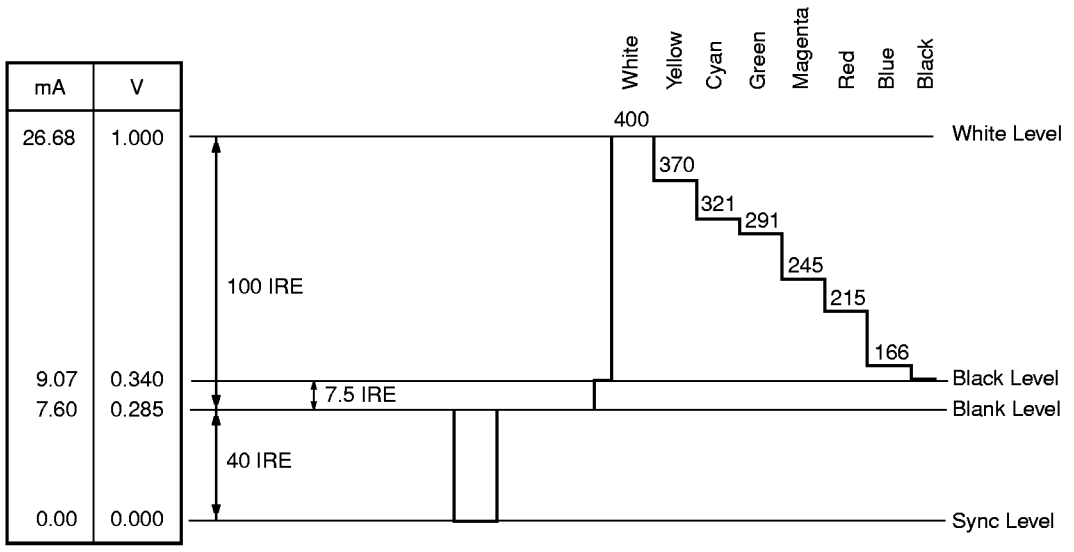
1.8.2 Chrominance (C) Analog Output

Digital chrominance information drives the 9-bit D/A converter that generates the analog C video output (Figures 1-17 and 1-18 and Tables 1-6 and 1-7).

1.8.3 Composite Video (CVβS) Output

Digital composite video information drives the 9-bit D/A converter that generates the analog NTSC or PAL video output (Figures 1-19 and 1-20 and Tables 1-8 and 1-9).

Figure 1-15. 525-Line (NTSC/PAL-M) Y (Luminance) Video Output Waveform



Conditions: 37.5 Ω load, VRDAC = VREF_OUT, nominal RSET, and SETUP = 0. SMPTE-170 M levels are assumed. Color bars at 100% saturation (100/7.5/100/7.5) are shown.

Table 1-4. 525-Line (NTSC/PAL-M) Y (Luminance) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	βLANK*
White	26.68	400	0	1
βlack	9.07	136	0	1
βlank	7.60	114	0	0
Sync	0	0	1	0

Conditions: 37.5 Ω load, VRDAC = VREF_OUT, nominal RSET, and SETUP = 0. SMPTE-170 M levels are assumed. Color bars at 100% saturation (100/7.5/100/7.5) are shown.

Figure 1-16. 625-Line (PAL-β, D, G, H, I, N, N_c) Y (Luminance) Video Output Waveform

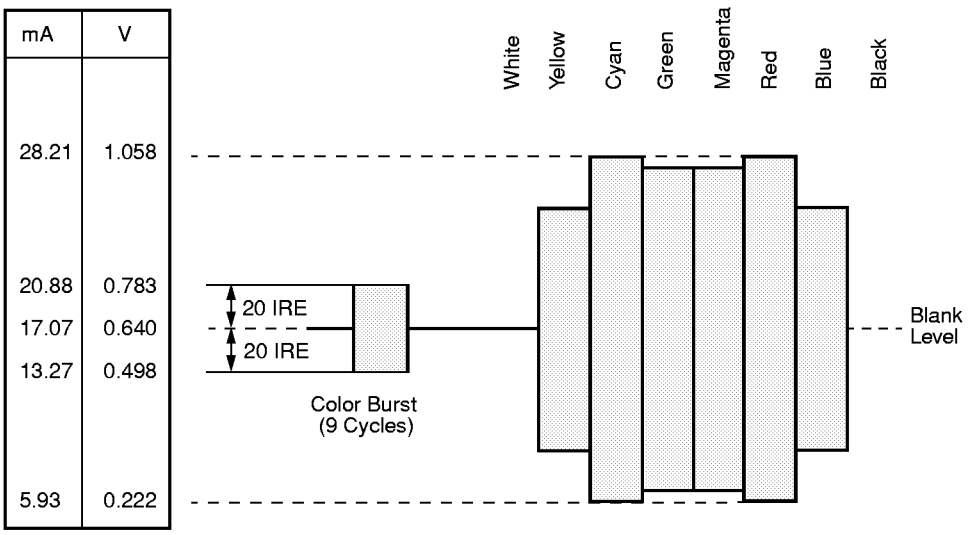
Conditions: 37.5 Ω load, VRDAC = VREF_OUT, SETUP, = 0, and nominal RSET. CCIR 624 levels are assumed. Color bars at 100% saturation (100/0/100/0) are shown.

Table 1-5. 625-Line (PAL-β, D, G, H, I, N, N_c) Y (Luminance) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	βLANK*
White	26.68	400	0	1
βlack	8.00	120	0	1
βlank	8.00	120	0	0
Sync	0	0	1	0

Conditions: 37.5 Ω load, VRDAC = VREF_OUT, SETUP, = 0, and nominal RSET. CCIR 624 levels are assumed. Color bars at 100% saturation (100/0/100/0) are shown.

Figure 1-17. 525-Line (NTSC/PAL-M) C (Chrominance) Video Output Waveform



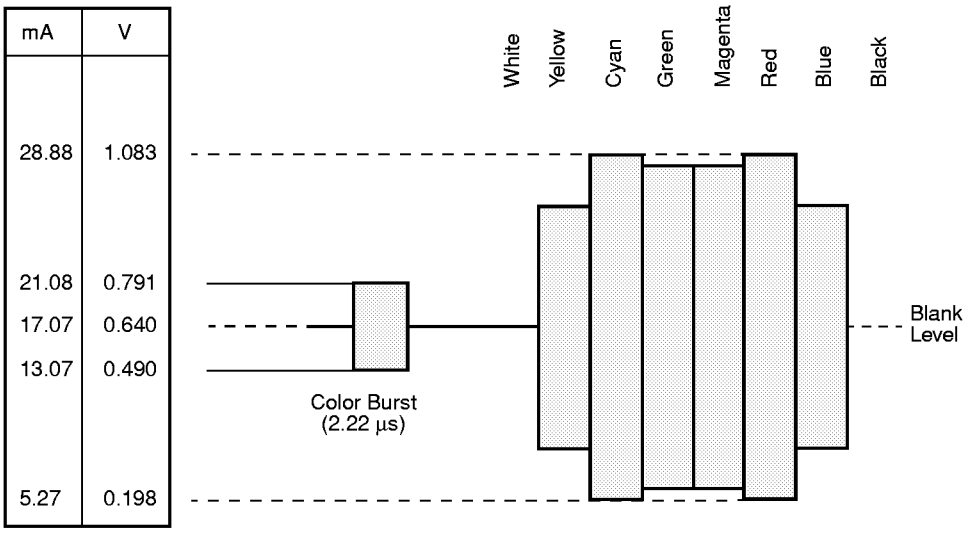
Conditions: 37.5 Ω load, VRDAC = VREF_OUT, nominal RSET, and chroma on. SMPTE-170 M levels are assumed. Color bars at 100% saturation (100/7.5/100/7.5) are shown.

Table 1-6. 525-Line (NTSC/PAL-M) C (Chrominance) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	βLANK*
Peak Chroma (High)	28.21	423	x	1
βurst (High)	20.88	313	x	x
βlank	17.07	256	x	0
βurst (Low)	13.27	199	x	x
Peak Chroma (Low)	5.93	89	x	1

Conditions: 37.5 Ω load, VRDAC = VREF_OUT, nominal RSET, and chroma on. SMPTE-170 M levels are assumed. Color bars at 100% saturation (100/7.5/100/7.5) are shown. Values for CRSCALE and CβSCALE are located in Table 2-3.

Figure 1-18. 625-Line (PAL-β, D, G, H, I, N, N_c) C (Chrominance) Video Output Waveform



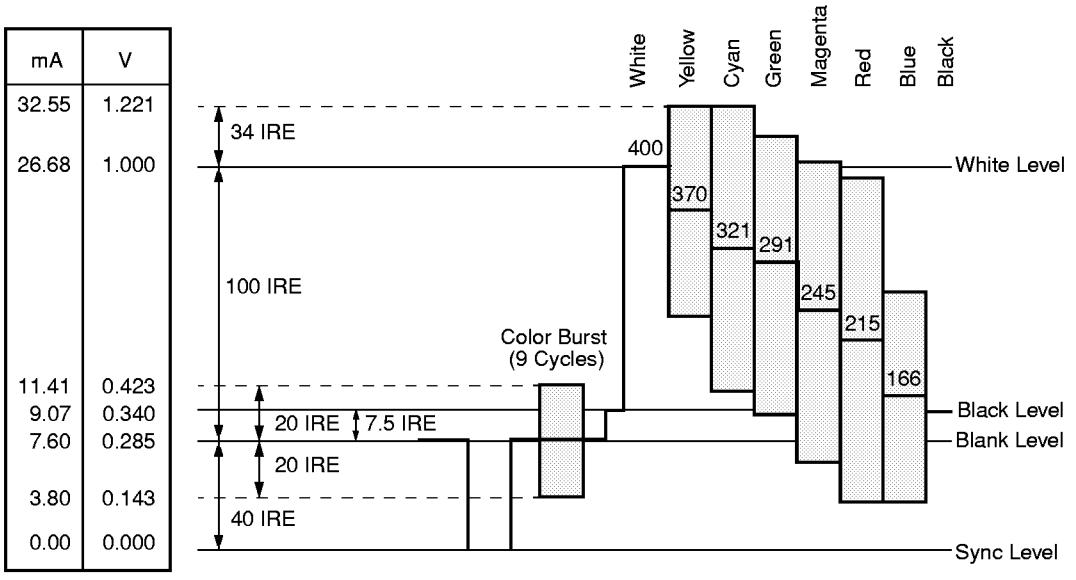
Conditions: 37.5 Ω load, VRDAC = VREF_OUT, nominal RSET, and chroma on. CCIR 624 levels are assumed. Color bars at 100% saturation (100/0/100/0) are shown.

Table 1-7. 625-Line (PAL-β, D, G, H, I, N, N_c) C (Chrominance) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	βLANK*
Peak Chroma (High)	28.88	433	x	1
βurst (High)	21.08	316	x	x
βlank	17.07	256	x	0
βurst (Low)	13.07	196	x	x
Peak Chroma (Low)	5.27	79	x	1

Conditions: 37.5 Ω load, VRDAC = VREF_OUT, nominal RSET, and chroma on. CCIR 624 levels are assumed. Color bars at 100% saturation (100/0/100/0) are shown. Values for CRSCALE and CβSCALE are located in Table 2-3.

Figure 1-19. Composite 525-Line (NTSC/PAL-M) Video Output Waveform



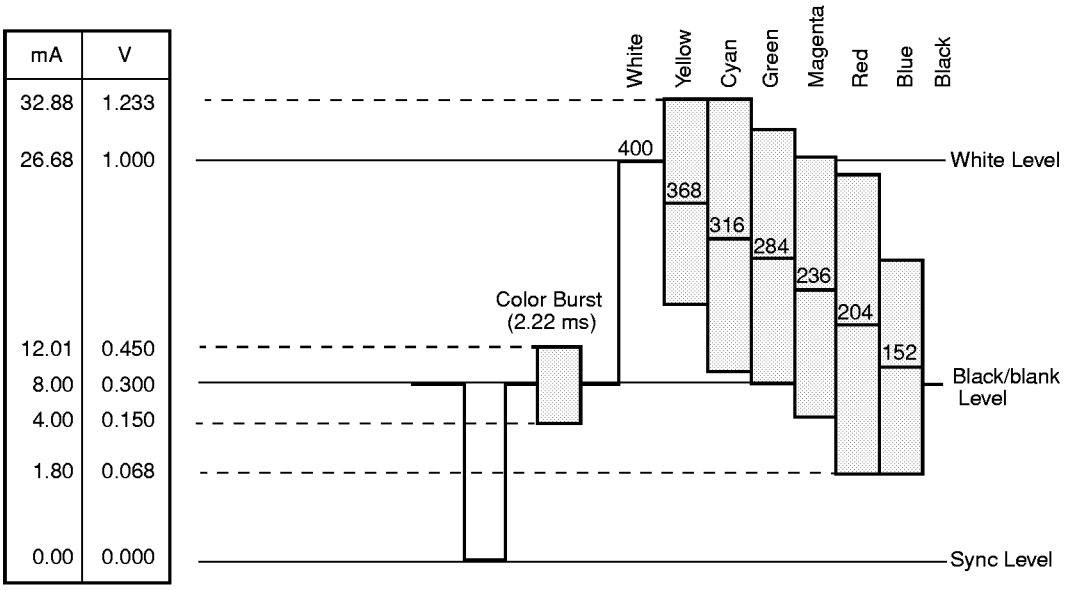
Conditions: 37.5 Ω load, VRDAC = VREF_OUT, nominal RSET, clipping off, chroma on, SETUP, = 0. SMPTE-170 M levels are assumed. Color bars at 100% saturation (100/7.5/100/7.5) are shown.

Table 1-8. Composite 525-Line (NTSC/PAL-M) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	βLANK*
Peak Chroma (High)	32.55	488	0	1
White	26.68	400	0	1
βurst (High)	11.41	171	0	x
βlack	9.07	136	0	1
βlank	7.60	114	0	0
βurst (Low)	3.80	57	0	x
Peak Chroma (Low)	3.20	48	0	1
Sync	0	0	1	0

Conditions: 37.5 Ω load, VRDAC = VREF_OUT, nominal RSET, clipping off, chroma on, SETUP, = 0. SMPTE-170 M levels are assumed. Color bars at 100% saturation (100/7.5/100/7.5) are shown. Values for CRSCALE and CβSCALE are located in Table 2-3.

Figure 1-20. Composite 625-Line (PAL-β, D, G, H, I, N, N_c) Video Output Waveform



Conditions: 37.5 Ω load, VRDAC = VREF_OUT, nominal RSET, SETUP, = 0, and clipping off. CCIR 624 levels are assumed. Color bars at 100% amplitude, and 100% saturation (100/0/100/0) are shown.

Table 1-9. Composite 625-Line (PAL-β, D, G, H, I, N, N_c) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	βLANK*
Peak Chroma (High)	32.88	493	0	1
White	26.68	400	0	1
βurst (High)	12.01	180	0	x
βlack	8.00	120	0	1
βlank	8.00	120	0	0
βurst (Low)	4.00	60	0	x
Peak Chroma (Low)	1.80	27	0	1
Sync	0	0	1	0

Conditions: 37.5 Ω load, VRDAC = VREF_OUT, nominal RSET, SETUP, = 0, and clipping off. CCIR 624 levels are assumed. Color bars at 100% amplitude, and 100% saturation (100/0/100/0) are shown. Values for CRSCALE and CβSCALE are located in Table 2-3.

2.0 Registers

2.1 Internal Registers

I²C Interface

A simplified I²C, (100 kbps) interface is provided for programming the registers. CLK must be applied and stable for I²C communication. Activating SLEEP or RESET* will disable I²C communication. It is possible for the SDA line to be held low if either SLEEP is active or a proper clock is not recognized by the device. CLK must be present for 4 cycles while RESET* is low for SDA to be released.

A read-back bit map is given in Table 2-1, and a register bit map is given in Table 2-2. Bit descriptions and detailed programming information follow the bit maps. All registers are write-only (except the ID register) and are set to zero following a software reset. A software reset is always performed at power-up; after power-up, a reset can be triggered by writing the SRESET register bit.

Data Transfer on the I²C Bus

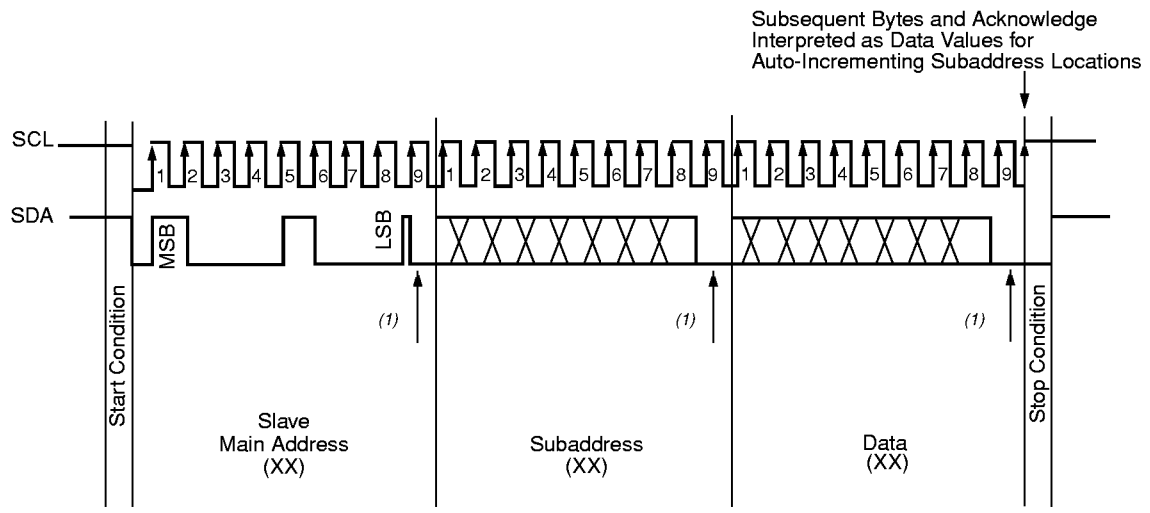
Figure 2-1 shows the relationship between SDA and SCL to be used when programming the internal registers via the I²C bus. If the bus is not being used, both SDA and SCL lines must be left high.

Every byte put onto the SDA line should be 8 bits long (MSB first), followed by an acknowledge bit, which is generated by the receiving device. Each data transfer is initiated with a start condition and ended with a stop condition. The first byte after a start condition is always the slave address byte. If this is the device's own address, the device will generate an acknowledge by pulling the SDA line low during the ninth clock pulse, then accept the data in subsequent bytes (auto-incrementing the subaddress) until another stop condition is detected.

The eighth bit of the address byte is the read/write bit (high = read from addressed device, low = write to the addressed device); so for the Bt866/867, the subaddress is only considered valid if the R/W bit is low. Data bytes are always acknowledged during the ninth clock pulse by the addressed device. During the acknowledge period, the transmitting device must leave the SDA line high.

Premature termination of the data transfer is allowed by generating a stop condition at any time. When this happens, the Bt866/867 will remain in the state defined by the last complete data byte transmitted and any master acknowledge subsequent to reading the chip ID (subaddress 0x89) is ignored.

Figure 2-1. SDA/SCL Diagram



Notes: (1) Acknowledge generated by Bt866/867.

Essential Registers

A hardware RESET must be asserted immediately after power-up for proper operation. The power-up state is defined to be black-burst CCIR 601 NTSC video. To enable active video, the EACTIVE register bit must be set high. To enable color video, the CRSCALE and CBSCALE registers must be programmed correctly. Suggested scaling coefficients are listed in the programming detail section. See Table 2-3

Important Registers

The default video format is interlaced CCIR 601 NTSC. Other video formats can be enabled by programming the five register bits: MODE[4:0]. To disable setup for NTSC, or to enable setup for PAL, the SETUP register bit must be set. Other registers may need to be programmed to achieve the desired timing of the synchronization pins; these include SYNC[2:0], HSYNCF[9:0] and HSYNCR[9:0].

Writing Addresses

Following a start condition, registers may be accessed at I^2C address 0x88 if the ALTADDR pin is low, or at 0x8A if the ALTADDR pin is high (pin 61 for 68-pin PLCC, or pin 14 for 52-pin MQFP). Following the address, a register subaddress is written to select the target register. All subaddresses are even for this part. Following the subaddress, the register data is written.

Reading Information

Following a start condition, writing 0x89 indicates a read sequence. Alternative slave address 0x8B is required if the ALTADDR pin is high. The first three bits indicate the part type (Bt866 or Bt867). The lower five bits indicate either the device version number or the Closed Captioning status bits. The ESTATUS bit controls what information is read back (See Table 2-1).

Table 2-1. CHIP I/O Read-back βit Map

ESTATUS	7	6	5	4	3	2	1	0
0	ID[2:0]			VERSION[4:0]				
1	ID[2:0]			CCSTAT[1:0]		FIELD[2:0]		

Note: The ID[2:0] bits indicate the part number: 6 is returned from the βt866; and 7 is returned from the βt867. The version number is indicated by bits VERSION[4:0]. The CCSTAT[1] bit is high if Closed Caption data has been written for the even field; it is low immediately after the clock run-in on line 284 or 335. The CCSTAT[0] bit is high if Closed Caption data has been written for the odd field; it is low immediately after the clock run-in on line 21 or 22. The FIELD[2:0] bits represent the field number, where 000 indicates the first field.

Table 2-2. Register βit Map

8-βit Subaddress (Write Only)	D7	D6	D5	D4	D3	D2	D1	D0
0x60	Reserved							
0x62	OSDY1							
•••(1)	•••							
0x7E	OSDY15							
0x80	Reserved							
0x82	OSDCR1							
•••(1)	•••							
0x9E	OSDCR15							
0xA0	Reserved							
0xA2	OSDCβ1							
•••(1)	•••							
0xβE	OSDCβ15							
0xC0	SRESET	Reserved (Write with a zero, or not at all)						
0xC2	Reserved.							
0xC4	Reserved.							
0xC6	Reserved.							
0xC8	CRSCALE							
0xCA	CβSCALE							
0xCC	DACOFF	YCSWAP	YC16	ESTATUS	ECCGATE	OSDNUM	OSDEXT	OSDβAR
0xCE	CCF2β1							
0xD0	CCF2β2							
0xD2	CCF1β1							
0xD4	CCF1β2							
0xD6	HSYNCF[7:0]							
0xD8	HSYNCR[7:0]							
0xDA	SYNC[2:0]			HSYNCF[9,8]		HSYNCR[9,8]		PORCH
0xDC	SETUP	CβSWAP	SETMODE	MODE[4:0]				
0xDE	ECCF2	ECCF1	DCHROMA	F625L	SCRESET	EVβI	EACTIVE	ECLIP
0xE0	Reserved.							
•••	Reserved.							
0xFE	Reserved.							

Notes: (1) Even addresses only.
2. Reserved registers should not be written to at all.

2.2 Programming Detail

OSDY1–OSDY15 Represent 15 Y (luminance) values, where D0 represents the LSB. Use of these lookup tables is explained in the Overlays section.

OSDCR1–OSDCR15 Represent 15 Cr (chroma) values, where D0 represents the LSB. Use of these lookup tables is explained in the Overlays section.

OSDCβ1–OSDCβ15 Represent 15 Cb (chroma) values, where D0 represents the LSB. Use of these lookup tables is explained in the Overlays section.

SRESET
0 = Normal operation.
1 = Software reset. All registers are set to 0.

CRSCALE/CβSCALE These 8-bit values are used to scale the Cr and Cb values for subsequent encoding. These registers must be programmed in order to enable color. Recommended values are shown in Table 2-3.

Table 2-3. Scaling Coefficients Table

Scaling Register	CCIR 624 (ITU-R βT.47083)		CCIR 709 or SMPTE274M Colormetry	
	With Setup	Without Setup	With Setup	Without Setup
CRSCALE	C1	CC	D9	E5
CβSCALE	89	91	8F	98

Note: These coefficients are designed to boost chroma amplitude by approximately 3% to compensate for sin(x)/x loss. Values are hexadecimal.

DACOFF

0 = Normal operation.
1 = Disable DAC output current and internal voltage reference. This will limit power consumption to just the digital circuits.

YCSWAP

0 = Normal pixel component sequence.
1 = Swap Y and C pixel components.
The normal pixel sequence is Cb-Y-Cr-Y. This sequence begins during the first CLK period following the falling edge of HSYNCO*, and repeats continuously every 4 CLK periods. Setting this bit to a 1 will enable the luma and chroma samples to be swapped at the pixel port.

YC16

0 = 8-bit mode: YCrCb data is input on P[7:0] as 8-bit multiplexed video.
1 = 16-bit mode: YCrCb data is input on P[7:0] and Y[7:0], where multiplexed CrCb is input on P[7:0].

ESTATUS

0 = Reading the CHIP I/O register returns the version number.
1 = Reading the CHIP I/O register returns Closed Captioning status and field number.

ECCGATE

0 = Normal Closed Caption encoding.
1 = Enable Closed Caption encoding constraints. After encoding, future encoding is disabled until a complete pair of new data bytes is received. This prevents encoding of redundant or incomplete data.

OSDNUM

0 = Overlay LUT values are 2's complement.
1 = Overlay LUT values are straight binary.

OSDEXT

0 = 8-color mode. Pin OSD[3] enables overlays when high. Pins OSD[2:0] select any color numbered 8-15.
1 = 15-color mode will extend range to 15 colors. Any nonzero value on pins OSD[3:0] will select a color numbered 1-15. Overlays are disabled when OSD[3:0] pins are all zero.

OSDβAR

0 = Overlays are enabled with OSD pins only.
1 = Enable colorbars. OSD pins are ignored. Overlay colors 8-15 are selected automatically during eight equal segments throughout the active video line. Standard 100/x/75/x can be achieved by programming according to Table 2-4. All numbers are hexadecimal. OSDNUM must be set to a logical 1 to use these values, which are straight binary representations.

Table 2-4. Color βar Table

Color	Y Address	Y Value	Cr Address	Cr Value	Cb Address	Cb Value
White	70	Eβ	90	80	β0	80
Yellow	72	A2	92	8E	β2	2C
Cyan	74	83	94	2C	β4	9C
Green	76	70	96	3A	β6	48
Magenta	78	54	98	C6	β8	β8
Red	7A	41	9A	D4	βA	64
βlue	7C	23	9C	72	βC	D4
βlack	7E	10	9E	80	βE	80

CCF2β1 This is the first byte of Closed Caption information for field 2. Field 2 is line 284 for NTSC or line 335 for PAL. Data is encoded MSB first.

CCF2β2 This is the second byte of Closed Caption information for field 2. Field 2 is line 284 for NTSC or line 335 for PAL. Data is encoded MSB first.

CCF1β1 This is the first byte of Closed Caption information for field 1. Field 1 is line 21 for NTSC or line 22 for PAL. Data is encoded MSB first.

CCF1β2 This is the second byte of Closed Caption information for field 1. Field 1 is line 21 for NTSC or line 22 for PAL. Data is encoded MSB first.

SYNC[2]
0 = Normal operation of HSYNCO* and VSYNCO*.
1 = Compatibility with unusual MPEG decoders is possible by using the HSYNCO* pin as an active-high pixel-blanking signal. HSYNCO* would therefore be programmed to fall at the start of active video pixels, and then rise 720 pixels later. The SYNC[2] bit keeps HSYNCO* high during the vertical blanking interval so that pixels are read only during active video lines. SYNC[2] also inverts VSYNCO* so that it is high for odd fields. The field signal must be enabled by setting SYNC[1] to 0. Programmable HSYNCO* must be enabled by setting SYNC[0] to 1.

SYNC[1]
0 = Output field signal on VSYNCO*. The field signal transitions four CLK periods prior to the falling edge of HSYNC* at the start of a new field. VSYNCO* is normally high during even fields.
1 = Output vertical synchronization pulse on VSYNCO*. The standard pulse falls at the start of a new field and is low for 3 lines or 2.5 lines, for 525-line or 625-line systems, respectively.

SYNC[0]
0 = Output default horizontal synchronization pulse on HSYNCO*. The standard pulse falls at the start of a new line and remains low for 4.7 µs.
1 = Output a programmable hsync pulse on HSYNCO*. By programming HSYNCR and HSYNCF, HSYNCO* can rise and fall at any desired time during each line.

HSYNCF [9:0]
HSYNCR [9:0]

These 10-bit values can be used to program the horizontal count for the falling and rising edges (HSYNCF and HSYNCR, respectively) of HSYNCO*. These values are useful only if variable HSYNCO* output timing is enabled with bit SYNC[0]. HSYNCF and HSYNCR cannot be zero and cannot be equal.

PORCH

0 = Front and back porch timing conforms to CCIR 624. Front porch is 1.5 µs and back porch is 9.4 or 10.5 for M-systems or PAL-systems. The active video region is therefore smaller than the 720 pixels specified in CCIR 601.
1 = Redefine porch timing per CCIR 601. This only functions in CCIR 601 mode. HSYNC* is not affected by this mode. This setting allows the full picture with 720 pixels to be encoded by using a portion of both the front and back porch for active video. (See Table 1-3.)

SETUP

0 = Normal setup. The 7.5 IRE setup is enabled for active NTSC video lines and is disabled for PAL systems.
1 = Different setup. The 7.5 IRE setup is enabled for active PAL video lines and is disabled for NTSC systems.

CβSWAP

0 = Normal pixel sequence.
1 = The Cb and Cr pixel sequence is swapped. Refer to the pixel sequence section for more information.

SETMODE

This bit is ignored in master mode. (Autodetect is not available in master mode.)
0 = Video mode is automatically detected. This is further explained in the SLAVE mode section.
1 = Override automatic mode-detection. The mode will be set according to the MODE[4:0] bits.

MODE[4:3]

0 = Configured for most common video systems.
Non zero = Configure for PAL-M, PAL-N(Argentina), and others. All possible combinations of the MODE[4:0] settings are summarized in Table 2-5. Parametric information for different video formats are summarized in Tables 1-2 and 1-3.

MODE[2]

0 = NTSC
1 = PAL

MODE[1]

0 = Interlaced 525 or 625 line operation.
1 = Non interlaced 262 or 312 line operation.

MODE[0]

0 = CCIR 601 pixel resolution.
1 = Square pixel operation.

ECCF2

0 = Disable Closed Caption encoding on field 2.
1 = Enable Closed Caption encoding on field 2.

ECCF1

0 = Disable Closed Caption encoding on field 1.
1 = Enable Closed Caption encoding on field 1.

DCHROMA
0 = Normal operation.
1 = Blank chroma.

F625L
0 = Normal operation.
1 = Force 625-line operation. Can be used to encode NTSC or PAL-M with 625 line timing.

SCRESET
0 = Normal operation. The subcarrier phase is reset at the beginning of each field sequence.
1 = Disable subcarrier reset event at beginning of field sequence.

EVβI
0 = Video is blanked during the vertical blanking interval.
1 = Enable active video during vertical blanking interval. Setup is never added during VBI, and scaling of YCrCb pixels is always based on 100% blank to white, i.e., normal PAL input scaling.

EACTIVE
0 = Enable black burst; video is blanked on all lines.
1 = Enable video during normally active lines.

ECLIP
0 = Normal operation.
1 = Enable clipping; DAC values less than 31 are made 31. This limit corresponds to roughly one-fourth of the sync height.

Table 2-5. Function of Register 0xDC βits MODE[4:0]

MODE[4:0]	Format	Line Rate	Luminance Sample Rate(3)	SC Frequency	Typical Market
00000	NTSC Interlaced 601	15734.264	13,500,000	3,579,545.00	N. America, Japan
00010	NTSC Noninterlaced 601	15734.264	13,500,000	3,579,575.00	N. America, Japan
001X0	PAL-β,D,G,H,I,N 601	15625.000	13,500,000	4,433,618.75	W. Europe, SE Asia
011X0	PAL-N_c 601	15625.000	13,500,000	3,582,056.25	Argentina
101X0(1)	PAL-M 60 Hz HDTV	15750.000	13,513,500	3,575,611.49	βrazil-SDTV
11000(2)	NTSC-60 Hz Interlaced HDTV	15750.000	13,513,500	3,579,545.00	N. America
11010(2)	NTSC 60 Hz Noninterlaced HDTV	15750.000	13,513,500	3,579,575.00	N. America
111X0(1)	PAL-M 601	15734.264	13,500,000	3,575,611.49	βrazil
00001	NTSC Interlaced Square	15734.264	12,272,727	3,579,545.00	N. America, Japan
00011	NTSC Noninterlaced Square	15734.264	12,272,727	3,579,575.00	N. America, Japan
001X1	PAL-β,D,G,H,I,N Square	15625.000	14,750,000	4,433,618.75	W. Europe, SE Asia
011X1	PAL-N_c Square	15625.000	14,750,000	3,582,056.25	Argentina
101X1(1)	PAL-M 60 Hz Square-HDTV	15750.000	12,272,727	3,575,611.49	βrazil-SDTV
11001	NTSC 60 Hz Interlaced Square HDTV	15750.000	12,285,000	3,579,545.00	N. America
11011	NTSC 60 Hz Noninterlaced Square HDTV	15750.000	12,285,000	3,579,575.00	N. America
111X1(1)	PAL-M Square	15734.264	12,285,000	3,575,611.49	βrazil

Notes: (1) With setup enabled, the sync amplitude is slightly higher than normal for the VβI lines. Without setup enabled, all lines are slightly high.
(2) SCRESET should be 1.
(3) Input CLK or xtal frequencies must be 2x Luminance Sample Rate.
4. Hex modes 0x10 through 0x13 are reserved. Rates are in Hertz. SETUP should be set high for Japan, Uruguay, and Paraguay. Note that the interlaced mode bit is a don't-care (x) for PAL modes in this table.

3.0 PC Board Considerations

The layout should be optimized for lowest noise on the power and ground planes by providing good decoupling. The trace length between groups of power and ground pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for ground and power, respectively.

3.0.1 Component Placement

Components should be placed as close as possible to the associated pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt866/867 to be located as close as possible to the power supply connector and the video output connector.

3.0.2 Power and Ground Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board. The analog power plane should provide power to all analog power pins, protection diodes, RF modulator, VREF circuitry, VBIAS, and COMP decoupling. There should be at least a 1/8-inch gap between the digital and analog power planes, connected by a single point through a ferrite bead, as illustrated in Figure 3-1. The ground plane should be a single unified plane overlapping both analog and digital power planes. The path back to the power supply should be the lowest impedance possible with only one possible return path. This layout eliminates noise on the analog signals caused by cross-currents from digital switching.

This bead should be located within 3 inches of the Bt866/867. The bead provides impedance to switching currents, which provides increased impedance at high frequencies. A low-resistance (<0.5 Ω) bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743021447, or TDK BF45-4001.

Figure 3-1. Example Power Plane Layout

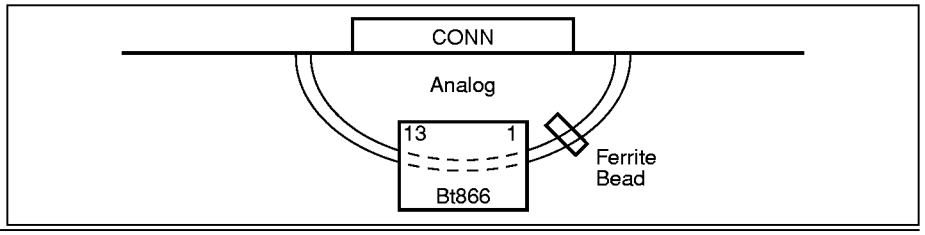


Figure 3-2. Typical Connection Diagram

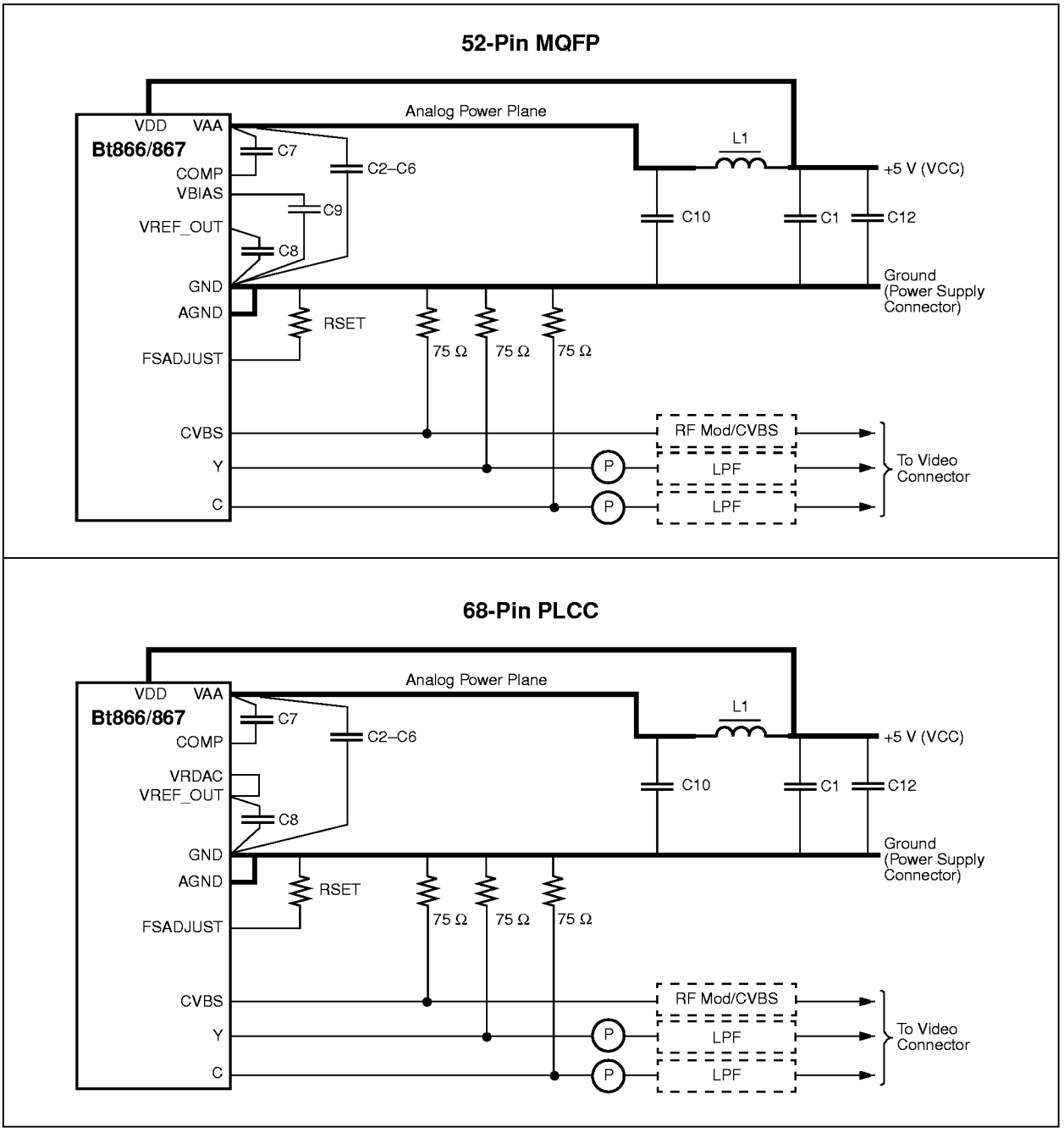
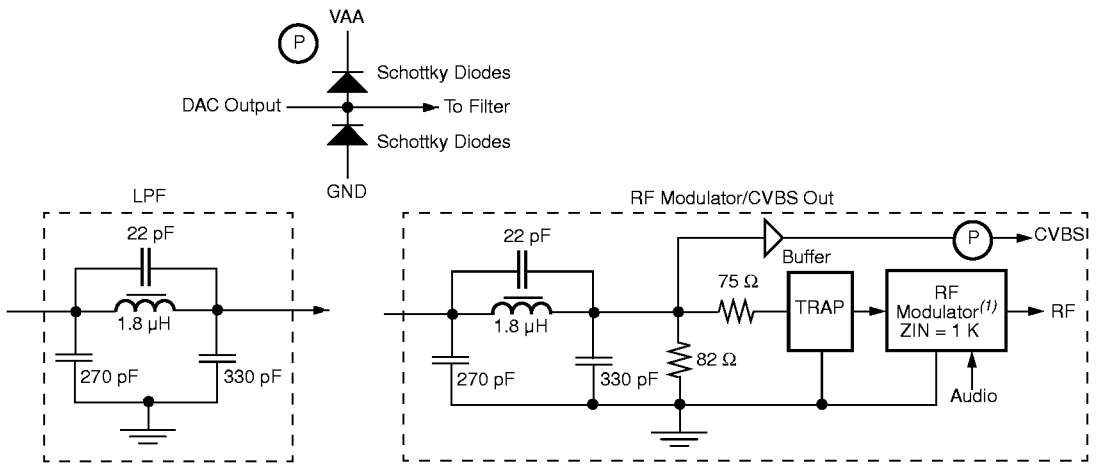


Figure 3-3. External Component and Filter Circuitry



Notes: (1) Some modulators will require AC coupling capacitors (10 µF).

Table 3-1. Typical Parts List

Location	Description	Vendor Part Number
C1–C9	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C10, C12	47 µF Capacitor	Mallory CSR13F476KM
L1	Ferrite βead - Surface Mount	Fair-Rite 2743021447
RSET	1% Metal Film Resistor (100 Ω)	Dale CMF-55C
TRAP	Ceramic Resonator	Murata TPSx.xMJ or Mβ2 (where x.x = sound carrier frequency in MHz)
	Schottky Diodes	βAT85 (βAT54F Dual) HP 5082-2305 (1N6263) Siemens βAT 64-04 (Dual)

Note: Vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect βt866/867 performance.

3.1 Decoupling

3.1.1 Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors can be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

3.1.2 Power Supply Decoupling

The best power supply performance is obtained with a 0.1 µF ceramic capacitor decoupling each group of power pins to GND. The capacitors should be placed as close as possible to the device power and GND pins and connected with short, wide traces.

The 47 µF capacitor shown in Figure 3-2 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 5% of the power supply hum and ripple noise, less than 1 MHz, will couple onto the analog outputs.

3.1.3 COMP Decoupling

The COMP pin must be decoupled to the closest VAA pin, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

3.1.4 VREF_OUT Decoupling

For 52-pin MQFP only: A 0.1 µF ceramic capacitor should be used to decouple this pin to AGND.

3.1.5 VRDAC Decoupling

For 68-pin PLCC only: A 0.1 µF ceramic capacitor should be used to decouple this input to AGND.

3.1.6 VBIAS Decoupling

For 52-pin MQFP only: A 0.1 µF ceramic capacitor should be used to decouple this pin to AGND.

3.2 Signal Interconnect

3.2.1 Digital Signal Interconnect

The digital inputs to the Bt866/867 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one-fourth the signal edge time. Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing can be reduced by damping the line with a series resistor (30–300 Ω).

The analog circuitry can also pick up radiation of digital signals. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

3.2.2 Analog Signal Interconnect

The Bt866/867 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should overlay the ground plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and AGND should be as close as possible to the Bt866/867 to minimize reflections. Unused DAC outputs should be connected to AGND.

3.3 Applications Information

3.3.1 ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage. Device damage can produce symptoms of catastrophic failure or erratic device behavior with leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided; they could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA and GND pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage.

3.3.2 Clock and Subcarrier Stability

The color subcarrier is derived directly from the CLK input, hence any jitter or frequency deviation of CLK will be transferred directly to the color subcarrier. Jitter within the valid CLK cycle interval will result in hue noise on the color subcarrier on the order of 0.9–1.6 degrees per nanosecond. Random hue noise can result in degradation in AM/PM noise ratio (typically around 40 dB for consumer media such as Videodiscs and VCRs). Periodic or coherent hue noise can result in differential phase error (which is limited to 10 degrees by FCC cable TV standards).

Any frequency deviation of the CLK from nominal will challenge the subcarrier tracking capability of the destination receiver. This can range from a few parts-per-million (ppm) for broadcast equipment to 50 ppm for industrial equipment to a few hundred ppm for consumer equipment. Greater subcarrier tracking range generally results in poorer subcarrier decoding dynamic range. This means that wide subcarrier frequency deviation and receivers that tolerate jitter will introduce more noise in the decoded image. Crystal clock sources provide best stability and lowest jitter, with 50–100 ppm accuracy required by most industrial or consumer receivers. A 30-ppm tolerance constraint applies for Teletext and MPEG2.

Some applications call for maintaining correct Subcarrier-Horizontal (SC-H) phasing for correct color framing, which requires subcarrier coherence within specified tolerances over a four-field interval for 525-line systems or 8 fields for 625-line systems. Any CLK interruption (even during vertical blanking interval), which results in mis-registration of the CLK input or nonstandard pixel counts per line, can result in SC-H excursions outside the NTSC limit of ±40 degrees (reference EIA RS170A) or the PAL limit of ±20 degrees (reference EBU D23-1984).

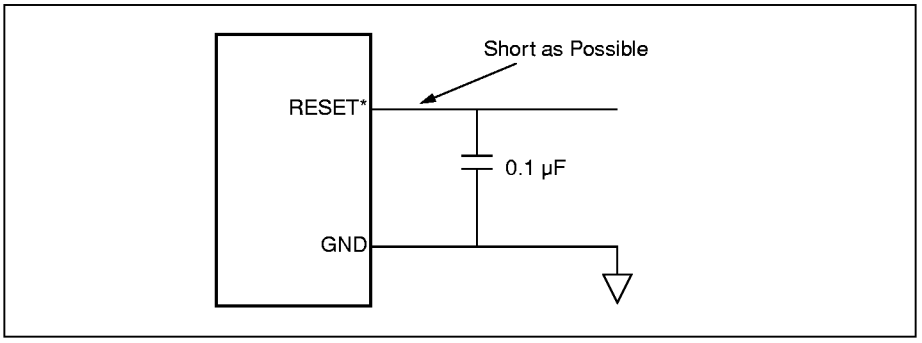
In slave mode, any deviation of the number CLK cycles between HSYNC* falling edges when in slave mode can result in automatic mode switching, unless the SETMODE bit is set for the desired mode of operation.

3.3.3 Reset Precautions

The user should make the length of the traces connected to the RESET* input pin as short as possible. In addition, Rockwell recommends that a 0.1 µF capacitor be connected across the RESET* input pin and the digital ground pins (GND) for decoupling purposes (see Figure 3-4.)

All of Bt866/867's programmable register bits can be reset through software (i.e., setting register bit SRESET = 1). Furthermore, both the Bt866/867's registers and timing can be reset by a low pulse of at least 0.05 µs (>1 complete period of CLK) input directly to RESET*. If noise, having a pulse width close to 0.05 µs, is inadvertently input to RESET*, it could cause the encoder to unintentionally reset the subcarrier phase and/or the horizontal and vertical counters. This type of timing error could cause faulty system operation (see Figure 3-4).

Figure 3-4. Wiring for the RESET* Input Pin



4.0 Parametric Information

4.1 DC Electrical Parameters

Table 4-1. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (Measured to GND)				7.0	V
Voltage on Any Signal Pin(1)		GND –0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		Indefinite		
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+125	°C
Vapor Phase Soldering (1 Minute)	TVSOL			220	°C

Notes: (1) This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply or ground voltage by more than 0.5 V can cause destructive latchup.
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		70	°C
DAC Output Load(1)	RL		37.5		Ω
Nominal RSET	RSET		100		Ω

Notes: (1) C component not to exceed 80 Ω.
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 DC Characteristics

Table 4-3. DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Output Current-DAC Code 511 (Iout FS)		32.03	34.08	36.12	mA
Output Voltage-DAC Code 511		1.19	1.28	1.37	V
Video Level Error		–5		5	%
Output Capacitance			22		pF
Digital Inputs (except those specified below)					
Input High Voltage	VIH	2.0		VAA +0.5	V
Input Low Voltage	VIL	GND –0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		7		pF
SCL, SDA, XTAL_IN					
Input High Voltage	VIH	0.7 VAA		VAA +0.5	V
Input Low Voltage	VIL	GND –0.5		0.3 VAA	V
SLEEP Input					
Input High Voltage	VIH	2.0		VAA +0.5	V
Input Low Voltage	VIL	GND –0.5		0.6	V
CLK Input					
Input High Voltage	VIH	2.4		VAA +0.5	V
Input Low Voltage	VIL	GND –0.5		0.8	V
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
Three-State Current	IOZ			50	µA
Output Capacitance	CDOUT		10		pF
VREF_IN Input Current	IREF_IN		10		µA

Note: As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature (25° C) and nominal voltage (5 V).

4.3 AC Characteristics

Table 4-4. AC Characteristics *(1 of 2)*

Parameter	EIA/TIA 250C Ref	Min	Typ	Max	Units
Hue Accuracy[1, 2, 6]			1.0	2.5	± °
Color Saturation Accuracy[1, 2]			1.0	2.3	± %
Chroma AM/PM Noise[3]	1 MHz Red Field		–62		dβ rms
Differential Gain[2]	6.2.2.1		1.3		% p–p
Differential Phase[2]	6.2.2.2		1.1		° p–p
SNR (Unweighted 100 IRE Y Ramp Tilt Correct)[2]					
RMS	6.3.1		60		dβ rms
Peak Periodic	6.3.2		56		dβ p-p
100 IRE Multiburst	6.1.1		–5	6.0	± IRE
Chroma/Luma Gain Ineq[2]	6.1.2.2		–5		± IRE
CVβS Output			–2		± IRE
Y/C Output			–7		± IRE
Chroma/Luma Delay Ineq[2]	6.1.2		2	5	ns
Short Time Distortion 100 IRE/Pixel[2]	6.1.6		1.8		%
Luminance Nonlinearity[2]	6.2.1		2		%
Chroma/Luma Intermod[2]	6.2.3		0.1		± IRE
Chroma Nonlinear Gain[2]	6.2.4.1		1.0	1.5	± IRE
Chroma Nonlinear Phase[2]	6.2.4.2		0.1	1.0	± °
Pixel/Control Setup Time[4]		7			ns
Pixel/Control Hold Time[4, 5]		3			ns
Control Output Delay Time[4]		2		17	ns
Control Output Hold Time[4]		2			ns

Table 4-4. AC Characteristics *(2 of 2)*

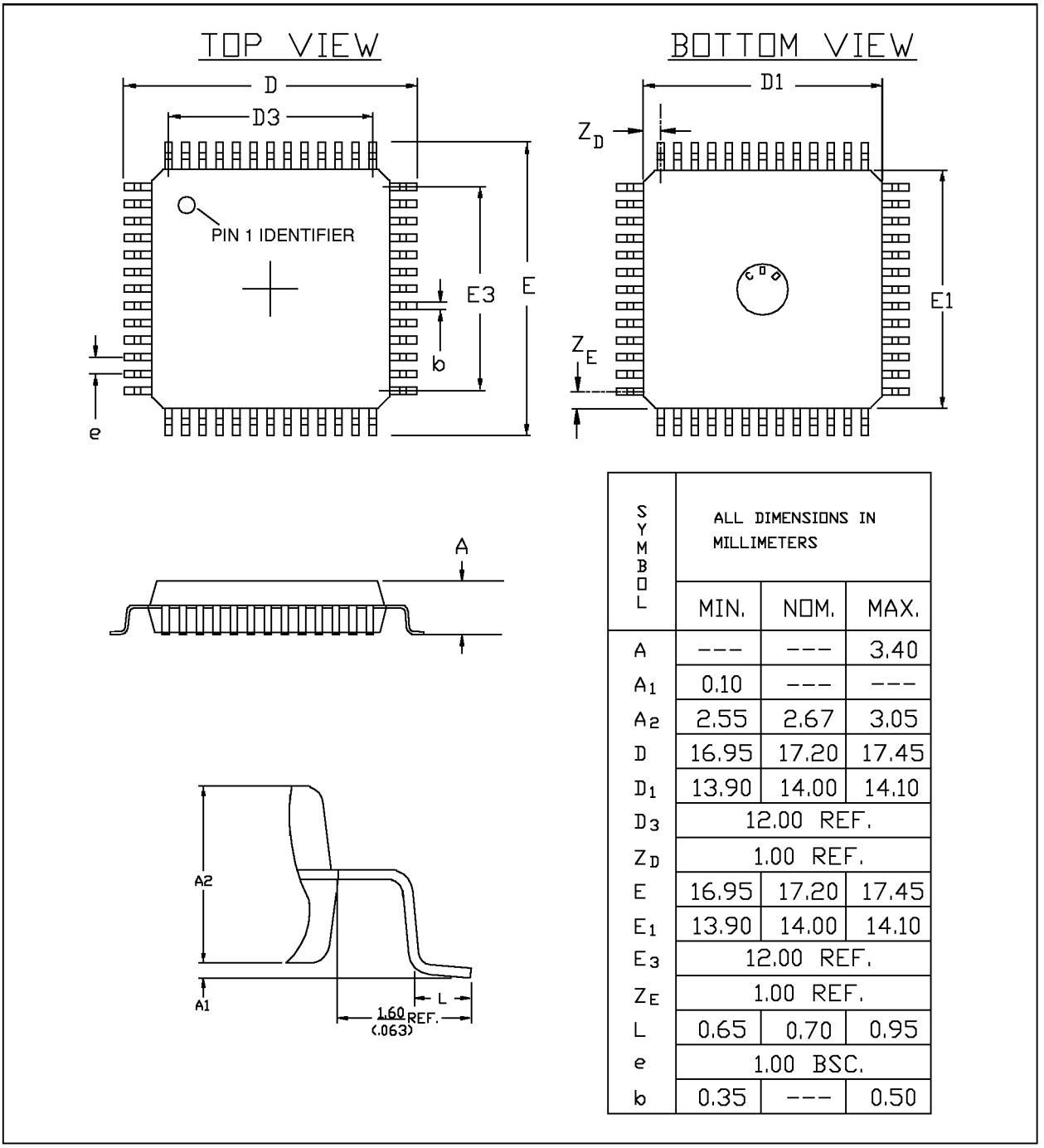
Parameter	EIA/TIA 250C Ref	Min	Typ	Max	Units
CLK Frequency		24.54	27	29.50	MHz
CLK Pulse Width Low Time		8			ns
CLK Pulse Width High Time		8			ns
Total Supply Current			170	210	mA
Power-Down Mode Current			10		mA

Notes: (1) 100/7.5/75/7.5 color bars normalized to burst.
(2) Guaranteed by characterization at CCIR resolution NTSC-M without post filter.
(3) Without post filter. Guaranteed by design.
(4) Control pins are defined as HSYNC*, VSYNC*, HSYNCO*, VSYNCO*, SLAVE, SDA, SCL.
(5) 300 ns hold time SDA–SCL not provided.
(6) The SC-H phase is nonzero and depends upon the clock rate and the video standard chosen.
7. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature (25° C) and nominal voltage (5 V).

4.4 Package Drawings

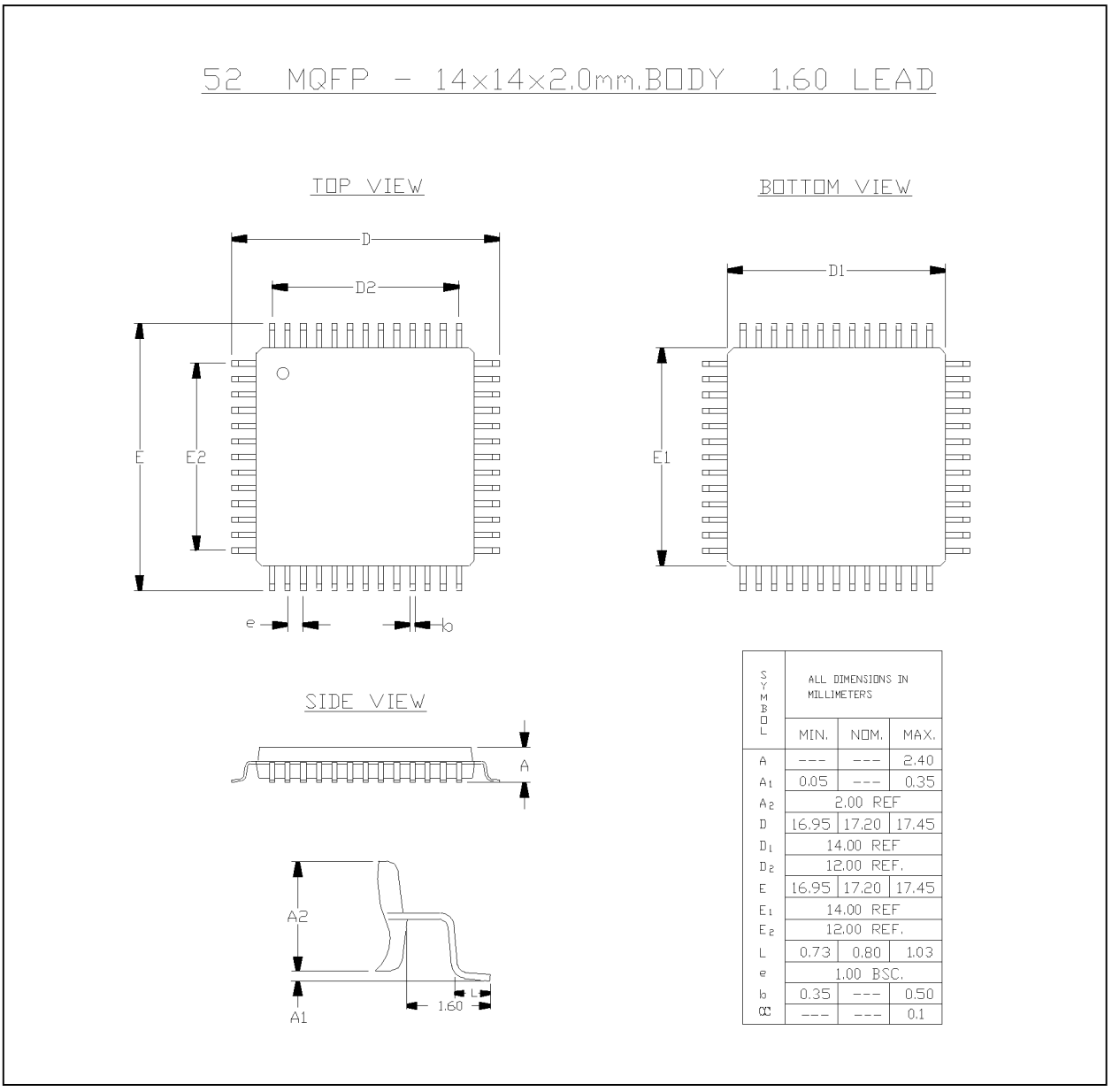
See Ordering Information at beginning of document for further details on part numbers and package usage.

Figure 4-1. 52-Pin Metric Quad Flatpack (MQFP) - Effective for Part Numbers 25866-11 and 25867-11



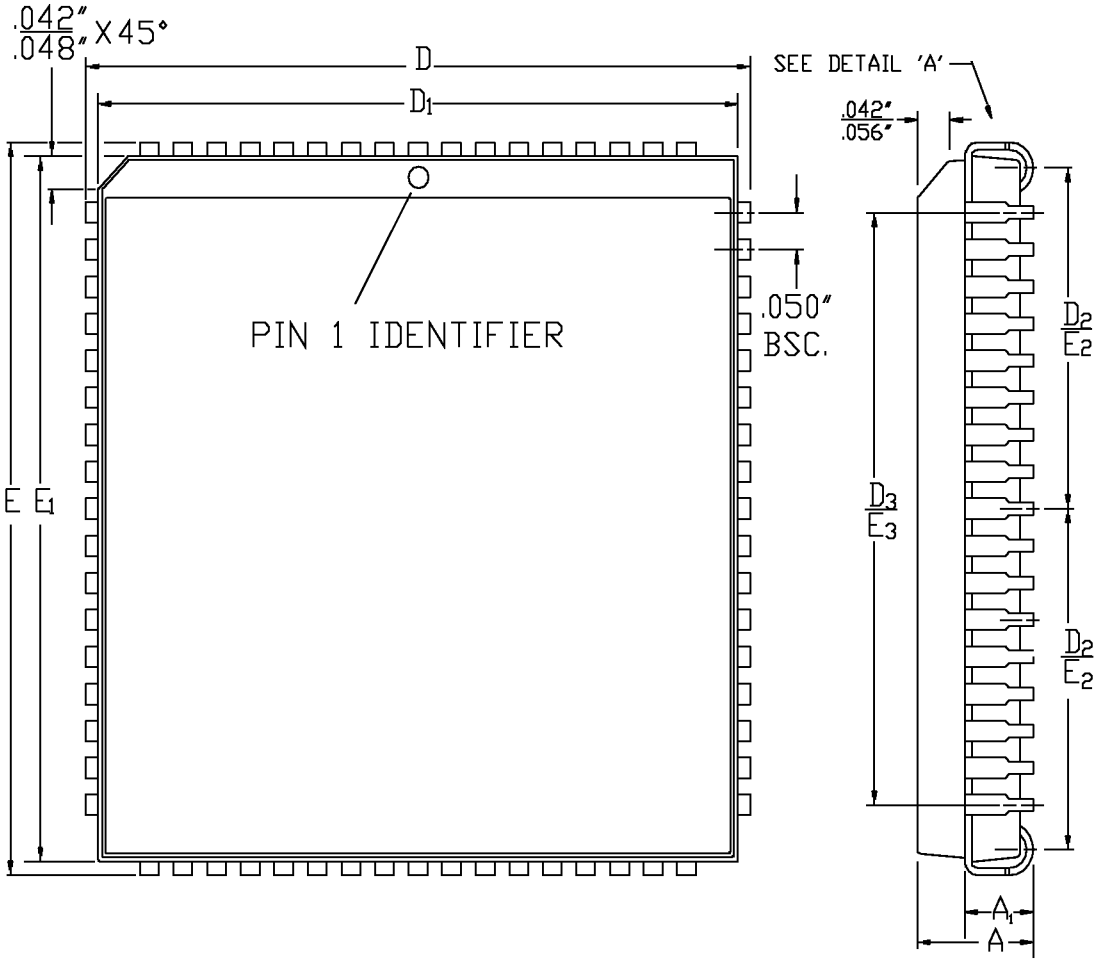
SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	3.40
A_1	0.10	---	---
A_2	2.55	2.67	3.05
D	16.95	17.20	17.45
D_1	13.90	14.00	14.10
D_3	12.00 REF.		
Z_D	1.00 REF.		
E	16.95	17.20	17.45
E_1	13.90	14.00	14.10
E_3	12.00 REF.		
Z_E	1.00 REF.		
L	0.65	0.70	0.95
e	1.00 BSC.		
b	0.35	---	0.50

Figure 4-2. 52-Pin Metric Quad Flatpack (MQFP) - Effective for Part Numbers 25866-13



SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	2.40
A_1	0.05	---	0.35
A_2	2.00 REF		
D	16.95	17.20	17.45
D_1	14.00 REF		
D_2	12.00 REF.		
E	16.95	17.20	17.45
E_1	14.00 REF		
E_2	12.00 REF.		
L	0.73	0.80	1.03
e	1.00 BSC.		
b	0.35	---	0.50
ccc	---	---	0.1

Figure 4-3. 68-Pin Plastic Leaded Chip Carrier (PLCC)



SYMBOL	INCHES			MILLIMETERS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	.165		.200	4.20		5.08
A_1	.090		.130	2.29		3.30
D	.985		.995	25.02		25.27
D_1	.950		.958	24.13		24.33
D_2	.445		.465	11.30		11.81
D_3	.800 REF.			20.32 REF.		
E	.985		.995	25.02		25.27
E_1	.950		.958	24.13		24.33
E_2	.445		.465	11.30		11.81
E_3	.800 REF.			20.32 REF.