ANALOG DEVICES

16-Channel Data Acquisition System

AD1341

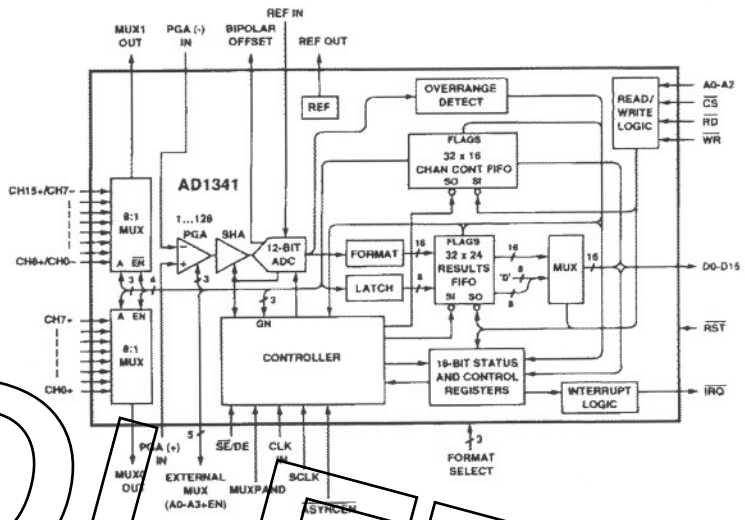
FEATURES

- 150,000 Channels/Second Throughput Rate
- Analog Inputs
  - 16 Single-Ended (SE) or 8 Differential (DE); Expandable to 32 SE or 16 DE
  - Over Voltage Protected
  - Power Supply Loss Protected
- Programmable Gain Amplifier (PGA)
  - Binary Gains 1 to 128
  - Independent Gain Selection per Channel
- 12-Bit Sampling A/D Converter
- Processor Interface
  - FIFOs for Channel Control and Conversion Results
  - Fully Asynchronous 16-Bit Parallel Bus
  - 15 ns Data Access Time
  - Selectable 16-Bit Data Format
  - Programmable Interrupt Structure
- Ceramic Surface Mount Package

APPLICATIONS

- DSP Data Acquisition
- Missile Guidance
- Vibration Analysis
- Process Control

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1341 is a complete 16-channel data acquisition system optimized for use in multichannel control and digital signal processing applications. The device consists of two 8-channel input multiplexers, a programmable gain amplifier (PGA), a 12-bit sampling A/D converter, two 32-word FIFOs, a controller, and registers for status and control. The device is packaged in a 100-lead ceramic quad flat package.

The input multiplexers can be configured for either 16 channels of single-ended input or 8 channels of differential input. The number of channels can be doubled with the addition of a single external 16-channel multiplexer. The inputs are protected against power loss for applications where the AD1341 is not powered from the same source as its inputs.

The programmable gain amplifier has differential inputs and 8 binary gain ranges from 1 to 128. Each channel can be programmed for a different gain. The controller timing allows the AD1341 to operate at the full 150,000 channels/second at gains from 1 to 8. Above 8, the throughput rate decreases proportionately to the increase in gain.

The 12-bit sampling A/D converter is specified and tested for both static and dynamic performance.

The AD1341 communicates asynchronously with the microprocessor over a 16-bit-wide data path. Data can be formatted in either straight binary or twos complement with left, center or right justification. A 32-word FIFO is used to control channel selection and PGA gain. A second 32-word FIFO is used to store A/D conversion results.

PRODUCT HIGHLIGHTS

1. High throughput rate makes the AD1341 ideal for use in a wide range of applications in motion control, speech processing, PC data acquisition, medical instrumentation, and missile guidance.
2. Software development is simplified because timing for channel selection, PGA gain changing and settling, and A/D conversion is internal to the AD1341. Registers are available for enabling interrupt conditions and polling interrupt conditions or real-time status.
3. Software overhead is reduced by having FIFOs store channel information and conversion results.
4. Processor interface is simplified because the AD1341 operates fully asynchronously to the processor, has a maximum 15 ns data access time and is isolated by hybrid circuit construction.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

AD1341—SPECIFICATIONS

(T_A = +25°C, V_S = ±15 V dc, V_{DD} = +5 V dc, 16-channel, single-ended bipolar mode, ASYNCEN = Low, F_{CLK} = 3.0 MHz, and G = 1, unless otherwise noted)

Parameter	AD1341KZ Min	AD1341KZ Typ	AD1341KZ Max	AD1341TZ Min	AD1341TZ Typ	AD1341TZ Max	Units
ANALOG INPUTS (Per Channel)							
Impedance							
Single Ended		100‖50			100‖50		MΩ‖pF
Differential		100‖25			100‖25		MΩ‖pF
Voltage Range							
Common Mode	±10			±10			V
Differential		10÷G			10÷G		V
CMRR @ 120 Hz, G = 1	80	90		80	90		dB
G = 128	80	90		80	90		dB
Bias Current (V_{CM} = 0)		±0.1	±2		±0.1	±2	nA
T_{min} to T_{max}			±200			±300	nA
Voltage Noise (RTI) G = 1		75			75		μV rms
G = 128		10			10		μV rms
ANALOG OUTPUT							
Reference Voltage	9.90		10.10	9.90		10.10	V
Drift		±10	±30		±10	±30	ppm/°C
Output Current	±1	±2		±1	±2		mA
TRANSFER CHARACTERISTICS							
Standard Throughput Rate[1]							
G = 1, 2, 4 or 8	150,000			150,000			Chan/Sec
G = 16	75,000			75,000			Chan/Sec
G = 32	37,500			37,500			Chan/Sec
G = 64	18,750			18,750			Chan/Sec
G = 128	9,375			9,375			Chan/Sec
Accelerated Throughput Rate[1, 2]							
G = 1, 2, 4 or 8	150,000			150,000			Chan/Sec
G = 16	100,000			100,000			Chan/Sec
G = 32	57,690			57,690			Chan/Sec
G = 64	29,410			29,410			Chan/Sec
G = 128	14,850			14,850			Chan/Sec
STATIC CHARACTERISTICS							
PGA Gain Accuracy (Any Gain)		±1/2	±2		±1/2	±2	%
Integral Nonlinearity		±1/2	±1		±1/2	±1	LSB
T_{min} to T_{max}			±1			±1	LSB
Resolution for No Missing Codes	12			12			Bits
T_{min} to T_{max}	12			12			Bits
Unipolar Offset Error		±1	±2		±1	±2	LSB
T_{min} to T_{max}			±4			±6	LSB
Bipolar Zero Error		±1	±2		±1	±2	LSB
T_{min} to T_{max}			±4			±6	LSB
Gain Error		±1	±2		±1	±2	LSB
T_{min} to T_{max}			±8			±12	LSB
DYNAMIC CHARACTERISTICS							
SNR							
G = 1, f_S = 150.0 kHz[3]	70	73		70	73		dB
G = 2, f_S = 150.0 kHz		72			72		dB
G = 4, f_S = 150.0 kHz		72			72		dB
G = 8, f_S = 150.0 kHz		71			71		dB
G = 16, f_S = 75.0 kHz[3]	68	71		68	71		dB
G = 32, f_S = 37.5 kHz		70			70		dB
G = 64, f_S = 18.8 kHz		69			69		dB
G = 128, f_S = 9.4 kHz		66			66		dB

Parameter	AD1341KZ Min	AD1341KZ Typ	AD1341KZ Max	AD1341TZ Min	AD1341TZ Typ	AD1341TZ Max	Units
THD							
G = 1, f_S = 150.0 kHz[3]		−90	−80		−90	−80	dB
G = 2, f_S = 150.0 kHz		−90			−90		dB
G = 4, f_S = 150.0 kHz		−88			−88		dB
G = 8, f_S = 150.0 kHz		−88			−88		dB
G = 16, f_S = 75.0 kHz[3]		−88	−78		−88	−78	dB
G = 32, f_S = 37.5 kHz		−88			−88		dB
G = 64, f_S = 18.8 kHz		−85			−85		dB
G = 128, f_S = 9.4 kHz		−84			−84		dB
CHANNEL-TO-CHANNEL ISOLATION		80			80		dB
DIGITAL INPUTS[4]							
Input Voltage							
Logic Low			0.8			0.8	V
Logic High	2.0			2.25			V
Input Current		±60	±200		±60	±200	μA
Input Capacitance		2			2		pF
$\overline{RST}$ Low Pulse Width	10			10			ns
CLK Input							
Frequency			3.0			3.0	MHz
Duty Cycle	45		55	45		55	%
DIGITAL OUTPUTS[4]							
Output Voltage							
Logic Low							
I_{OL} = 4.0 mA		0.2	0.4				V
I_{OL} = 3.2 mA					0.2	0.4	V
Logic High							
I_{OH} = −4.0 mA	2.4	4.5					V
I_{OH} = −3.2 mA				2.4	4.5		V
Output Capacitance		6			6		pF
High Impedance Leakage, D0–D15		±60	±200		±60	±200	μA
Off State Leakage, $\overline{IRQ}$		±1	±10		±1	±10	μA
POWER SUPPLY							
Operating Voltage Range							
$+V_S$	+14.25		+15.75	+13.5		+16.5	V
$-V_S$	−15.75		−14.25	−16.5		−13.5	V
V_{DD}	+4.75		+5.25	+4.5		+5.5	V
Quiescent Current							
$+V_S$		41	56		41	56	mA
$-V_S$		35	50		35	50	mA
V_{DD}		5	10		5	10	mA
POWER CONSUMPTION		1.2	1.6		1.2	1.6	W
PSRR, $\pm V_S$		±1/2			±1/2		LSB/V
TEMPERATURE RANGE							
Operating and Specified	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	°C

NOTES

[1]All channel gains are fixed at the specified value.

[2]Accelerated performance is achieved through using a pipeline architecture and constant SHA acquisition times (see page 12 of this data sheet).

[3]f_{IN} = 4.6 kHz for G = 1, 2.3 kHz for G = 16 tests. SNR excludes harmonics 2–9. THD includes harmonics 2–9. Input amplitude is −0.3 dB relative to full-scale at each gain.

[4]Guaranteed over operating temperature range, tested at +25°C only.

Specifications subject to change without notice.

AD1341

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to APWR/ASIG GND . . . . . +18 V
$-V_S$ to APWR/ASIG GND . . . . . −18 V
V_{DD} to DGND . . . . . +7 V
APWR/ASIG GND to DGND . . . . . −0.3 V to +0.3 V
Analog Inputs to APWR/ASIG GND
Multiplexer . . . . . $+V_S$ + 16 V, $-V_S$ − 16 V
PGA . . . . . $-V_S$ to $+V_S$
Reference Input . . . . . 0 V to +11 V
Digital Inputs to DGND . . −0.3 V to V_{DD} + 0.3 V or 10 mA
Output Short Circuit Duration
Reference & Multiplexer Outputs . . . . . Indefinite
Digital Outputs . . . . . 1 Output for 1 Second
Lead Soldering Temperature (10 seconds) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

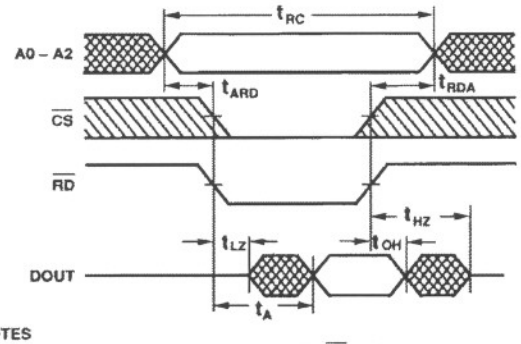
SWITCHING CHARACTERISTICS (Over operating temperature and power supply voltage range, with C_{OUT} = 30 pF or 100 pF except where noted)

Parameter	Description	Condition	Min	Typ	Max	Units
READ CYCLE						
t_{RC}	Read Cycle Time	C_{OUT} = 30 pF	25			ns
		C_{OUT} = 100 pF	35			ns
t_A	Data Access Time	C_{OUT} = 30 pF			15	ns
		C_{OUT} = 100 pF			25	ns
		C_{OUT} = 150 pF			35	ns
t_{LZ}	Output LO-Z Time		2			ns
t_{HZ}	Output HI-Z Time	C_{OUT} = 30 pF			15	ns
		C_{OUT} = 100 pF			25	ns
t_{OH}	Output Hold Time		2			ns
t_{ARD}	Address Valid to $\overline{RD}$ Low		3			ns
t_{RDA}	$\overline{RD}$ High to Address Invalid		3			ns
t_{ACS}	Address Valid to $\overline{CS}$ Low		3			ns
t_{CSA}	$\overline{CS}$ High to Address Invalid		3			ns
WRITE CYCLE						
t_{WC}	Write Cycle Time		15			ns
t_{WP}	Write Pulse Width		5			ns
t_{SU}	Input Setup Time		2			ns
t_{IH}	Input Hold Time		3			ns
t_{AWR}	Address Valid to $\overline{WR}$ Low		3			ns
t_{WRA}	$\overline{WR}$ High to Address Invalid		3			ns
t_{ACS}	Address Valid to $\overline{CS}$ Low		3			ns
t_{CSA}	$\overline{CS}$ High to Address Invalid		3			ns

ORDERING GUIDE

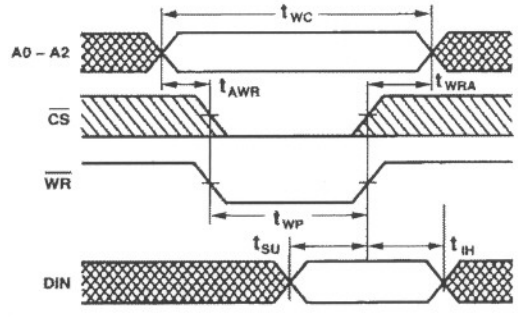
Model	Temperature Range	Package Option*
AD1341KZ	0°C to +70°C	Z-100
AD1341TZ/883B	−55°C to +125°C	Z-100

*Z = Ceramic Leaded Chip Carrier Package.



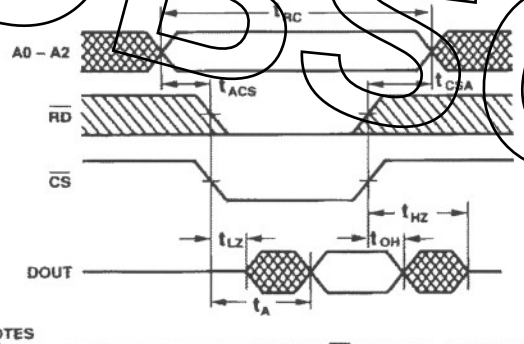
NOTES
$\overline{CS}$ IS VALID BEFORE OR COINCIDENT WITH $\overline{RD}$ HIGH - TO - LOW TRANSITION.
$\overline{CS}$ IS INVALID AFTER OR COINCIDENT WITH $\overline{RD}$ LOW - TO - HIGH TRANSITION.
$\overline{WR}$ IS NOT ACTIVE DURING READ CYCLE.

Figure 1a. Timing Waveform for Read Cycle No. 1 ($\overline{RD}$ Controlled)



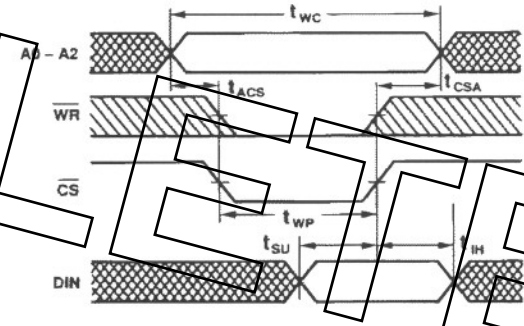
NOTES
$\overline{CS}$ IS VALID BEFORE OR COINCIDENT WITH $\overline{WR}$ HIGH - TO - LOW TRANSITION.
$\overline{CS}$ IS INVALID AFTER OR COINCIDENT WITH $\overline{WR}$ LOW - TO - HIGH TRANSITION.
$\overline{RD}$ IS NOT ACTIVE DURING WRITE CYCLE.

Figure 2a. Timing Waveform for Write Cycle No. 1 ($\overline{WR}$ Controlled)



NOTES
$\overline{RD}$ IS VALID BEFORE OR COINCIDENT WITH $\overline{CS}$ HIGH - TO - LOW TRANSITION.
$\overline{RD}$ IS INVALID AFTER OR COINCIDENT WITH $\overline{CS}$ LOW - TO - HIGH TRANSITION.
$\overline{WR}$ IS NOT ACTIVE DURING READ CYCLE.

Figure 1b. Timing Waveform for Read Cycle No. 2 ($\overline{CS}$ Controlled)



NOTES
$\overline{WR}$ IS VALID BEFORE OR COINCIDENT WITH $\overline{CS}$ HIGH - TO - LOW TRANSITION.
$\overline{WR}$ IS INVALID AFTER OR COINCIDENT WITH $\overline{CS}$ LOW - TO - HIGH TRANSITION.
$\overline{RD}$ IS NOT ACTIVE DURING WRITE CYCLE.

Figure 2b. Timing Waveform for Write Cycle No. 2 ($\overline{CS}$ Controlled)

AC TEST CONDITIONS

Input Pulse Levels	DGND to +3.0 V
Input Rise/Fall Times	<5 ns
Timing Reference Levels	
Inputs	1.5 V
Outputs	
LOW	0.4 V
HIGH	2.4 V
Enabled to LOW	V_T −0.1 V
Enabled to HIGH	V_T +0.1 V
Disabled from LOW	V_{OL} +0.5 V
Disabled from HIGH	V_{OH} −0.5 V

V_T = 1.5 V, the voltage to which 3-stated outputs are forced.

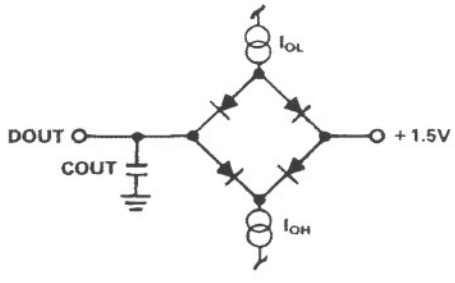


Figure 3. Output Load

AD1341

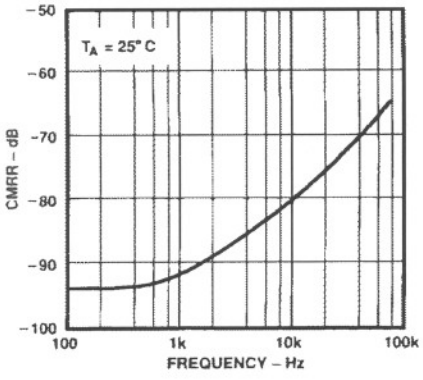


Figure 4. PGIA Common-Mode Rejection vs. Frequency, Gain = 1

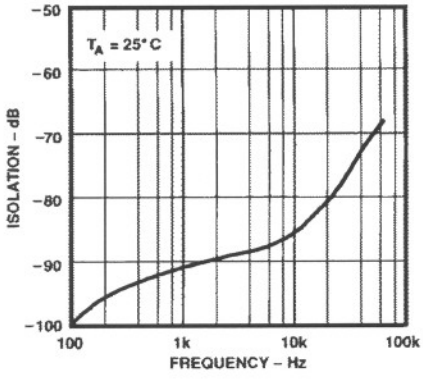


Figure 5. Multiplexer Off Isolation vs. Frequency

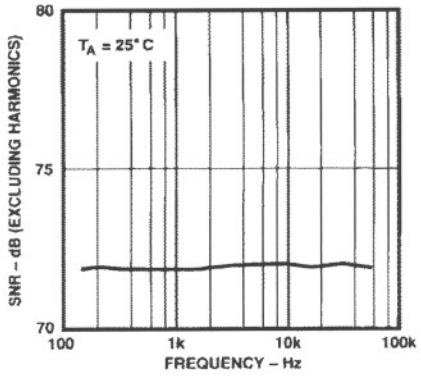


Figure 6. Signal-to-Noise Ratio vs. Frequency, Single Channel, Gain = 1

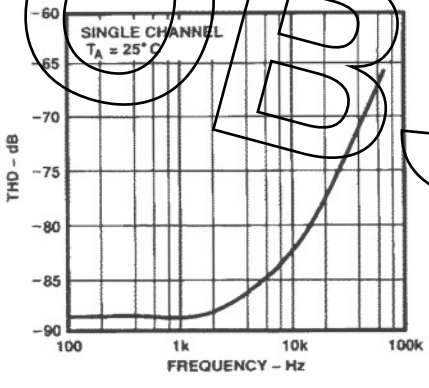


Figure 7. THD vs. Input Frequency, Single Channel, Gain = 1

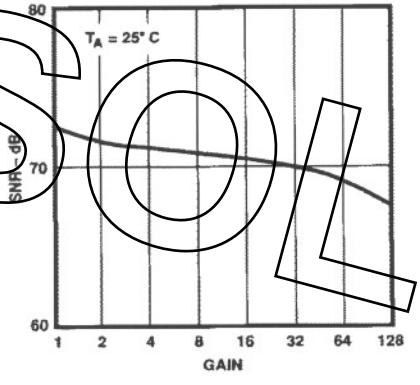


Figure 8. SNR vs. Gain, f_{IN} = 1904 Hz

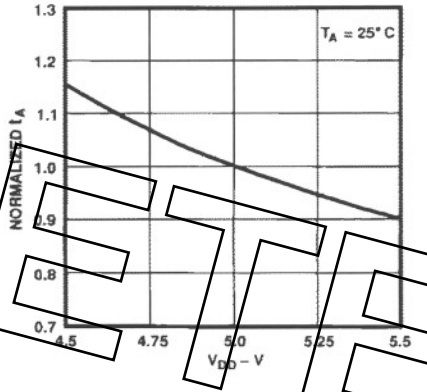


Figure 9. Normalized Data Access Time vs. V_{DD}

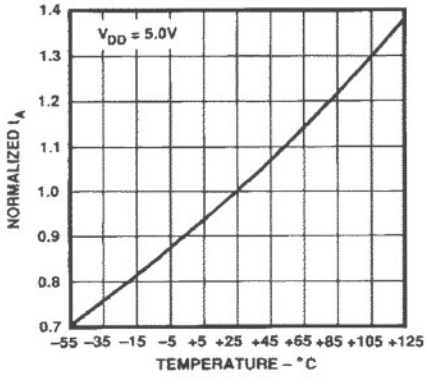


Figure 10. Normalized Data Access Time vs. Temperature

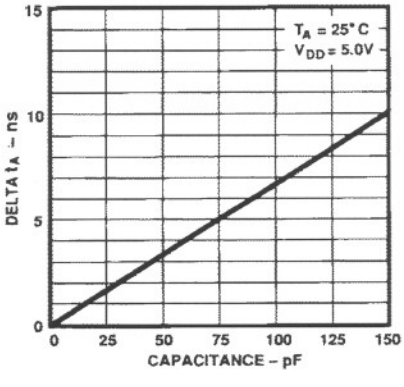


Figure 11. Change in Data Access Time vs. Loading

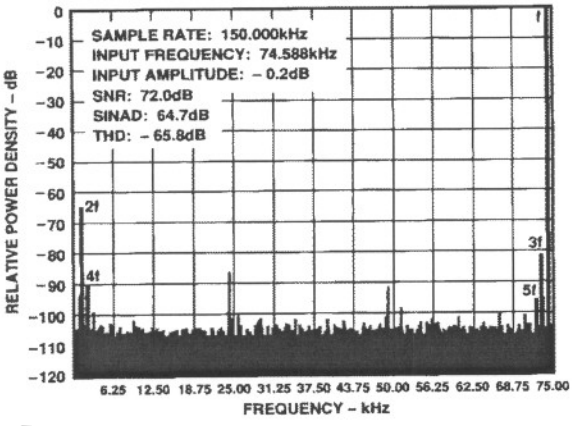


Figure 12. AD1341 Dynamic Performance (Single Channel, Gain = 1)

THEORY OF OPERATION

Functional Overview

The AD1341 is a complete data acquisition system designed with modern processor technology in mind. The heart of the AD1341 is a 12-bit Sampling Analog-to-Digital Converter with a maximum throughput of 150 kHz. The basic 10 V input range may be pin-strapped for either unipolar (0 to +10 V) or bipolar (−5 V to +5 V) operation. The ADC is preceded by a Programmable-Gain Instrumentation Amplifier possessing 8 binary-weighted gains between 1 and 128. Multiplexers provide 16 input channels which can be configured for either single-ended or 8-channel differential operation via a pin-strap option. All multiplexer inputs are fully protected against overvoltage and power-loss conditions. The multiplexer outputs and PGIA inputs are not internally connected to provide maximum flexibility and expansion capability. A +10 V reference output is also available.

The AD1341 offers a wide range of interface and control options. Programming and data readout are performed over a high speed asynchronous parallel 16-bit bus. Conversion results are stored in a 32-word FIFO which can be used to reduce I/O overhead. Six data formats are available. Sampling sequences of up to 32 channel/gain combinations are written to a command

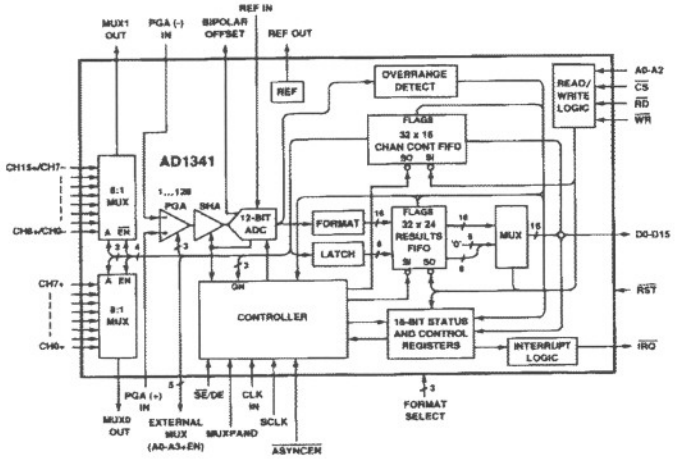


Figure 13. Functional Block Diagram

FIFO. A sampling sequence may be executed just once or may be continued indefinitely using the programmable Repeat mode. The AD1341 also includes expansion outputs which make possible a doubling of the number of input channels using a single external multiplexer. Expanded configurations retain all the operating features of a stand-alone AD1341. The interrupt structure is fully programmable. Status polling is fully supported. Finally, the AD1341 includes an independent programmable 16-bit countdown timer. Figure 13 shows a complete block diagram of the AD1341.

Input Configurations

The AD1341's ADC may be configured for either unipolar or bipolar inputs. Unipolar operation results when Ref Out (Pin 80) is connected to Ref In (Pin 79). BP Off (Pin 78) must be connected to Analog Signal Ground during unipolar operation. Bipolar operation requires the connection of Ref In, Ref Out, and BP Off. An external +10 V reference such as the AD2710 may be used if lower drift is required. A +10.24 V reference will provide a basic LSB size of 2 mV when the PGIA gain is set to 1.

The AD1341's multiplexer outputs and PGA inputs are not connected internally, but are instead brought out to package pins. Several pin-strapping options are possible to tailor the part to meet specific system requirements. The number of input channels may also be doubled with ease by using the AD1341's external multiplexer addressing capabilities.

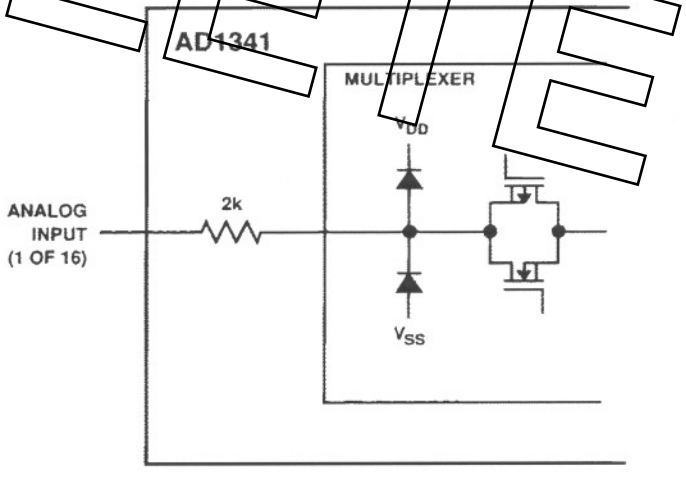


Figure 14. AD1341 Input Protection Circuitry

Single-ended or differential operation is selected using the $\overline{SE}$/DE input. When the MUXPAND input is grounded, the AD1341 can provide either 16 single-ended or 8 differential inputs. The number of inputs may be increased to 32 (single-ended) or 16 (differential) by pulling up the MUXPAND input and using an ADG506A multiplexer. Five expansion outputs enable and address the external multiplexer to give the expanded system the full functionality and programmability of a stand-alone AD1341. The four possible input schemes are shown in Figures 15 through 18, and the required pin-strapping is summarized in Table I.

AD1341

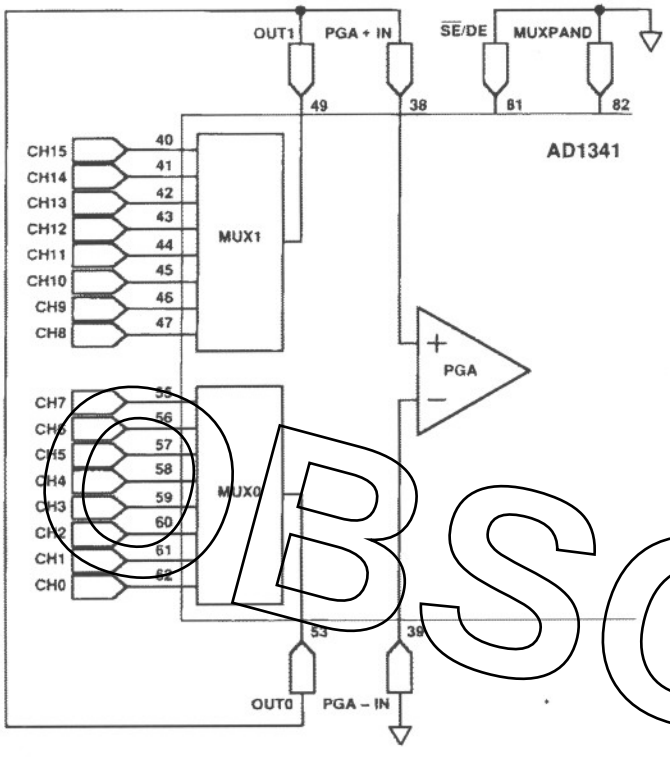


Figure 15. AD1341 Configured for 16 Single-Ended Input Channels

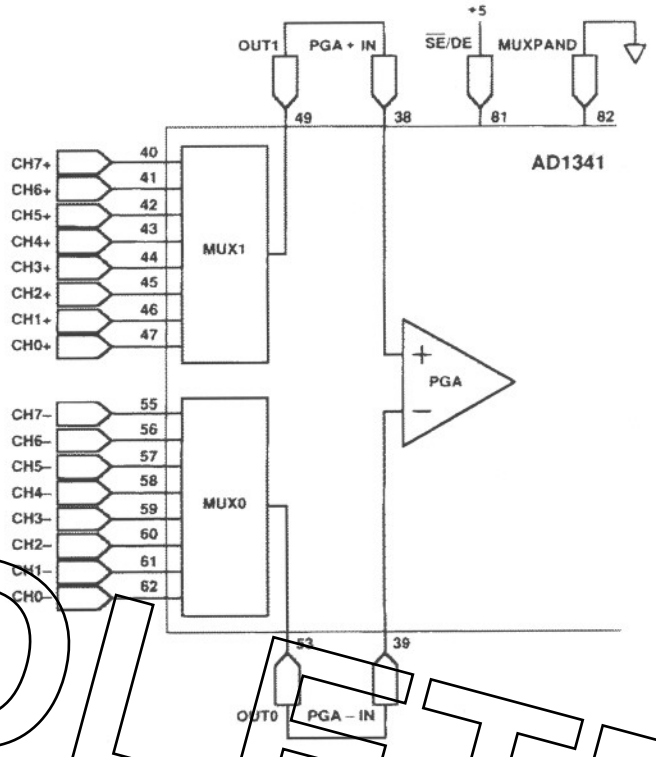


Figure 16. AD1341 Configured for 8 Differential Input Channels

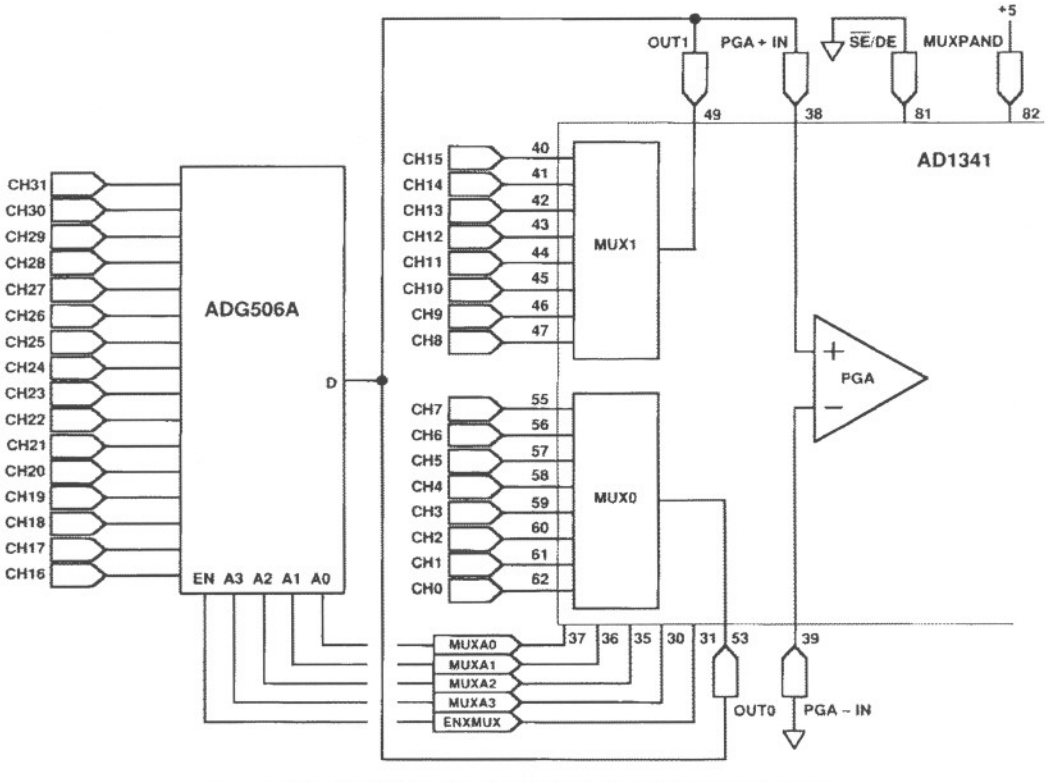


Figure 17. AD1341 with Expansion to 32 Single-Ended Input Channels

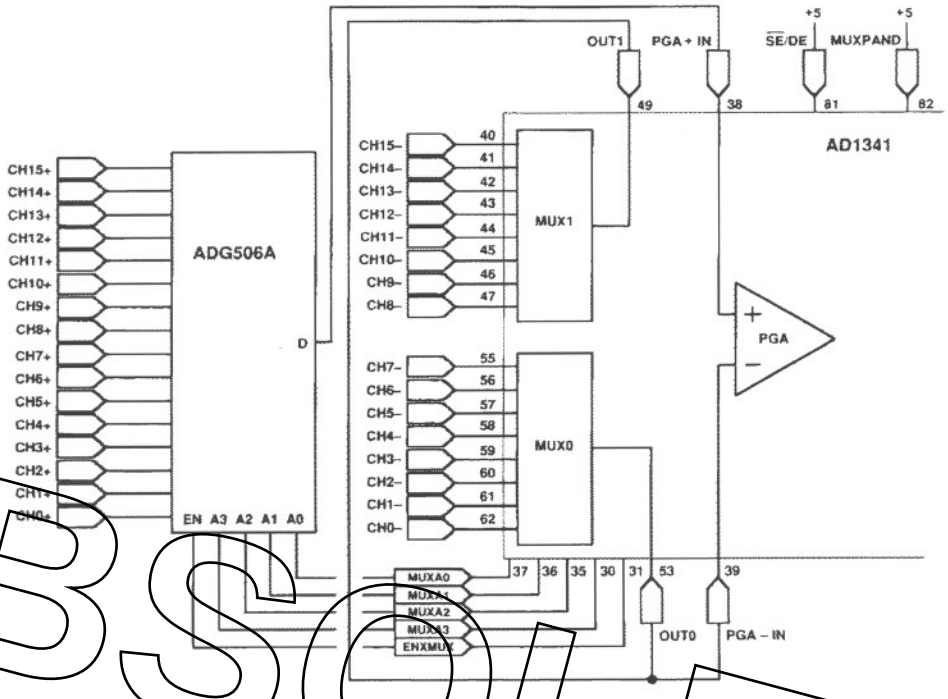


Figure 18. AD1341 with Expansion to 16 Differential Input Channels

	16-Channels Single-Ended	8-Channels Differential	32-Channels Single-Ended	16-Channels Differential
SE/DE	0	1	0	1
MUXPAND	0	0	1	1
MUXOUT1	PGA+IN	PGA+IN	PGA+IN	PGA–IN
MUXOUT0	PGA+IN	PGA–IN	PGA+IN	PGA–IN
ASIGGND	PGA–IN		PGA–IN	
D (ADG506A)			PGA+IN	PGA+IN
EN (ADG506A)			ENXMUX	ENXMUX
A0 (ADG506A)			MUXA0	MUXA0
A1 (ADG506A)			MUXA1	MUXA1
A2 (ADG506A)			MUXA2	MUXA2
A3 (ADG506A)			MUXA3	MUXA3

Table I. Connections for AD1341 Input Options

The AD1341's multiplexer inputs are protected against destructive latchup under power-loss and overvoltage conditions. Each input uses a 2 kΩ current-limiting resistor and two diodes to provide protection to at least 16 V beyond the analog supplies (Figure 14). The expanded input configurations in Figures 17 and 18 maybe similarly protected by adding 2 kΩ resistors in series with each external multiplexer input. Interactions between channels may occur under overload conditions. Unused AD1341 and ADG506A multiplexer inputs must be grounded.

Data Format Selection

Six data formats are available, offering a choice between natural binary and 2s complement coding with left, center, or right justification of the 12-bit result within the 16-bit field. The data format is determined by connections made to the three inputs FMT0, FMT1, and FMT2 (Pins 87, 86, and 85). These connections should be hardwired. Logical 0s are assigned to all unused places in the natural binary formats. The sign bit is extended as required and 0s are forced in empty least-significant places in the 2s complement formats. Tables II and III describe the data formats and their selection.

FMT2	FMT1	FMT0	Output Format
0	0	0	Natural Binary, Left Justified
0	0	1	Natural Binary, Right Justified
0	1	0	Natural Binary, Center Justified
0	1	1	Reserved
1	0	0	2s Complement, Left Justified
1	0	1	2s Complement, Right Justified
1	1	0	2s Complement, Center Justified
1	1	1	Reserved

Table II. Data Format Selection

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Nat Bin, LJ	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	0	0
Nat Bin, CJ	0	0	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0
Nat Bin, RJ	0	0	0	0	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
2s Com, LJ	$\overline{B11}$	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	0	0
2s Com, CJ	$\overline{B11}$	$\overline{B11}$	$\overline{B11}$	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0
2s Com, RJ	$\overline{B11}$	$\overline{B11}$	$\overline{B11}$	$\overline{B11}$	$\overline{B11}$	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

Table III. AD1341 Data Formats. D15 Is Data Bus MSB; B11 Is ADC MSB

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Figure 19 shows the basic connections required for a data acquisition system with 16 single-ended input channels, ±5 V input range, and left-justified 2s complement data.

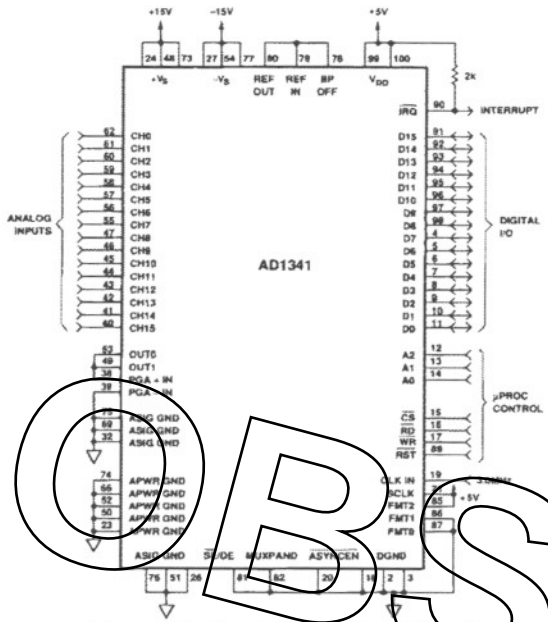

Figure 19. Typical Interface Circuit

Control Structure

The AD1341 is controlled through its digital interface. The device is completely disabled following power-up or a reset and must be programmed before conversions can be initiated.

Conversion sequences are stored in the Channel Control FIFO, from which they are subsequently executed. Each conversion instruction contains both a channel address and a channel gain. The Channel Control FIFO is 32 words deep.

Execution of programmed conversion sequences is enabled via the Mode Control Register. This register is also used to perform a programmed reset, to enable or disable interrupts, Repeat mode, and the timer, and to choose the system timing option. Selection from among a wide range of interrupt options is governed by the contents of the Interrupt Mask Register. Register contents may be read back for verification. A 32-word FIFO provides buffering for conversion results. The AD1341's register address space is defined in Table IV.

A2	A1	A0	Register Name/Function	Mnemonic	Type
0	0	0	Channel Control FIFO	CCR	R/W
0	0	1	Conversion Result FIFO	CRR	R
0	1	0	Reserved		
0	1	1	Reserved		
1	0	0	Mode Control Register	MCR	R/W
1	0	1	Timer Register	TMR	R/W
1	1	0	Interrupt Mask Register	IMR	R/W
1	1	1	Status Register	STS	R

Table IV. AD1341 Addresses

REGISTER DESCRIPTIONS

Channel Control Register (CCR)

The CCR is a 16-bit read/write register. Up to 32 CCR words may be written to the Channel Control queue for subsequent execution. The CCR contains a channel address and an associated gain. This information can be read back after the conversion is complete and the conversion result has been read out. The CCR bits are as follows (the MSB is B15):

CCR Description

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Name	0	0	0	0	0	GN2	GN1	GN0	0	0	0	A4	A3	A2	A1	A0

Bits GN2 through GN0 control the PGIA gain. GN0 is the LSB. Gains are binary weighted, ranging from 1 to 128. A gain code of 000 corresponds to a gain of 1 and a gain code of 111 produces a gain of 128. Any channel may be programmed for any gain. A4 through A0 are channel address bits. A0 is the LSB. The range of available addresses depends upon the input configuration, which is determined by the wiring of the $\overline{SE}$/DE and MUXPAND inputs. Address ranges are outlined in Table V. Address bits invalid for the chosen input configuration must be written as 0s. Bits outside the gain and address fields are ignored during writes and set to 0 during reads.

Input Configuration	$\overline{SE}$/DE	MUXPAND	Valid Address Range
8-Channel Differential	1	0	0–7
16-Channel Single-Ended	0	0	0–15
16-Channel Differential	1	1	0–15
32-Channel Single-Ended	0	1	0–31

Table V. AD1341 Address Ranges

The CCR should be read only *after* reading a conversion result from the CRR (see below). Reading the CRR causes the related CCR data to be stored in a temporary register. The contents of this register are presented on the data bus during a subsequent CCR read. If the first CCR read is not performed before the second CRR read, the gain and channel information associated with the first CRR result will be lost.

Conversion Result Register (CRR)

The CRR is a 16-bit read-only FIFO register. The results of conversions are stored in the CRR up to 32 words deep. The results can be read out sequentially without reading the CCR in between, but the channel and gain information for the previous result will be discarded. In the descriptions below R0–R11 represent the conversion result and SE represents sign-extension bits. These will be the same as R11 for 2s complement numbers and are 0 for natural (unsigned) binary numbers.

CRR Description—Left Justified

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Name	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0	0	0

CRR Description—Center Justified

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Name	SE	SE	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	0

CRR Description—Right Justified

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Name	SE	SE	SE	SE	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0

Overrange and underrange results in natural binary format are coded as twelve 1s and twelve 0s, respectively, and are positioned within the 12-bit field as determined by the selected

justification. Twos complement overranges and underranges are represented as 0111 1111 1111 and 1000 0000 0000, respectively. These results will also be properly justified and sign-extended.

Mode Control Register (MCR)
The MCR is a 16-bit read/write register. It contains six active bits. The reset (default) state for all bits is 0.

MCR Description

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Name	INT	0	RST	0	CVN	0	REP	0	TIM	0	ACC	0	0	0	0	0

INT enables or disables the interrupt mask register (IMR). Interrupt generation under IMR control is enabled when INT is set to 1. New interrupts are disabled when INT is set to 0, but any interrupts pending when INT was set to 0 are not affected.

RST provides a programmed AD1341 reset. Writing a 1 to RST causes all registers and FIFOs to be reset to their default states. RST remains set until the reset sequence is complete, at which time it is cleared. A reset sequence requires one complete clock cycle and may take up to 667 ns (assuming a 3 MHz clock) depending upon the timing of the MCR write relative to the system clock.

CVN enables or disables conversions under host control. Setting CVN begins the execution of the conversion sequence stored in the CCR. Clearing CVN prevents the initiation of further conversions; any in-process conversion(s) will be completed and the conversion results written to the CRR. An in-process conversion is one for which the gain and channel instruction has been clocked out of the CCR. CVN may be set again anytime after it has been cleared; any conversions still in the CCR will resume in an orderly fashion.

REP enables the Repeat mode when set to 1. This bit may be set at any time. Setting REP disables any further writing to the CCR. Once REP has been set, the data written into the CCR queue since the last read will be repeated in a circular fashion. If Repeat mode is enabled after conversions have begun only the unexecuted conversions in the CCR queue will be repeated. Repeat mode functions with any number of instructions in the CCR queue. Clearing REP clears the CCR queue and the controller in preparation for receiving new data and starting new conversions.

TIM is used to disable or enable the 16-bit internal timer. The timer is disabled when TIM is set to 0, and enabled when TIM is set to 1. When enabled the counter counts down from the count stored in the TMR and generates an interrupt (if the timer interrupt is enabled). The preset count is then reloaded from the TMR and another countdown cycle begins on the next clock edge. Clearing TIM will halt the timer and clear its count. The contents of the TMR are not affected by clearing TIM. If the timer is enabled after having been disabled, it will begin its countdown from the previously programmed count. A Terminal Count signal is available on Pin 22.

ACC permits selection between standard and accelerated system timing (see *Conversion Timing*). Standard timing is selected when ACC is set to 0, and accelerated (optimized) timing is selected when ACC is set to 1.

Timer Register (TMR)
The TMR is a read/write register used to load and query the general purpose timer. Writing to the TMR will program a time delay value. The delay time is given by

delay time = programmed count × basic delay unit.

The basic delay unit is one clock period, or 333.3 ns with a 3.00 MHz clock, and the maximum delay is 65535 basic delay units. T15 is the MSB. The reset (default) state for the TMR is 0. There may be an uncertainty of 1 clock period on the first countdown interval after the timer is enabled. All subsequent timer intervals will be identical and equal to the programmed delay provided timer operation is not interrupted.

TMR Description

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Name	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0

Reading the TMR will give the current programmed value. Reads are supported only when the timer is disabled. It is not possible to read the timer status during timer operation.

Interrupt Mask Register (IMR)
The IMR is a 16-bit read/write register. Setting bits in the IMR determines the conditions used to generate an interrupt to the host processor. The desired interrupt condition(s) is set by writing a 1 to the appropriate bit(s); all other IMR bits must be written as 0s. The reset (default) state for the IMR is all bits 0.

IMR Description

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Name	0	CVD	CVP	TME	0	ORG	0	CCF	CCH	CCE	0	0	0	CRF	CRH	CRE

Set IMR bits have the following effects:

CVD will cause an interrupt to be asserted every time a conversion result is shifted into the CRR.

CVP will cause an interrupt to be asserted when the conversion result obtained by executing the last command in the CCR is shifted into the CRR. The condition for a CVP interrupt is sensed at the scheduled start of the "last" conversion (see *Conversion Timing*). Writing another command to the CCR prior to the scheduled start of the "last" conversion will block the CVP interrupt.

TME will cause an interrupt to be asserted when the timer count reaches zero.

ORG will cause an interrupt to be asserted whenever overrange data are shifted into the CRR.

CCF will cause an interrupt to be asserted when the CCR queue is full. The CCR depth is 32 words.

CCH will cause an interrupt to be asserted when the CCR queue is at least half full (contains at least 16 words).

CCE will cause an interrupt to be asserted when the last channel/gain command is shifted out of the CCR and the conversion programmed therein begins. It is this conversion which leads to a CVP interrupt if no further commands are written to the CCR.

CRF will cause an interrupt to be asserted when the CRR is full. The CRR depth is 32 words.

CRH will cause an interrupt to be asserted when the CRR is at least half full.

CRE will cause an interrupt to be asserted when the CRR is empty.

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Status Register (STS)

The Status Register is a 16-bit read only register which provides a continuous summary of the AD1341's internal state. The default condition for all STS bits is transparent. When an interrupt condition is enabled, the STS will latch the corresponding bit upon the assertion of the enabled interrupt; all other bits remain transparent. *The interrupt will remain asserted until the processor reads the STS contents; any latched STS bits will be reset to transparent mode once the read operation is completed.* Any pending interrupt conditions will continue the interrupt request once the STS register is read. The EVT bit is set whenever any of the unmasked interrupt conditions has generated an interrupt request.

STS Description

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Name	EVT	CVD	CVP	TME	0	ORG	0	CCF	CCH	CCE	0	0	0	CRF	CRH	CRE

STS bits correspond to IMR bits with the exception of EVT. STS bits have the following meanings:

EVT is set whenever an enabled interrupt event has occurred. This bit cannot be cleared directly by the user and remains set until the interrupt has been serviced.

CVD is set whenever a conversion is completed.

CVP is set whenever the conversion pipeline (CCR queue) is empty.

TME is set when the timer expires.

ORG is set when overrange or underrange data are shifted into the CCR.

CCF is set when the CCR queue has been filled.

CCH is set when the CCR queue is at least half full.

CCE is set when the CCR queue has been emptied.

CRF is set when the CRR FIFO is full.

CRH is set when the CRR FIFO is at least half full.

CRE is set when the CRR FIFO is empty.

Some of the remaining STS bit positions are used for diagnostic purposes. These bits (B11, B9, B5, B4, and B3) should be masked during normal operation.

FIFO Boundary Conditions

Overflow conditions occur whenever more than 32 words are written to either the CCR or the CRR. In both cases, data beyond the 32nd word are lost. The first 32 data words are not affected.

An underflow condition occurs when more than 32 words are read out of the CRR. The last valid word remains in the CRR and will be placed on the bus repeatedly in response to additional read commands. The CCR queue cannot underflow. Conversions cease after the last command in the CCR has been read and executed when Repeat mode is disabled.

Conversion Timing

The AD1341 normally overlaps some of its signal processing functions to maximize throughput. Such pipelining provides maximum throughput when multiple conversion instructions are buffered in the CCR and executed sequentially using the internal controller. Externally triggered conversions are also possible, either with or without pipelining. Finally, the internal timer may be used in conjunction with external triggering to further customize the sampling rate.

Pipelined Conversions

Normal pipelined operation is enabled by grounding the $\overline{\text{ASYNCEN}}$ input (Pin 20) and tying the SCLK input to V_{DD}. In this mode the AD1341's timing is governed by its internal controller. Channel and gain instructions for conversion N+1 are read from the CCR and executed at the start of A/D conversion N. This permits the PGIA's settling to occur during the A/D conversion. The AD1341's throughput depends on the number of channels and the gain mix because of the variation in PGIA settling time with gain. The internal sequencer always provides the proper settling time for the active channel regardless of the number of channels used or the gains selected.

There are two sequencer modes, Standard and Accelerated, selected using the ACC bit (Bit 5) in the MCR. Standard timing mode increases both the SHA acquisition time and the PGIA settling time for higher gains. Accelerated mode maintains constant SHA acquisition time independent of gain and provides maximum system throughput. Table VI details throughput performance for the two timing modes. The listed throughputs assume all channels operate at the same gain.

	Standard Mode		Accelerated Mode	
Gain	Clocks per Pipelined Conversion	Throughput, Pipelined (kHz)	Clocks per Pipelined Conversion	Throughput, Pipelined (kHz)
1–8	20	150.00	20	150.00
16	40	75.00	30	100.00
32	80	37.50	52	57.69
64	160	18.75	102	29.41
128	320	9.38	202	14.85

Table VI. AD1341 Timing and Throughput (3 MHz Clock)

When Repeat mode is enabled, the instructions in the CCR are read and executed indefinitely in a circular fashion. The per-channel sampling rate in Repeat mode for arbitrary numbers of channels and various gains can be determined with a simple calculation. This calculation uses the "Clocks per Pipelined Conversion" data from Table VI and the programmed channel and gain mix. Each channel is sampled at the calculated rate, while the exact sample time will be determined by the specific channel and gain order. The example below an assumes input expansion as shown in Figure 17.

11 channels at gains between 1 and 8	$11 \times 20 = 220$ clock periods
8 channels at gain of 16	$8 \times 30 = 240$ clock periods
5 channels at gain of 32	$5 \times 52 = 260$ clock periods
2 channels at gain of 64	$2 \times 102 = 204$ clock periods
4 channels at gain of 128	$4 \times 202 = 808$ clock periods
30 channels	1732 clock periods

$$\textit{System sample rate} = \frac{1}{1732 \times 333.33\ ns} = 1.73210\ kHz$$

Calculation of System Sample Rate (Accelerated Timing Mode, 3 MHz Clock)

It is also possible to measure the system sample rate by counting the number of clock periods between successive rising edges of the CC output. CC goes high at the start of the last conversion in a sequence and remains high until that conversion is completed. CC does not toggle when a single conversion is repeated. The duty cycle of CC depends on the number of channels in a sequence and their gains. Transitions of CC occur on rising clock edges.

Externally Triggered Conversions

Conversions may be triggered directly by the host system when $\overline{\text{ASYNCEN}}$ is tied to V_{DD}. *Externally triggered conversions may only be used with Repeat mode enabled.* Channel and gain information must first be written to the CCR. After all CCR writes are completed, REP (MCR Bit 9) should be set by the host processor. This clocks out the first CCR instruction, setting the multiplexer address and PGIA gain. A subsequent rising edge on the SCLK input places the SHA into Hold mode and triggers the A/D conversion, which is clocked to its completion using the 3 MHz clock. The first rising clock edge following the rising edge of SCLK also clocks the next channel/gain word from the CCR, permitting the pipelining of externally triggered conversions. The typical setup time for SCLK high relative to the rising edge of the clock is 10 ns.

The AD1341's acquisition timing controller is inoperative when $\overline{\text{ASYNCEN}}$ is tied high, so the host system must provide sufficient time to acquire each input before pulsing the SCLK line. Failure to do so will produce an incorrect conversion result. The minimum time required for a given gain may be found using the "Clocks per Pipelined Conversion" columns of Table VI. Externally triggered conversions have an inherent timing uncertainty of 1 clock period (333.3 ns with a 3 MHz clock) when SCLK is not synchronized with the external clock.

SCLK functions much like the Start-Convert input of a standard ADC. Unlike a conventional ADC, however, the AD1341 lacks a $\overline{\text{BUSY}}$ or STATUS output. The IMR may be programmed to cause an interrupt at the completion of each conversion, which will make the $\overline{\text{IRQ}}$ output functionally similar to a traditional $\overline{\text{BUSY}}$ or STATUS output. All AD1341 interrupt conditions function normally with externally-triggered conversions.

Timer-Controlled Conversions

The AD1341's programmable timer may be used to control externally triggered conversions, making possible extremely low sample rates with minimal host overhead. *Timer-controlled conversions may only be used with Repeat mode enabled.* TC (Pin 22) should be connected to SCLK (Pin 21), and the timer must be programmed to generate a delay at least equal to the largest required number of "Clocks per Pipelined Conversion" from Table VI.

MCR Bits 7 and 9 should be set after the CCR and TMR have been programmed. This will clock out the first CCR instruction and start the timer. The first input channel is sampled and the A/D conversion begins with first rising edge of the TC output, which indicates the end of the timer interval. This edge also clocks the next instruction from the CCR, reloads the timer delay stored in the TMR, and restarts the timer. A conversion is performed every time the timer expires until the AD1341 is reprogrammed or reset.

Single Conversions

Repeat must be disabled to perform a single conversion. The desired channel and gain must first be written to the CCR. Setting CVN (MCR Bit 11) will begin the conversion under internal timing control when $\overline{\text{ASYNCEN}}$ is low. The times required to perform the acquisition and conversion of a single sample are listed in Table VII; these times are measured from the first rising clock edge after CVN has been set. The typical setup time for CVN (trailing edge of $\overline{\text{WR}}$ to rising edge of CLK) is 10 ns.

Because acquisition and conversion begin on a clock edge rather than precisely when CVN is set, there may be an uncertainty in the instant at which the input is sampled. The variation will be up to one clock period in systems in which bus operation is not synchronous with the AD1341's 3 MHz clock, and one clock period (333 ns) should be added to the contents of Table VII to account for this. These variations can be eliminated when the host system's bus is synchronized with the 3 MHz clock provided CVN's setup time is met.

Gain	Standard Mode Conversion Time, µs	Accelerated Mode Conversion Time, µs
1–8	11.00	11.00
16	17.67	15.00
32	31.00	23.33
64	57.67	40.00
128	111.00	73.33

Table VII. AD1341 Conversion Times (3 MHz Clock, $\overline{\text{ASYNCEN}}$ Low)

With $\overline{\text{ASYNCEN}}$ high, single conversions may be triggered externally. The channel and gain instruction is clocked from the CCR when REP is set, and signal acquisition begins at that time. The rising edge of SCLK places the SHA into Hold mode, and the A/D conversion begins on the first rising clock edge following the SCLK transition. Table VIII lists the minimum permissible acquisition times between setting CVN and the rising edge of SCLK, along with the time required for the actual A/D conversion. The total conversion time is the sum of Table VIII's acquisition time and A/D time.

	Standard Mode		Accelerated Mode	
Gain	Acquisition Time, µs	A/D Time, µs	Acquisition Time, µs	A/D Time, µs
1–8	6.67	4.33	6.67	4.33
16	13.33	4.33	10.67	4.33
32	26.67	4.33	19.00	4.33
64	53.33	4.33	35.67	4.33
128	106.67	4.33	69.00	4.33

Table VIII. AD1341 Timing and Throughput (3 MHz Clock)

There is an uncertainty of one clock period in *both* the acquisition and A/D times listed in Table VIII when system operation is asynchronous. The first of these uncertainties arises from the variable relationship between the trailing edge of $\overline{\text{WR}}$ with respect to the rising edge of CLK, while the second results from the timing uncertainty between the rising edges of CLK and SCLK.

APPLICATIONS

Analog Interface

Each of the AD1341's 16 multiplexer inputs is protected against overvoltage and power-loss conditions by a series resistor and two diodes (Figure 14). Each input's time constant is typically 50 ns when the AD1341 is strapped for differential inputs and 100 ns in the single-ended configuration. The settling delays caused by these time constants have been accounted for in the AD1341's internal timing generator. Additional external series resistance will increase these time constants and could prevent the inputs from settling within the time allotted. For this reason the AD1341's inputs are best driven by low-impedance sources such as op amp outputs.

AD1341

The AD1341's multiplexer outputs and PGIA inputs are brought out of the package to permit easy system expansion. Excessive capacitance at these pins should be avoided as it will also interfere with settling. All connections should be kept as short and direct as possible to minimize capacitance and noise coupling. (The AD1341's timing generator allows sufficient input settling time with the capacitance added by the expansion multiplexer as shown in Figures 17 and 18.)

A small amount of charge is dumped through each input whenever it is selected or deselected. The magnitude of this charge is typically 4 pC. Each signal source should have a low output impedance at high frequencies in order to absorb this transient. Micropower op amps may have difficulty with this type of transient because of their generally higher output impedances and lower gain-bandwidth products. The AD711, AD712, and AD713 are good choices for driving the AD1341's inputs.

Each multiplexer input requires a return path for off-state leakage currents. The driving source normally supplies this path. Unused inputs must not be left floating and should be connected to the analog ground plane.

Power Supplies and Grounds

Proper grounding and power supply bypassing techniques are necessary to obtain the AD1341's specified performance. The AD1341 has separate connections for analog signal ground, analog power ground, and digital ground. All Analog Signal and Power Ground pins must be connected to a common ground plane beneath the AD1341. This will provide the low impedance path required to minimize coupling between dynamic supply currents and low level signals being processed by the AD1341.

The AD1341's metal lid is internally connected to Analog Power Ground to provide maximum shielding against electrical interference. The lid faces the circuit board when the AD1341 is soldered in place. The board surface directly beneath the AD1341 should not contain signal or power traces to eliminate the possibility of short circuits. Using this area as a ground plane will result in the lowest possible ground impedance and will preserve signal fidelity.

The Digital Ground pins should also be connected to this ground plane if at all possible. This will provide the greatest immunity to digital switching noise. If this causes ground loops or other system-level problems then a separate ground plane or other low impedance return path must be provided. In this case the analog and digital grounds should be connected together at the AD1341 using back-to-back Schottky diodes and a good high frequency bypass capacitor. Ceramic capacitors in the range 0.01–0.1 μF are recommended. These components will prevent destructive dc potential differences between grounds and will also provide a low impedance path for transient currents.

Each power supply should be capacitively bypassed to the ground plane(s) with the capacitors located as closely as possible to the device in order to provide a low source impedance for dynamic signal and supply currents. Both ceramic and solid tantalum capacitors should be used for each supply. Appropriate values are 0.01–0.1 μF for ceramic capacitors and 1–10 μF for tantalum capacitors. Aluminum electrolytic capacitors have much higher equivalent series resistance than comparable-value tantalum devices and are not recommended.

Digital Interface

The AD1341's fast parallel bus simplifies the system designer's task by permitting zero-wait-state operation in most applications. In many cases the interface between the AD1341 and a microprocessor requires nothing more than an address decoding function. Figures 20 through 23 illustrate the AD1341's interface with several popular single-chip digital signal processors.

The AD1341's digital interface provides TTL- and CMOS-compatible levels with 10K ECL speed, exhibiting typical edge rates of 1.4 ns with 15 pF loading. Proper layout and impedance

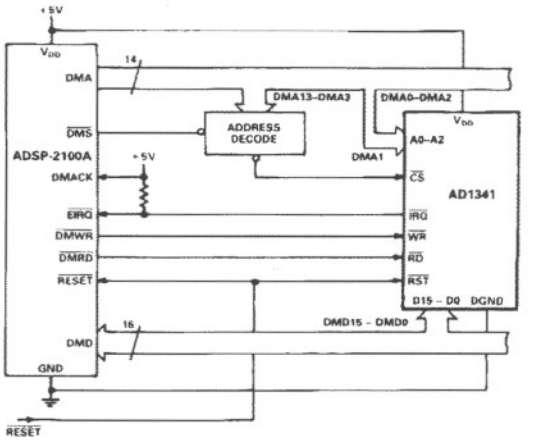


Figure 20. ADSP-2100A to AD1341 Interface

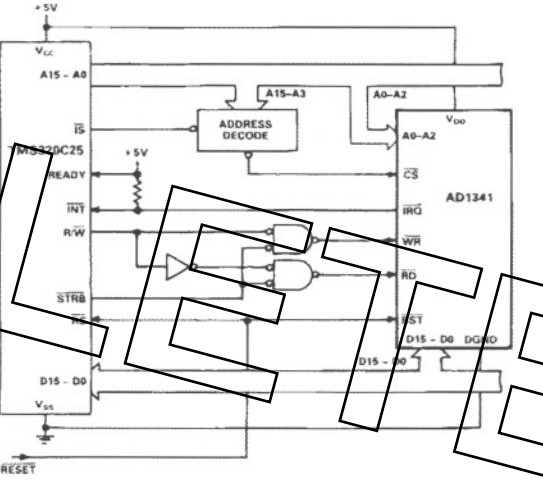


Figure 21. TMS320C25 to AD1341 Interface

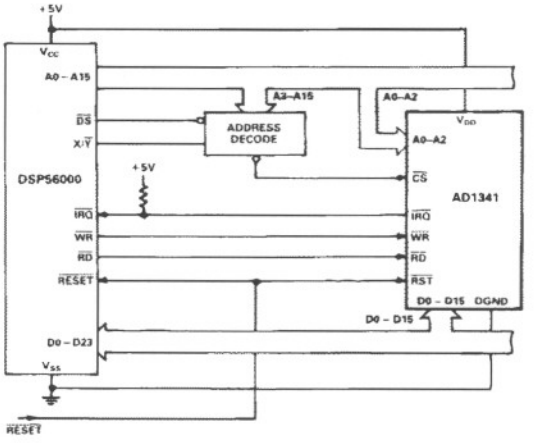


Figure 22. DSP56000 to AD1341 Interface

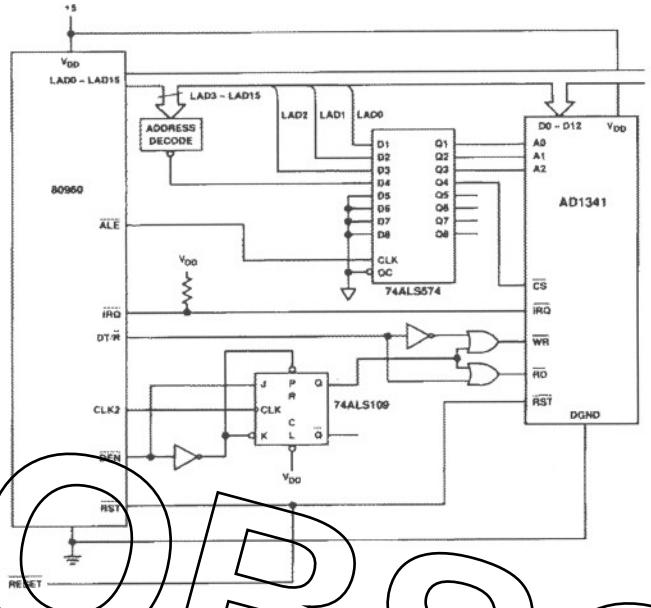


Figure 23. 80960 to AD1341 Interface

matching techniques are essential to prevent problems caused by crosstalk, reflections, and ground bounce.

Crosstalk

The fast edge rates and large voltage swings in CMOS systems will cause capacitive and inductive coupling (crosstalk) between adjacent PCB circuit traces. This will compromise signal integrity and reduce noise margins. The effect is most severe on "clocked" control lines ($\overline{RD}$, $\overline{WR}$, and $\overline{CS}$) which are close to data lines. The coupled noise may be large enough to initiate spurious I/O operations.

Crosstalk can be reduced by eliminating long parallel PCB circuit traces and by routing data lines away from clocked control lines. Grounded circuit traces may also be used to provide shielding between data and control lines, but this is less effective than physical separation.

Reflections

The gross impedance mismatches between high impedance CMOS inputs, low impedance CMOS outputs, and typical PCB circuit trace impedances can lead to voltage reflections and ringing. Reflections from impedance discontinuities become important whenever the line's round-trip delay exceeds the driving signal's rise or fall time. The critical line length, beyond which reflections begin to play a role, is only 13 cm for the AD1341, assuming an edge rate of 1.4 V/ns and a line delay of 0.055 ns/cm. The critical line length can be increased by running the signal lines over a ground plane because the added capacitance will reduce the edge rate (at the expense of increasing ground bounce).

A much better solution is to provide proper terminations for all signal lines. The AD1341's CMOS outputs do not have sufficient current drive capability to permit terminating PCB lines in their characteristic impedance. Series damping is a satisfactory alternative means to reduce reflections and ringing. A small resistor (typically 10 Ω to 75 Ω) is placed in series with the signal line as close to the signal source as possible. The goal is to match the driver's output resistance plus the series resistance to the line impedance. This will absorb any wave reflected back towards the source.

The primary disadvantage of series termination is that the line impedance and terminating resistor form a voltage divider network and the voltage along the line may lie between valid logic levels during the line's two-way propagation delay time. This means that while any number of device inputs may be connected at the end of the line, device inputs which require valid logic levels during the propagation delay time cannot be distributed along the line.

The Application Note "Systems Design Considerations When Using Cypress CMOS Circuits," published by Cypress Semiconductor Corporation, provides in-depth analysis and discussion of various line-matching techniques.

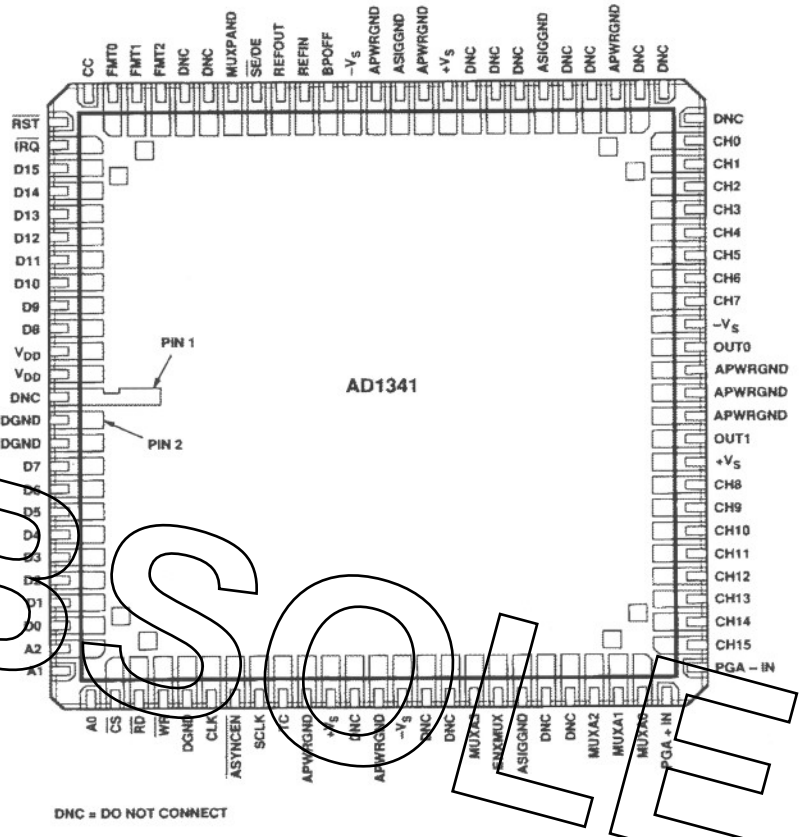
Ground Bounce

Large transient currents will flow into digital ground whenever one or more of the AD1341's data bus outputs switches from high to low (or from high impedance to low when the previous bus data were high). These currents result from the discharge of parasitic capacitances associated with the data bus. Inductance in the ground return path creates a resonant L-C circuit with the parasitic capacitances, resulting in ringing in "ground" at the device relative to "ground" at the supply or elsewhere in the system. The amplitude and duration of this ringing, or "ground bounce" depends on the amount of parasitic reactance. Both the amplitude and duration of the ringing increase as the inductance or capacitance increase.

The effect of ground bounce is to degrade the logic-low noise margin. This can result in system data errors. In particularly severe cases it can initiate spurious I/O operations in the AD1341 and cause the loss of data. The best defenses against ground bounce are to minimize the capacitive loading of the data bus and to use a ground plane to provide a low impedance return path for the inevitable transient currents. When large bus capacitance is unavoidable, it may prove beneficial to use BiCMOS bus transceivers between the AD1341 and the system data bus. This will increase both read and write cycle times, but the controlled edge speeds will reduce the peak currents, decreasing the possibility of erroneous data or I/O operations. The transceivers should be located close to the AD1341 to minimize the capacitance seen by the AD1341's data outputs.

AD1341

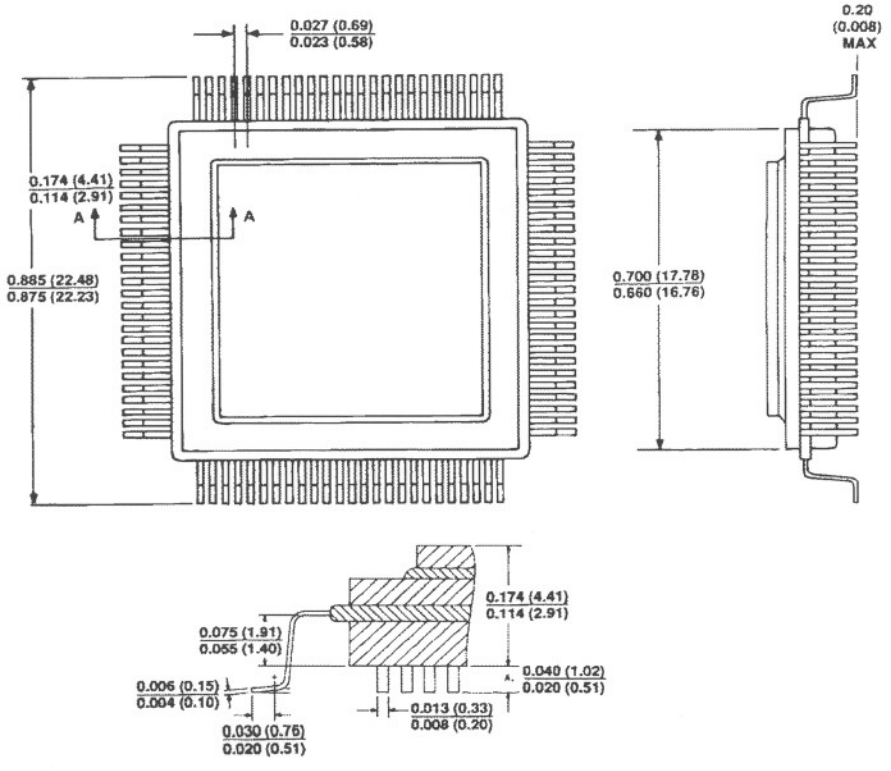
PIN ASSIGNMENTS



DNC = DO NOT CONNECT

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm.)



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