To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

DATA SHEET

THYRISTORS

5P4J,5P4J-Z,5P4J-ZK,5P6J,5P6J-Z,5P6J-ZK

5 A MOLD THYRISTOR

The 5P[ ]J, 5P[ ]J-Z, and 5P[ ]J-ZK are a P gate all diffused mold type Thyristor granted 5 A On-state Average Current (T_C = 95°C) with rated voltages up to 400 V or 600 V.

<R> FEATURES

- Suitable for capacitor discharge applications with high pulse current rating.
- $I_{GT} \leq 200\ \mu A$
- Employs flame-retardant epoxy resin for casing (UL94V-0).
- Surface mounting (Z and ZK)

<R> APPLICATIONS

- Contact-less switch for electronic devices, ignition devices, electronic household appliances and other light industry equipment

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Printed in Japan

The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

MAXIMUM RATINGS

<R>

CHARACTERISTICS	SYMBOL	5P4J, 5P4J-Z, 5P4J-ZK	5P6J, 5P6J-Z, 5P6J-ZK	UNIT	REMARK
Non-repetitive Peak Reverse Voltage	V_{RSM}	500	700	V	R_{GK} = 1 kΩ
Non-repetitive Peak Off-state Voltage	V_{DSM}	500	700	V	R_{GK} = 1 kΩ
Repetitive Peak Reverse Voltage	V_{RRM}	400	600	V	R_{GK} = 1 kΩ
Repetitive Peak Off-state Voltage	V_{DRM}	400	600	V	R_{GK} = 1 kΩ
Average On-state Current	$I_{T(AV)}$	5 (T_C = 95°C, θ = 180°, Single phase half wave)		A	See Fig. 11
Effective On-state Current	$I_{T(RMS)}$	8		A	
Surge On-state Current	I_{TSM}	65 (f = 50 Hz, sine half wave, 1 cycle)		A	See Fig. 2
Fusing Current	$\int i_T^2 dt$	20 (1 ms ≤ t ≤ 10 ms)		A^2s	–
Critical Rate Rise of On-state Current	dI_T/dt	50		A/μs	–
Peak Gate Power Dissipation	P_{GM}	2 (f ≥ 50 Hz, Duty ≤ 10%)		W	See Fig. 3
Average Gate Power Dissipation	$P_{G(AV)}$	0.2		W	
Peak Gate Forward Current	I_{FGM}	1 (f ≥ 50 Hz, Duty ≤ 10%)		A	–
Peak Gate Reverse Voltage	V_{RGM}	6		V	–
Junction Temperature	T_j	−40 to +125		°C	–
Storage Temperature	T_{stg}	−55 to +150		°C	–

<R> ELECTRICAL CHARACTERISTICS (T_j = 25°C, R_{GK} = 1 kΩ)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Repetitive Peak Reverse Current	I_{RRM}	V_{RM} = V_{RRM}	T_j = 25°C	–	–	100	μA
			T_j = 125°C	–	–	2	mA
Repetitive Peak Off-state Current	I_{DRM}	V_{DM} = V_{DRM}	T_j = 25°C	–	–	100	μA
			T_j = 125°C	–	–	2	mA
Critical Rate Rise of Off-state Voltage	dV_D/dt	V_{DM} = 2/3 V_{DRM}, T_j = 125°C		–	3	–	V/μs
On-state Voltage	V_{TM}	I_{TM} = 10 A		–	–	1.6	V
Gate-trigger Current	I_{GT}	V_{DM} = 6 V, R_L = 100 Ω		–	–	200	μA
Gate-trigger Voltage	V_{GT}	V_{DM} = 6 V, R_L = 100 Ω		–	–	0.8	V
Gate Non-trigger Voltage	V_{GD}	V_{DM} = 1/2 V_{DRM}, T_j = 125°C		0.2	–	–	V
Holding Current	I_H	V_{DM} = 24 V, I_{TM} = 10 A		–	1	–	mA
Circuit Commuted Turn-off Time	t_q	I_{TM} = 3 A, V_R ≥ 25 V V_{DM} = 2/3 V_{DRM}, dI_R/dt = 15 A/μs dV_D/dt = 3 V/μs, T_j = 125°C		–	80	–	μs
Thermal Resistance	$R_{th(j-c)}$	Junction to case DC		–	–	3	°C/W
	$R_{th(j-a)}$	Junction to ambient DC **Note**		–	–	62.5	

Note Mount on 0.7 x 7.5 cm^2 ceramic substrate

TYPICAL CHARACTERISTICS

Fig. 1 $i_T - V_T$ CHARACTERISTICS

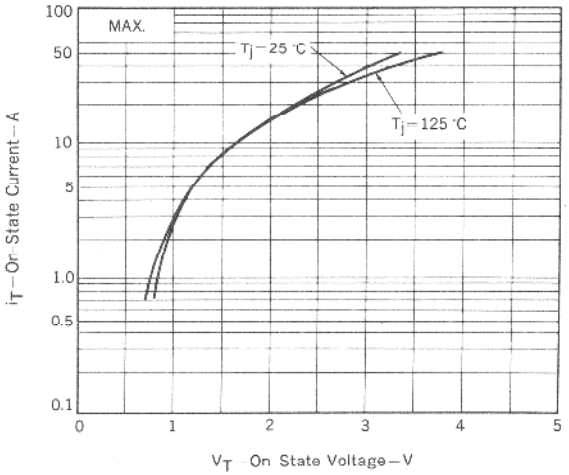

Fig. 2 I_{TSM} RATING

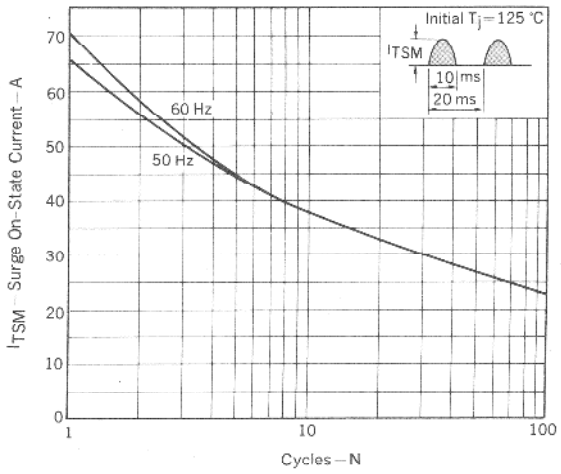

Fig. 3 $V_G - I_G$ RATING

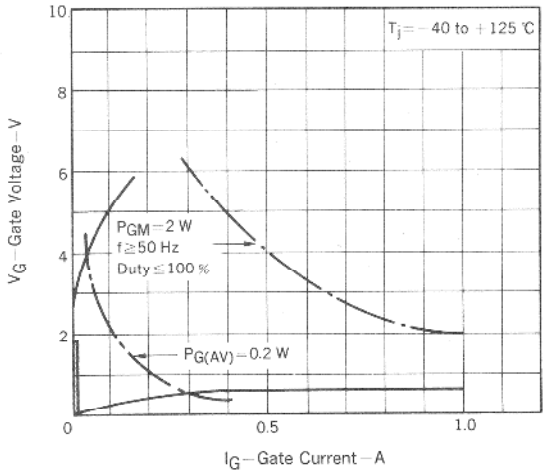

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Fig. 4 $V_{GT} - I_{GT}$ CHARACTERISTIC

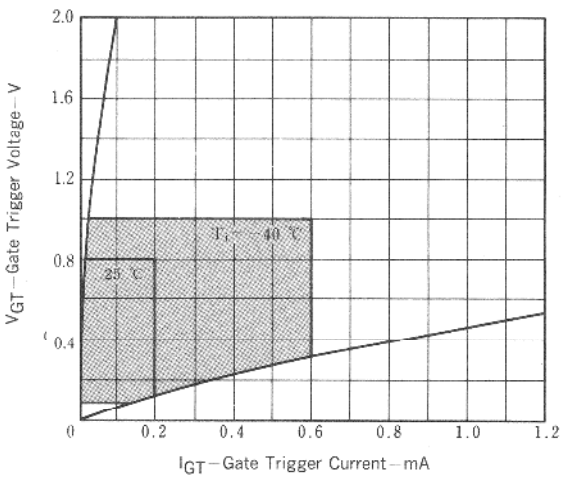

Fig. 5 $I_{GT} - T_a$ TYPICAL DISTRIBUTION

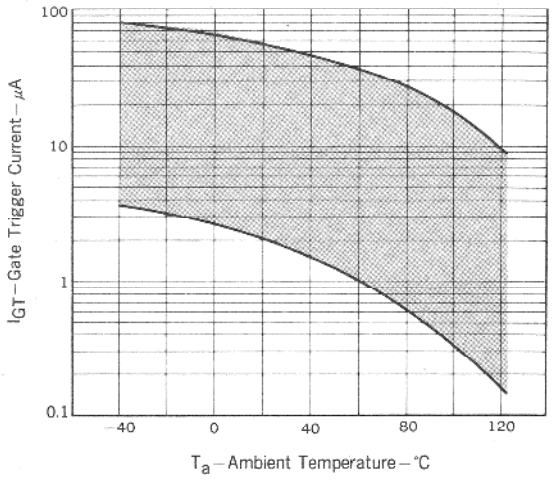

Fig. 6 $V_{GT} - T_a$ TYPICAL DISTRIBUTION

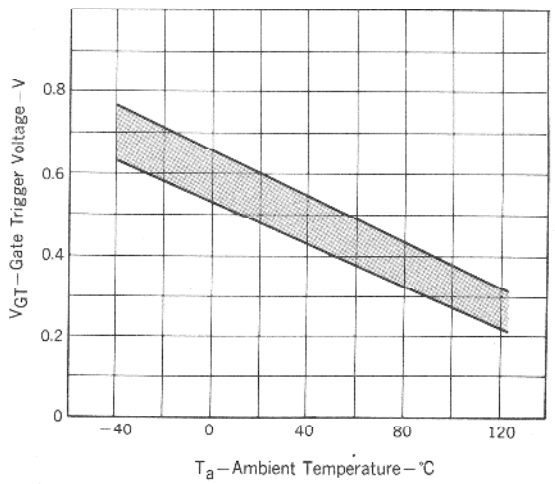

Fig. 7 $I_{GT} - \tau$ TYPICAL DISTRIBUTION

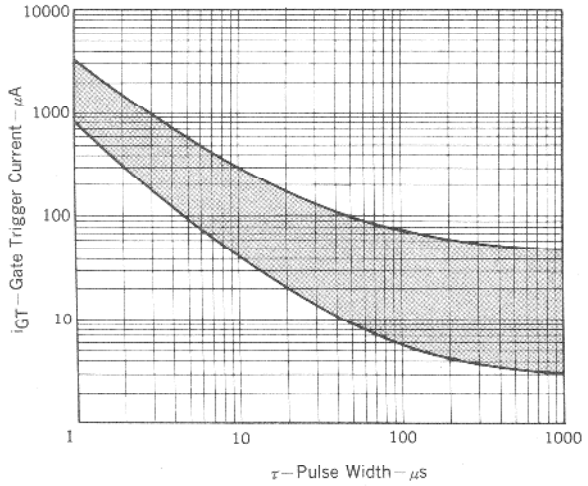

Fig. 8 $v_{GT} - \tau$ TYPICAL DISTRIBUTION

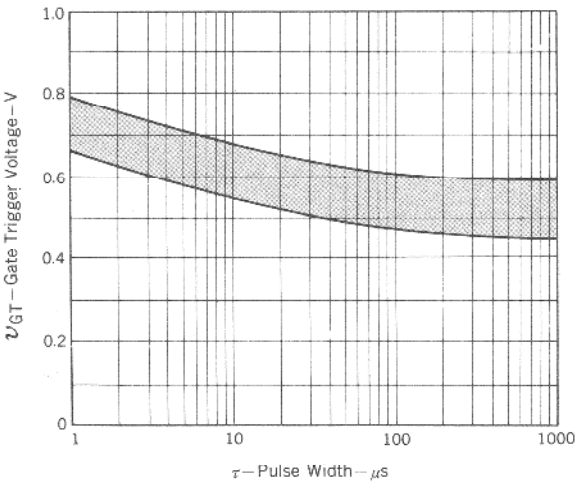

Fig. 9 $I_H - T_a$ TYPICAL DISTRIBUTION

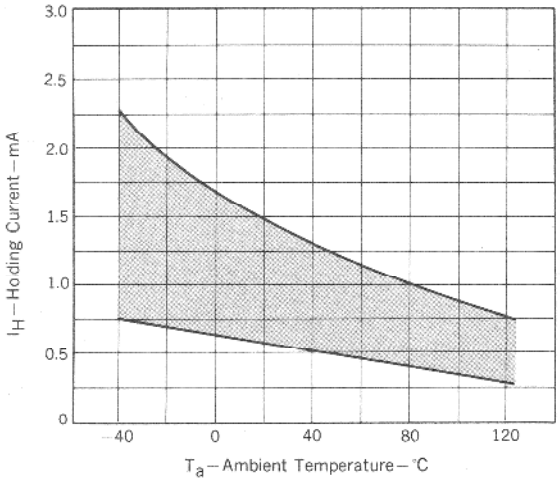

Fig. 10 $P_{T(AV)} - I_{T(AV)}$ CHARACTERISTIC

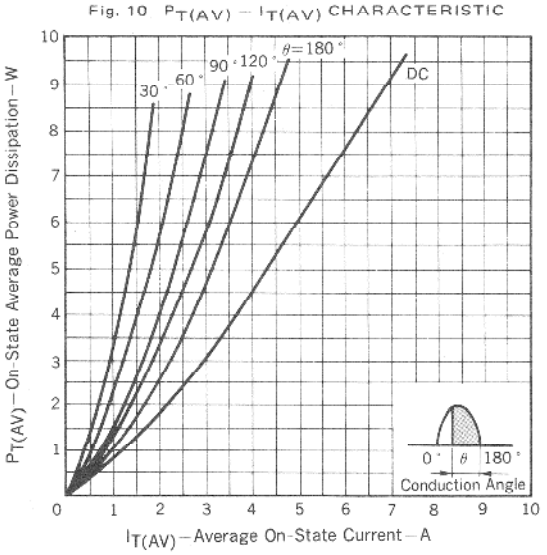

Fig. 11 $T_c - I_{T(AV)}$ RATING

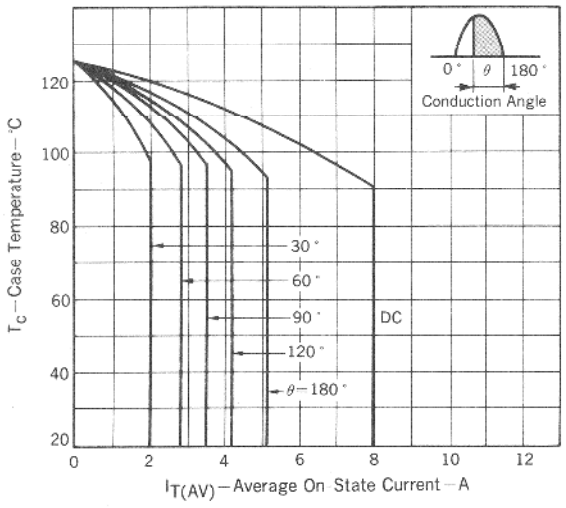

Fig. 12 $T_a - I_{T(AV)}$ RATING

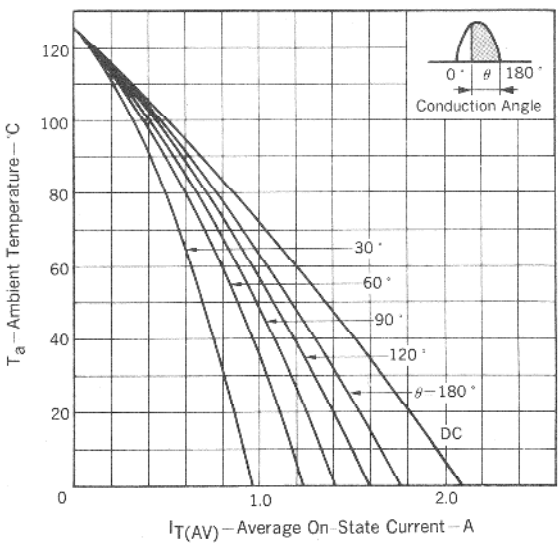

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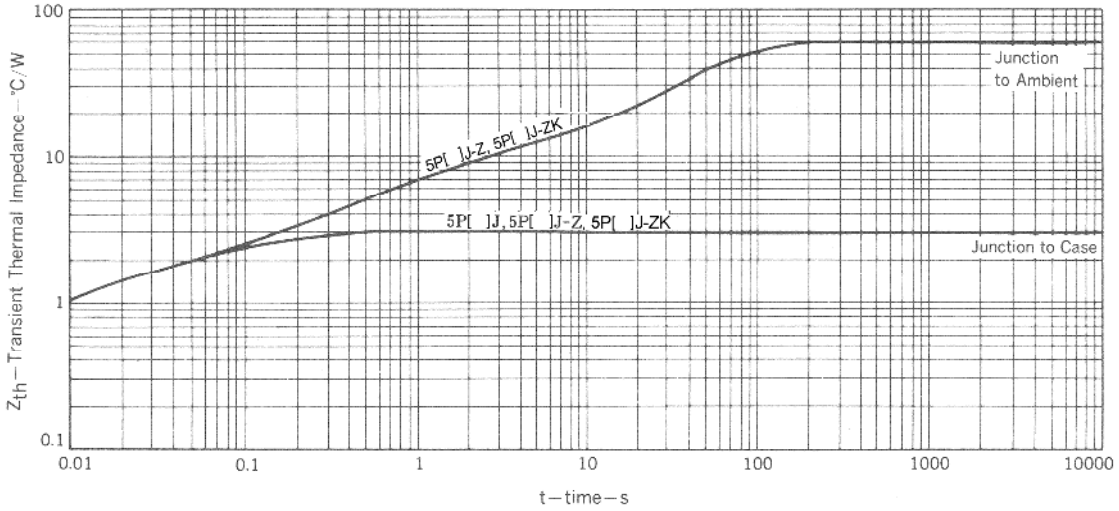
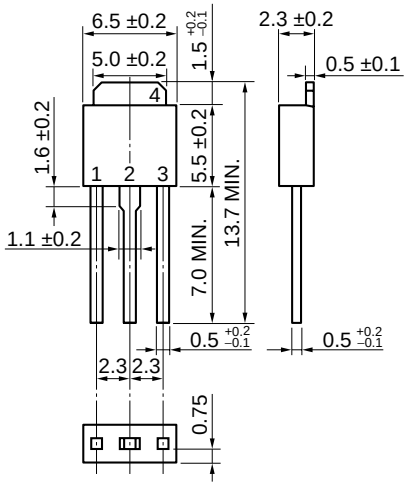
Fig. 13 Z_{th} CHARACTERISTIC



<R> **PACKAGE DRAWING (Unit: mm)**

▪ **5P[ ]J**

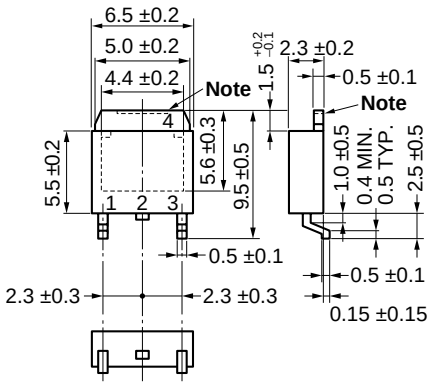


Pin Connection

1. Cathode
2. Anode
3. Gate
4. Fin (Anode)

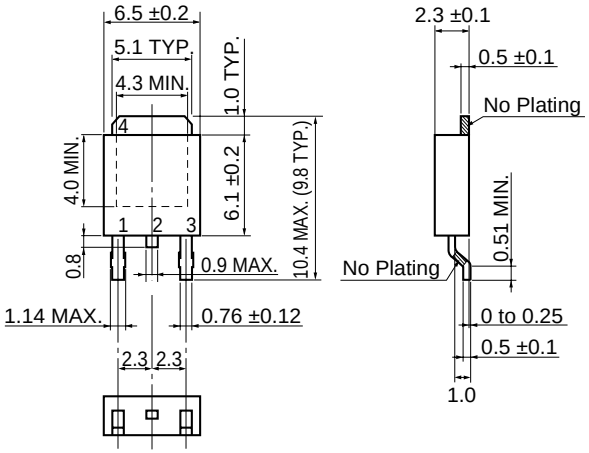
Standard weight: 0.3 g

▪ **5P[ ]J-Z**



Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

▪ **5P[ ]J-ZK**



Pin Connection

1. Cathode
2. Anode
3. Gate
4. Fin (Anode)

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