16-Bit, 4-Channel, CCD/CMOS Sensor Analog Front-End with LED Driver

Check for Samples: VSP5620, VSP5621, VSP5622

FEATURES

- **Four-Channel CCD/CMOS Signal: 2-Channel, 3-Channel, and 4-Channel Selectable**
- **Power Supply: 3.3 V Only, Typ (Built-in LDO, 3.3 V to 1.8 V)**
- **Maximum Conversion Rate:**
  - **VSP5620: 35 MSPS**
  - **VSP5621: 50 MSPS**
  - **VSP5622: 70 MSPS**
- **16-Bit Resolution**
- **CDS/SH Selectable**
- **Maximum Input Signal Range: 2.0 V**
- **Analog and Digital Hybrid Gain:**
  - **Analog Gain: 0.5 V/V to 3.5 V/V in 3/64-V/V Steps**
  - **Digital Gain: 1 V/V to 2 V/V in 1/256-V/V Steps**
- **Offset Correction DAC: ±250 mV, 8-Bit**
- **Standard LVDS/CMOS Selectable Output:**
  - **LVDS:**
    - **Data Channel: 2-Channel**
    - **Clock Channel: 1-Channel**
    - **8-Bit/7-Bit Serializer Selectable**
  - **CMOS: 4 Bits × 4**
- **Timing Generator**
  - **Fast Transfer Clock: One Signal**
  - **Slow Transfer Clock: One Signal**
- **LED Driver: Three Channels**
  - **Current: 60-mA/Channel Max, 16-Steps/Channel**
- **Timing Adjustment Resolution: t_{MCLK}/48**
- **Input Clamp/Input Reference Level Internal/External Selectable**
- **Reference DAC: 0.5 V, 1.1 V, 1.5 V, 2 V**
- **SPI™: Three-Wire Serial**
- **GPIO: Four-Port**
- **Power (at 4-channel, LVDS, 3.3 V, without LED Driver):**
  - **VSP5620: 320 mW at 35 MSPS**
  - **VSP5621: 406 mW at 50 MSPS**
  - **VSP5622: 523 mW at 70 MSPS**

APPLICATIONS

- **Copiers**
- **Facsimile Machines**
- **Scanners**

DESCRIPTION

The VSP5620/21/22 are high-speed, high-performance, 16-bit analog-to-digital-converters (ADCs) that have four independent sampling circuit channels for multi-output charge-coupled device (CCD) and complementary metal oxide semiconductor (CMOS) line sensors. Pixel data from the sensor are sampled by the sample/hold (SH) or correlated double sampler (CDS) circuit, and are then converted to digital data by an ADC. Data output is selectable in low-voltage differential signaling (LVDS) or CMOS modes.

The VSP5620/21/22 include a programmable gain to support the pixel level inflection caused by luminance and a built-in light-emitting diode (LED) driver to adjust the brightness. The integrated digital-to-analog-converter (DAC) can be used to adjust the offset level for the analog input signal. Furthermore, the timing generator (TG) is integrated in these devices for the control of sensor operation.

The VSP5620/21/22 use 1.65 V to 1.95 V for the core voltage and 3.0 V to 3.6 V for I/Os. The core voltage is supplied by a built-in low-dropout regulator (LDO).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VSP5621RSLR	ACTIVE	VQFN	RSL	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 85	VSP 5621	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

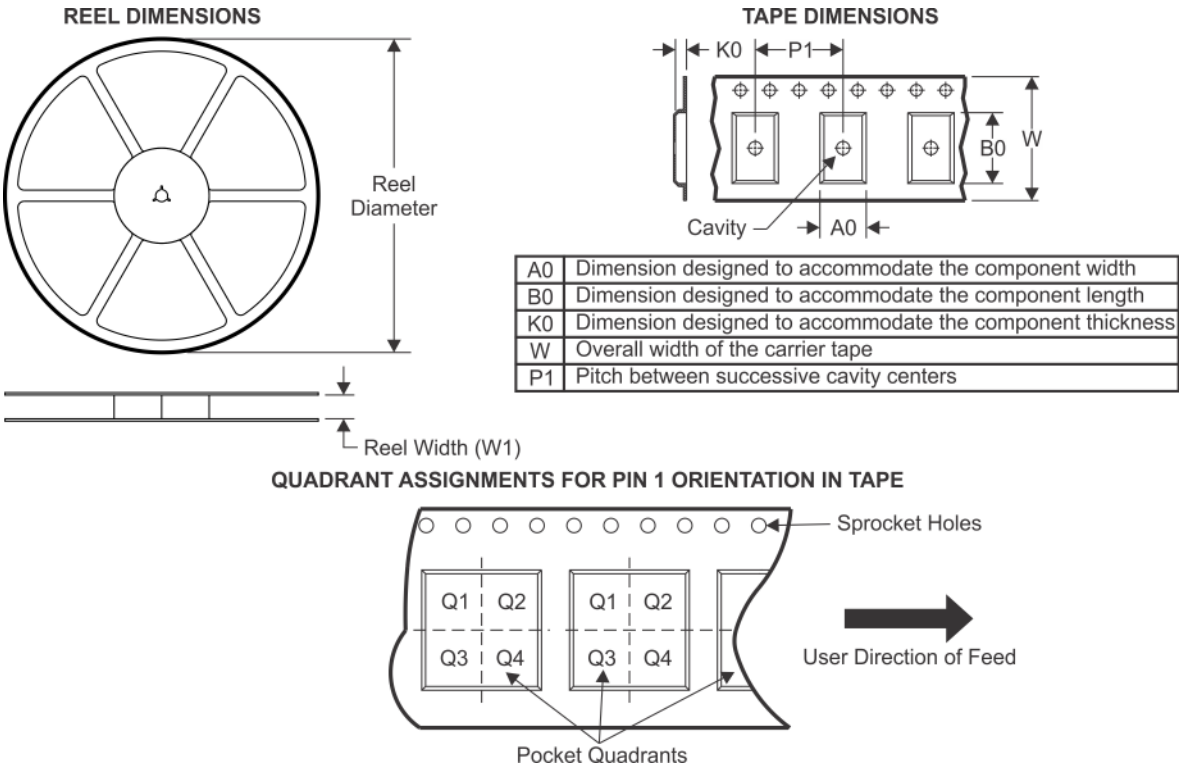
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

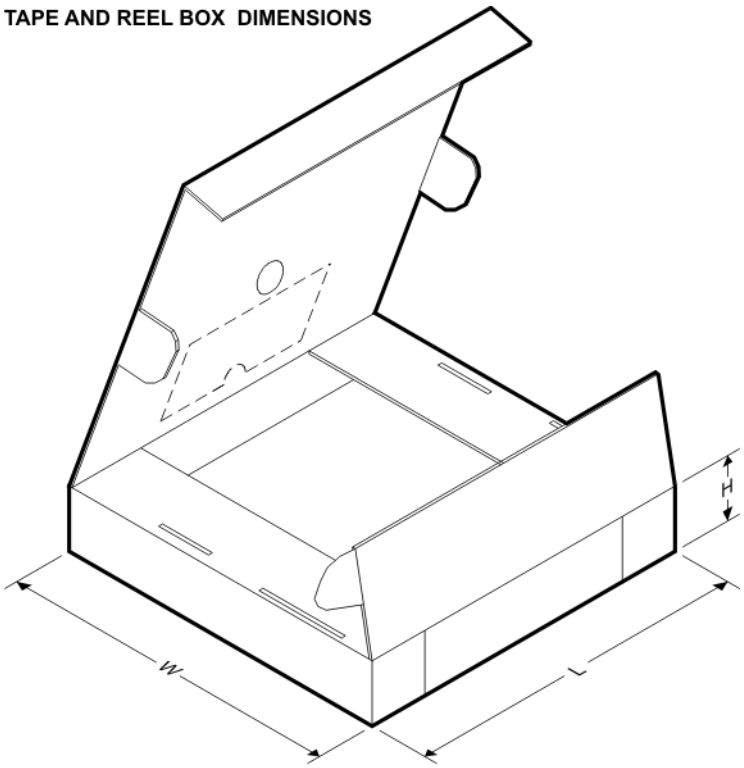


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VSP5621RSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

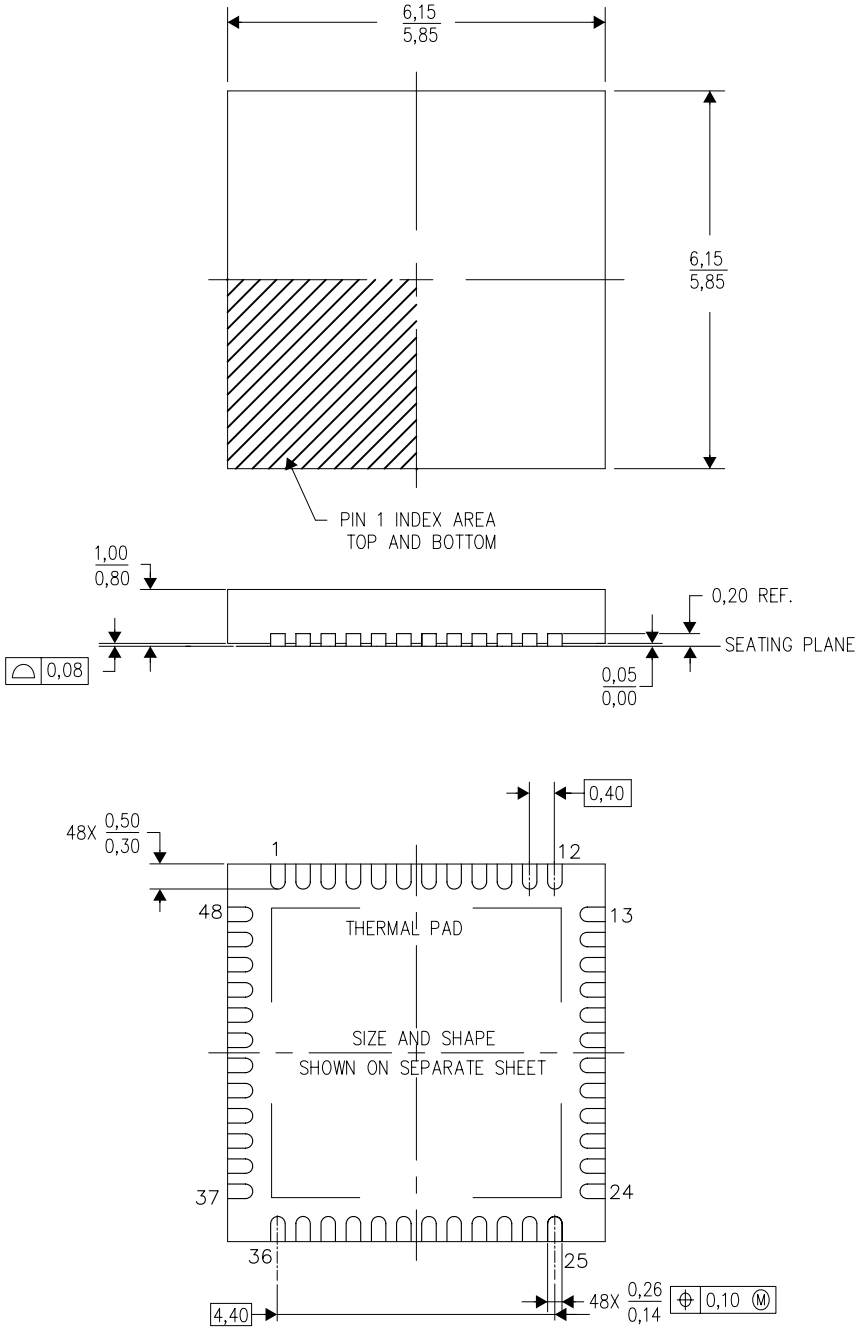
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VSP5621RSLR	VQFN	RSL	48	2500	367.0	367.0	38.0

RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



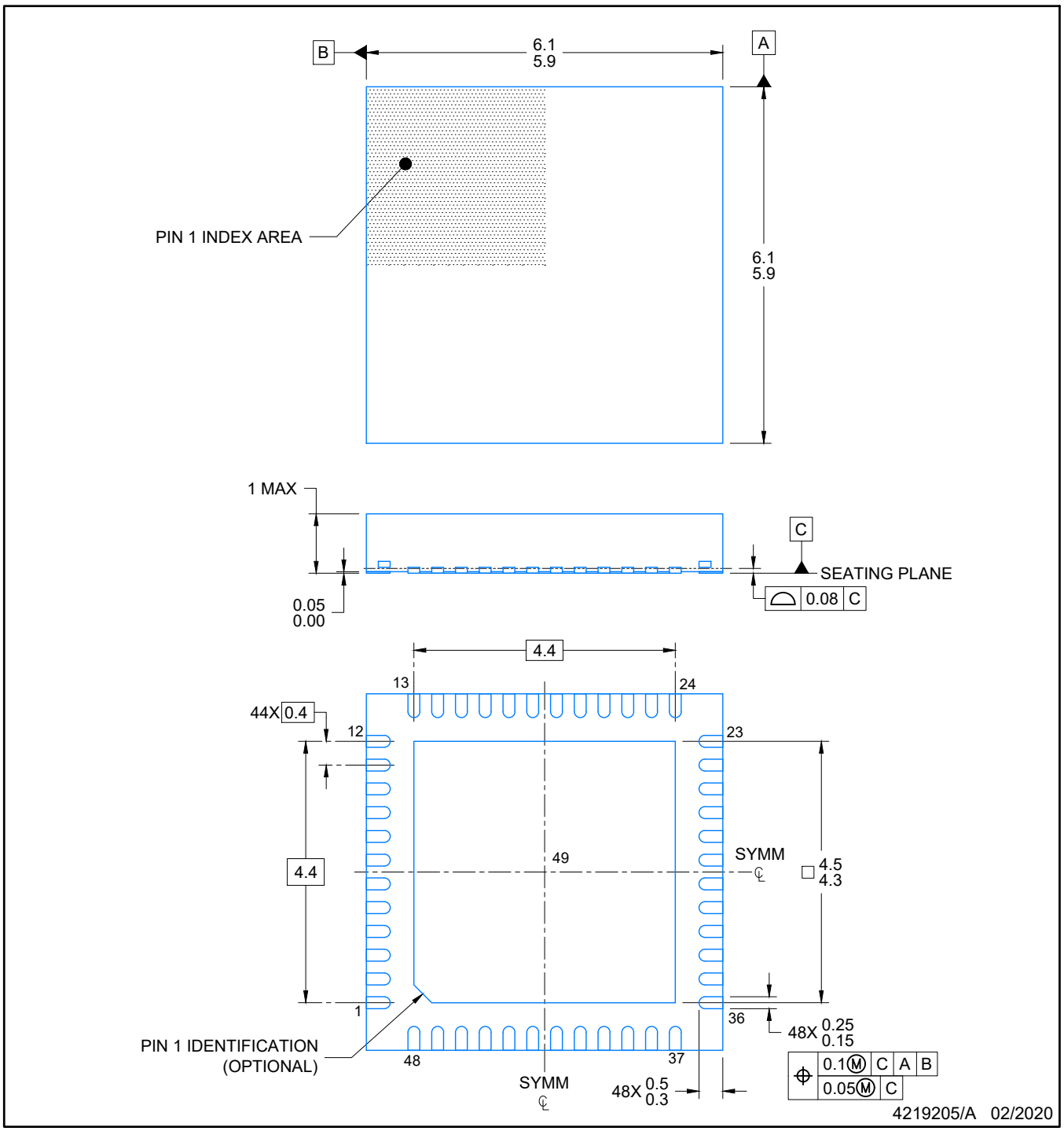
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

PACKAGE OUTLINE

RSL0048B

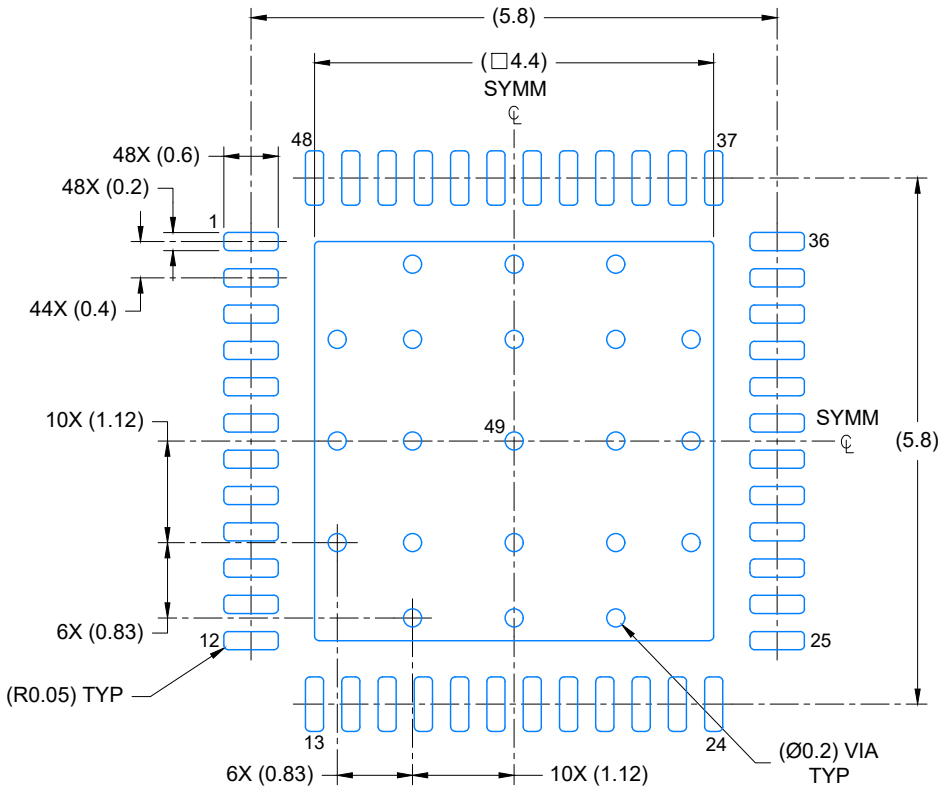
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

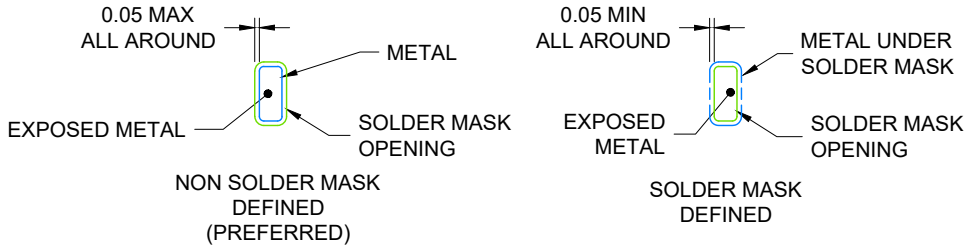


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

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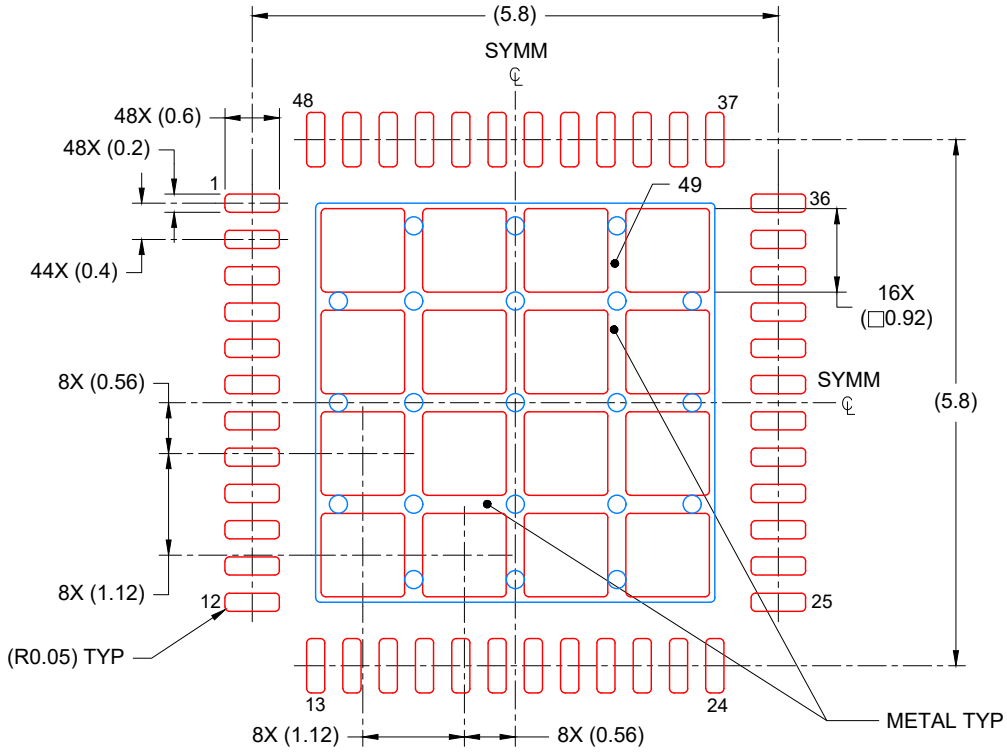
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
70% PRINTED COVERAGE BY AREA
SCALE: 12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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