19-5295; Rev 0; 6/10

Microsemi

MAX3612 Evaluation Kit

Evaluates: MAX3612

General Description

The MAX3612 evaluation kit (EV kit) is a fully assembled and tested demonstration board that simplifies evaluation of the MAX3612 low-jitter clock generator. The EV kit includes an on-board 25MHz crystal and switches for selecting different modes of operation. The reference inputs and clock outputs use SMA connectors and are AC-coupled to simplify connection to test equipment.

EV Kit Contents

- **MAX3612 EV Kit Board**

Features

- **Fully Assembled and Tested**
- **On-Board 25MHz Crystal**
- **Switches for Selecting Modes of Operation**
- **SMA Connectors and AC-Coupled Clock I/Os**

Ordering Information

PART	TYPE
MAX3612EVKIT+	EV Kit

+Denotes lead(Pb)-free and RoHS compliant.

Component List

DESIGNATION	QTY	DESCRIPTION
C1–C10, C14, C15, C16, C18–C24, C27–C32, C35, C36, C37	29	0.1µF ±10% ceramic capacitors (0402)
C11	1	2.2µF ±10% ceramic capacitor (0603)
C12	1	0.1µF ±10% ceramic capacitor (0603)
C13	1	33µF ±10% tantalum capacitor (B case) AVX TAJB336K010R
C17	1	27pF ±5% ceramic capacitor (0402)
C25	1	33pF ±5% ceramic capacitor (0402)
C26	1	10µF ±20% ceramic capacitor (0603)
J1–J9, J11, J13–J20, J22, J23, J24	21	SMA connectors, edge-mount, tab-contact Johnson 142-0701-851
J10, J12	2	Test points Keystone 5000
L1, L4, L5, L8, L9, L11, L13, L16, L17, L20, L21, L24, L25, L28, L29, L32, L35, L36	18	Ferrite beads (0402) Murata BLM15HD102SN1
L2, L3, L6, L7, L10, L12, L14, L15, L18, L19, L22, L23, L26, L27, L30, L31, L33, L34	18	4.7µH ±10% inductors (0805) Murata LQM21NN4R7K10
R1–R10, R12, R15–R18, R20, R21, R22	18	150Ω ±1% resistors (0402)
R11	1	49.9Ω ±1% resistor (0402)
R13	1	10.5Ω ±1% resistor (0402)
S1, S2, S9, S11, S13–S17	9	Switches, SP3T, slide Alps SSS211900
S3, S6, S18–S21	6	Switches, SPDT, slide E-Switch EG1218
TP1, TP2	2	Test points Keystone 5000
U1	1	Clock generator (48 TQFN-EP*) Microsemi MAX3612ETM+
U2	1	25MHz crystal NDK EXS00A-AT00429
—	1	PCB: MAX3612 EVALUATION BOARD+ REV B

**EP = Exposed pad.*

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Quick Start

1) Set the switches to the following settings to generate a 156.25MHz LVDS output from the 25MHz crystal reference:

   IN_SEL = XO

   PLL_BP = LOW

   DM = LOW

   DF = LOW

   DA = LOW

   DB = LOW

   DC = LOW

   QA_CTRL1 = LVDS

   QA_CTRL2 = DISABLED

   QB_CTRL = DISABLED

   QC_CTRL = DISABLED

   QA_TERM1 = LVDS

   QA_TERM2 = LVDS

   QB_TERM = LVDS

   QC_TERM = LVDS

2) Connect a +3.3V supply to VCC (J10) and GND (J12).

3) Set the supply current limit to 500mA. Using SMA cables, connect QA0 and $\overline{QA0}$ to a phase noise analyzer or scope. Terminate all unused enabled outputs (QA1, $\overline{QA1}$, QA2, $\overline{QA2}$).

Detailed Description

The MAX3612 evaluation kit (EV kit) simplifies evaluation by providing the hardware needed to evaluate all the MAX3612 functions. Table 1 contains functional descriptions for the switches. Table 2 provides the divider settings for various frequency configurations.

LVCMOS Clock Input

The LVCMOS clock input (CIN) is AC-coupled at the SMA connector and has an on-board 50Ω termination. For optimal performance, it is important to use a low-jitter square-wave clock source. Clock signals should be applied to CIN only when the switch IN_SEL is set to CIN.

Differential Clock Input

The differential clock input (DIN) is AC-coupled at the SMA connectors and has an internal 100Ω differential termination. For optimal performance, it is important to use a low-jitter, differential, square-wave clock source. Clock signals should be applied to DIN only when the switch IN_SEL is set to DIN.

LVDS/LVPECL Clock Outputs

The LVDS/LVPECL clock outputs (QA[4:0], QB[2:0], QC) are configured using switches S14–S21. Each output has an on-board bias-T, which provides DC-bias when configured as LVPECL and AC-coupling for direct connection to 50Ω-terminated test equipment. Unused outputs should be disabled (using switches S14–S17) or have 50Ω terminations placed on the SMA connectors. For optimal jitter measurements, a balun is recommended for differential to single-ended conversion when connected to single-ended test equipment such as a phase noise analyzer. See Figure 1 for the measurement setup.

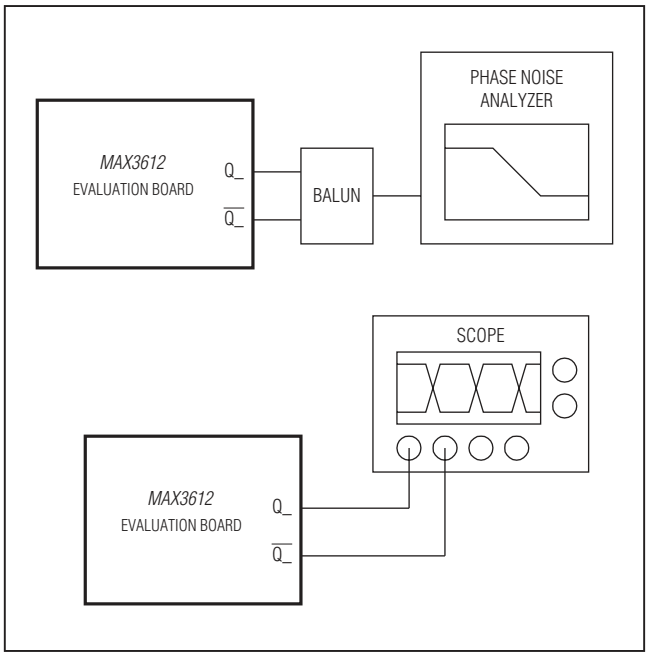

Figure 1. Measurement Setup

Table 1. Switch Descriptions

COMPONENT	NAME	FUNCTION
S1	IN_SEL	Selects input reference clock source. DIN = Differential input DIN, DIN CIN = LVCMOS input CIN XO = Crystal reference (25MHz on-board)
S2	PLL_BP	Selects PLL bypass mode. HIGH = All outputs PLL bypass OPEN = C output bank PLL bypass LOW = All outputs PLL enabled
S3	DM	Selects input divider M. See Table 2.
S6	DF	Selects feedback divider F. See Table 2.
S9	DA	Selects output divider A. See Table 2.
S11	DB	Selects output divider B. See Table 2.
S13	DC	Selects output divider C. See Table 2.
S14	QA_CTRL1	Selects QA[2:0] output interface (LVPECL, LVDS, or DISABLED).
S15	QA_CTRL2	Selects QA[4:3] output interface (LVPECL, LVDS, or DISABLED).
S16	QB_CTRL	Selects QB[2:0] output interface (LVPECL, LVDS, or DISABLED).
S17	QC_CTRL	Selects QC output interface (LVPECL, LVDS, or DISABLED).
S18	QA_TERM1	Selects QA[2:0] output termination. Provides DC path to GND for QA[2:0] bias-Ts when switched to LVPECL. DC path to GND is open when switched to LVDS.
S19	QA_TERM2	Selects QA[4:3] output termination. Provides DC path to GND for QA[4:3] bias-Ts when switched to LVPECL. DC path to GND is open when switched to LVDS.
S20	QB_TERM	Selects QB[2:0] output termination. Provides DC path to GND for QB[2:0] bias-Ts when switched to LVPECL. DC path to GND is open when switched to LVDS.
S21	QC_TERM	Selects QC output termination. Provides DC path to GND for QC bias-Ts when switched to LVPECL. DC path to GND is open when switched to LVDS.

Table 2. Divider Settings for Various Frequency Configurations

INPUT FREQUENCY (MHz)	INPUT DIVIDER	FEEDBACK DIVIDER	VCO FREQUENCY (MHz)	OUTPUT DIVIDER	OUTPUT FREQUENCY (MHz)
	DM	DF		DA, DB, DC	
25	LOW	LOW	625	OPEN	312.5
31.25	LOW	HIGH		LOW	156.25
125	HIGH	LOW		HIGH	125
156.25	HIGH	HIGH			

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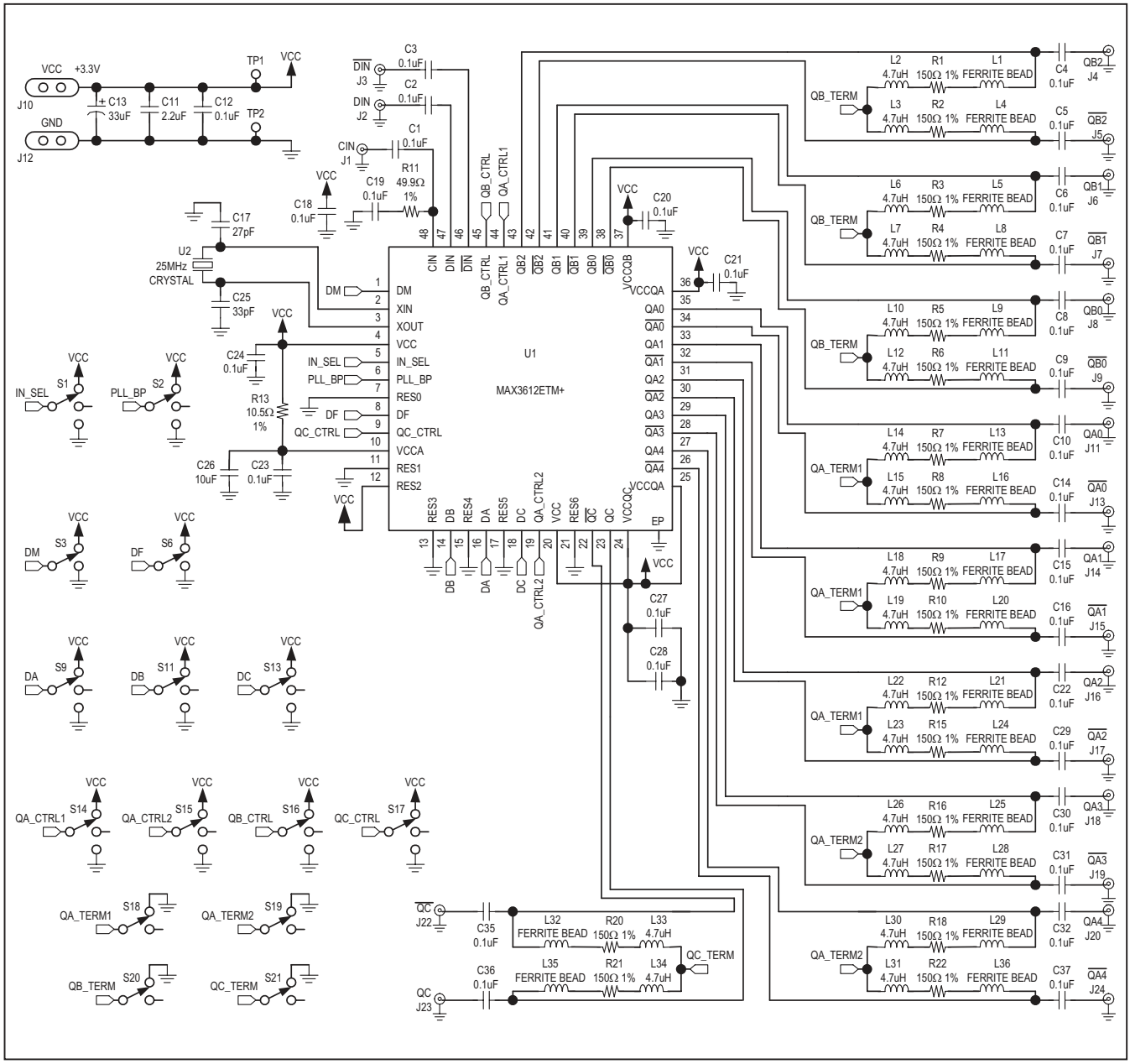


Figure 2. MAX3612 EV Kit Schematic

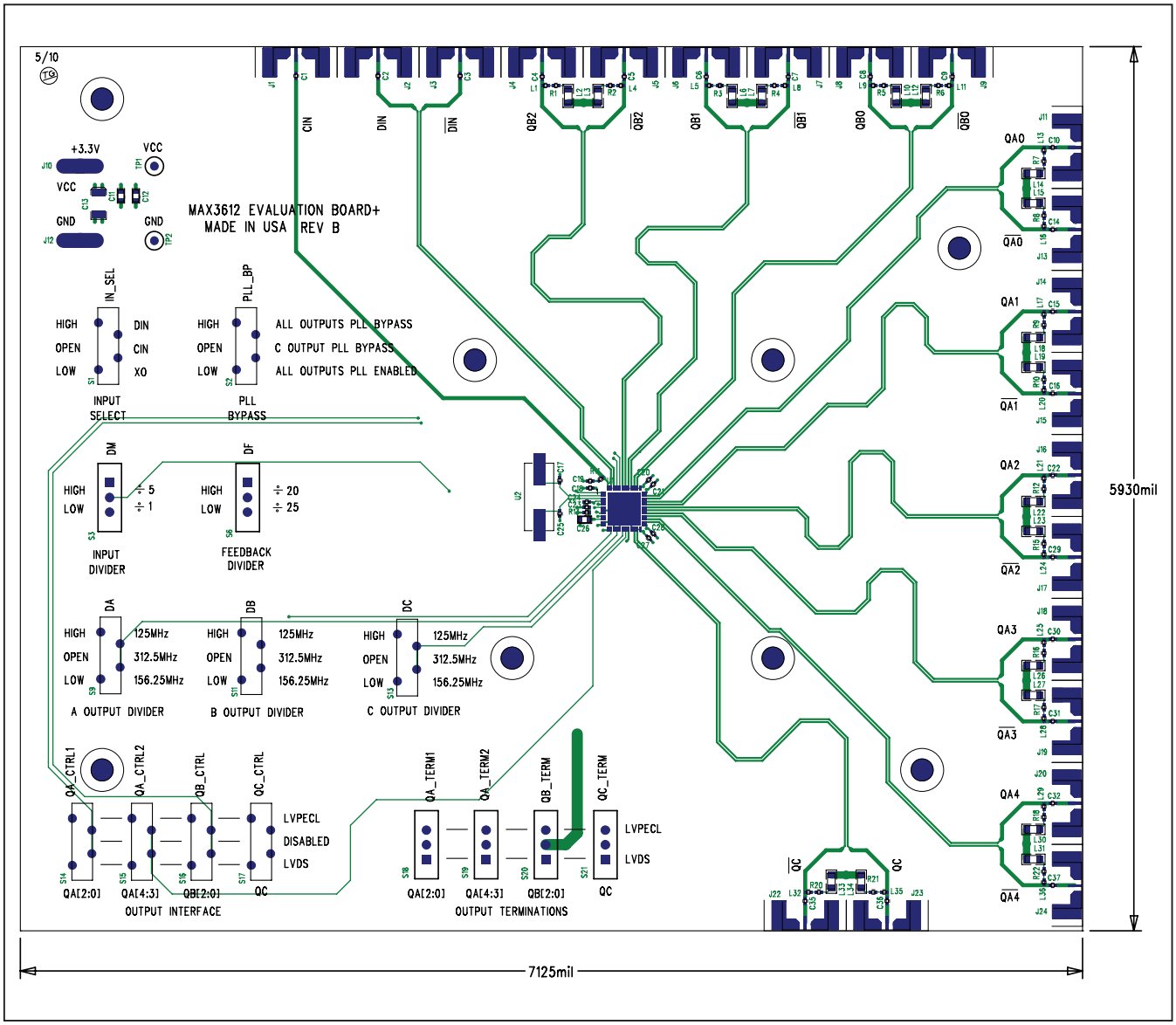


Figure 3. MAX3612 EV Kit Component Placement Guide—Component Side

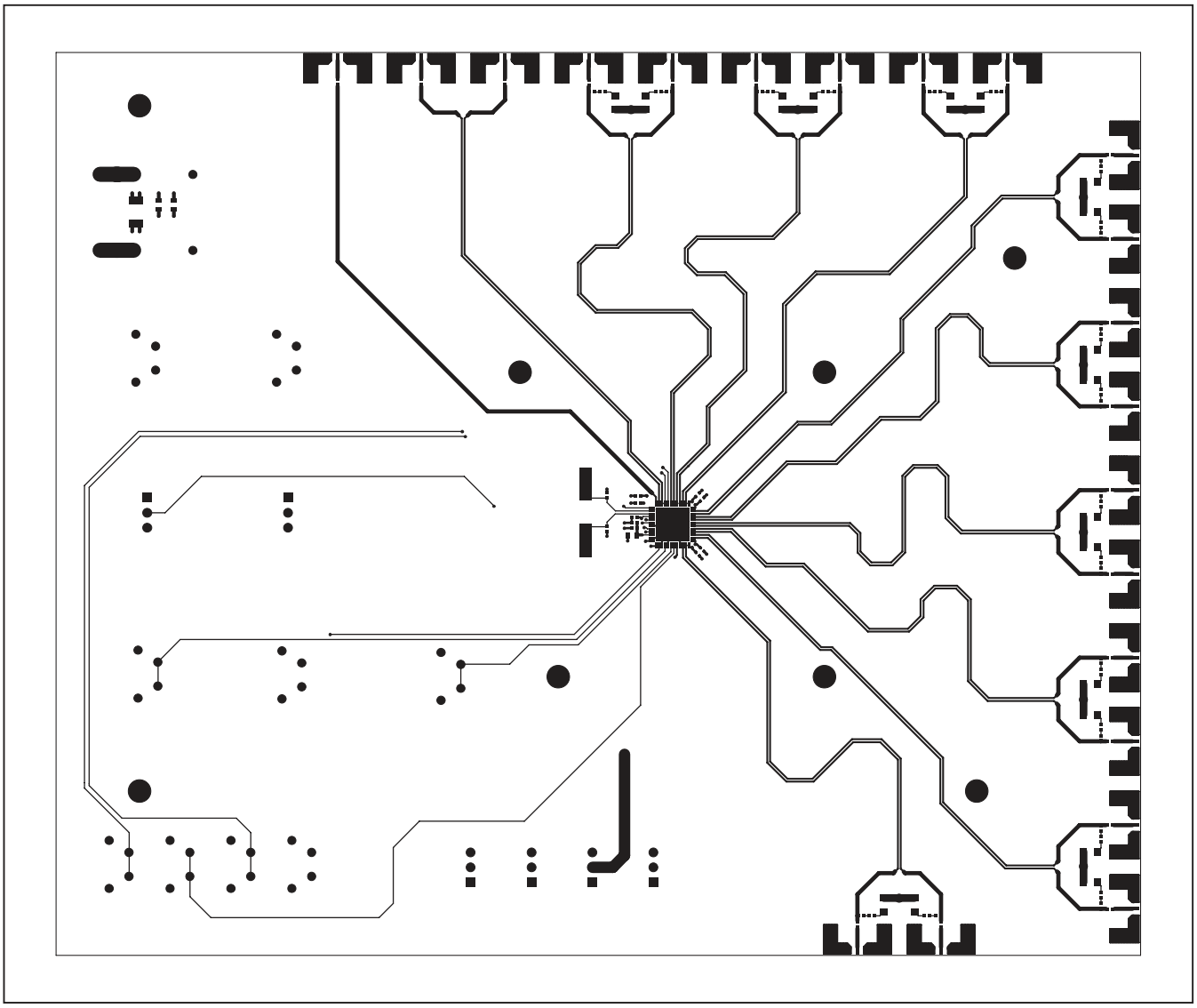


Figure 4. MAX3612 EV Kit PCB Layout—Component Side

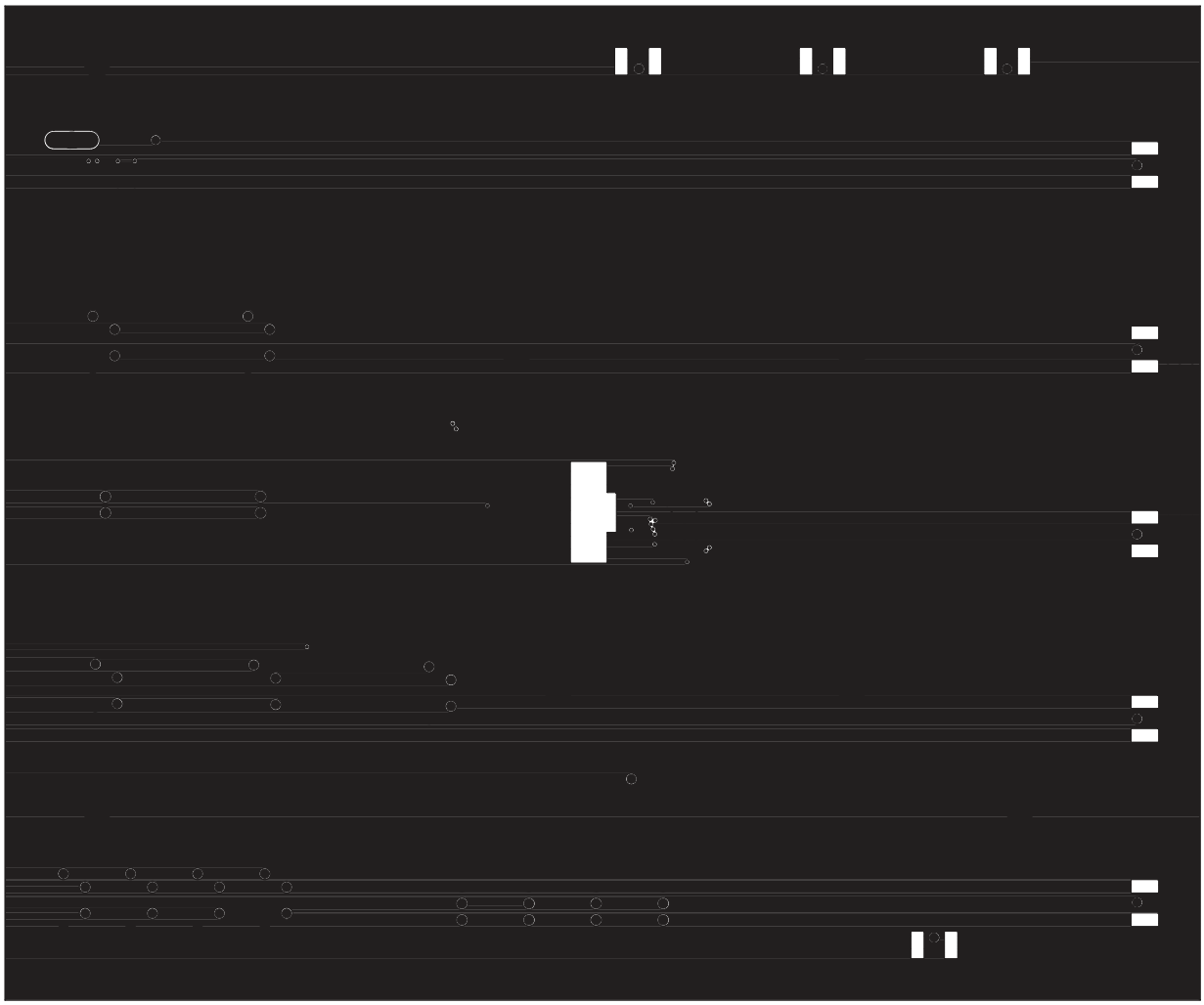


Figure 5. MAX3612 EV Kit PCB Layout—Ground Plane

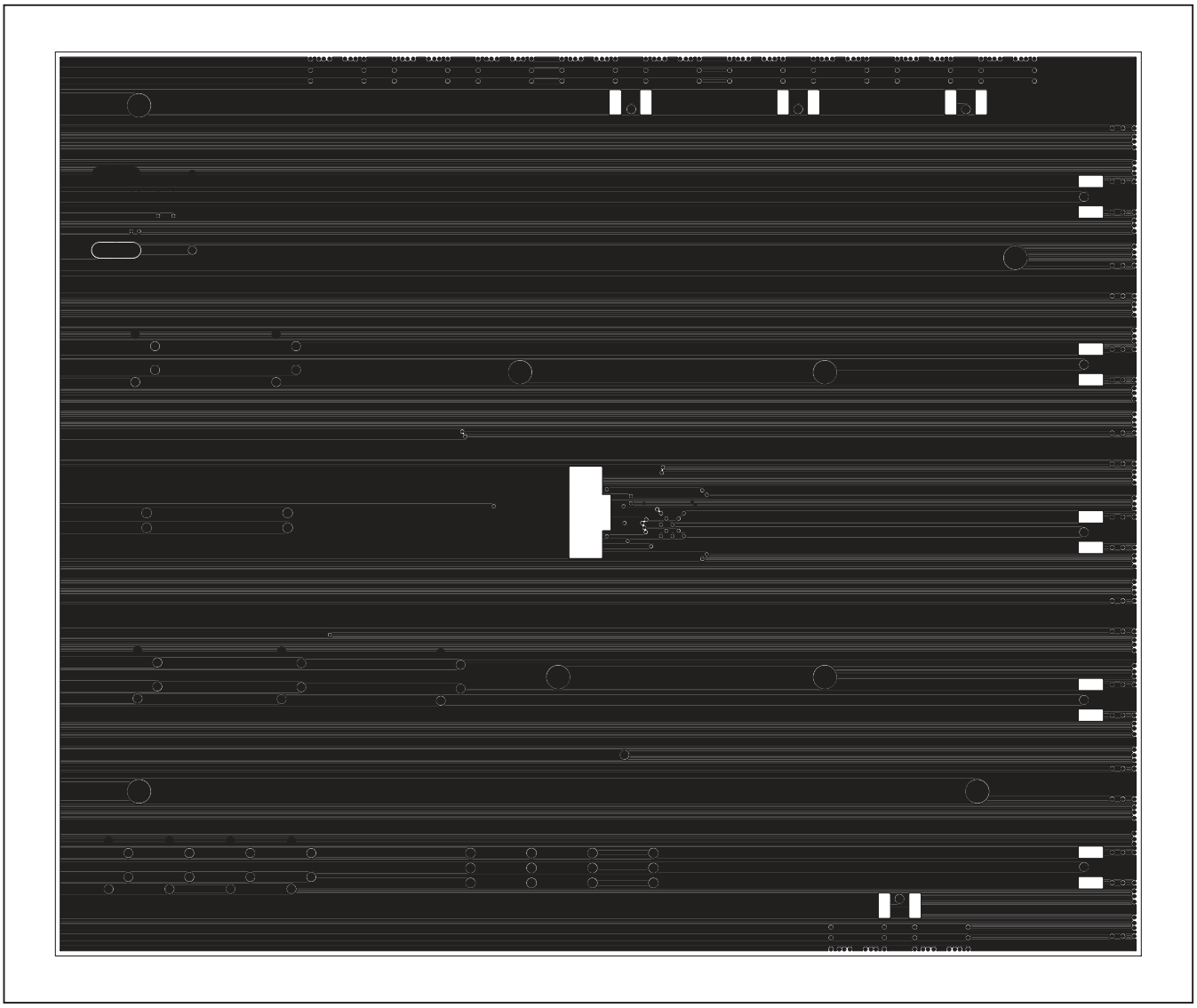


Figure 6. MAX3612 EV Kit PCB Layout—Power Plane

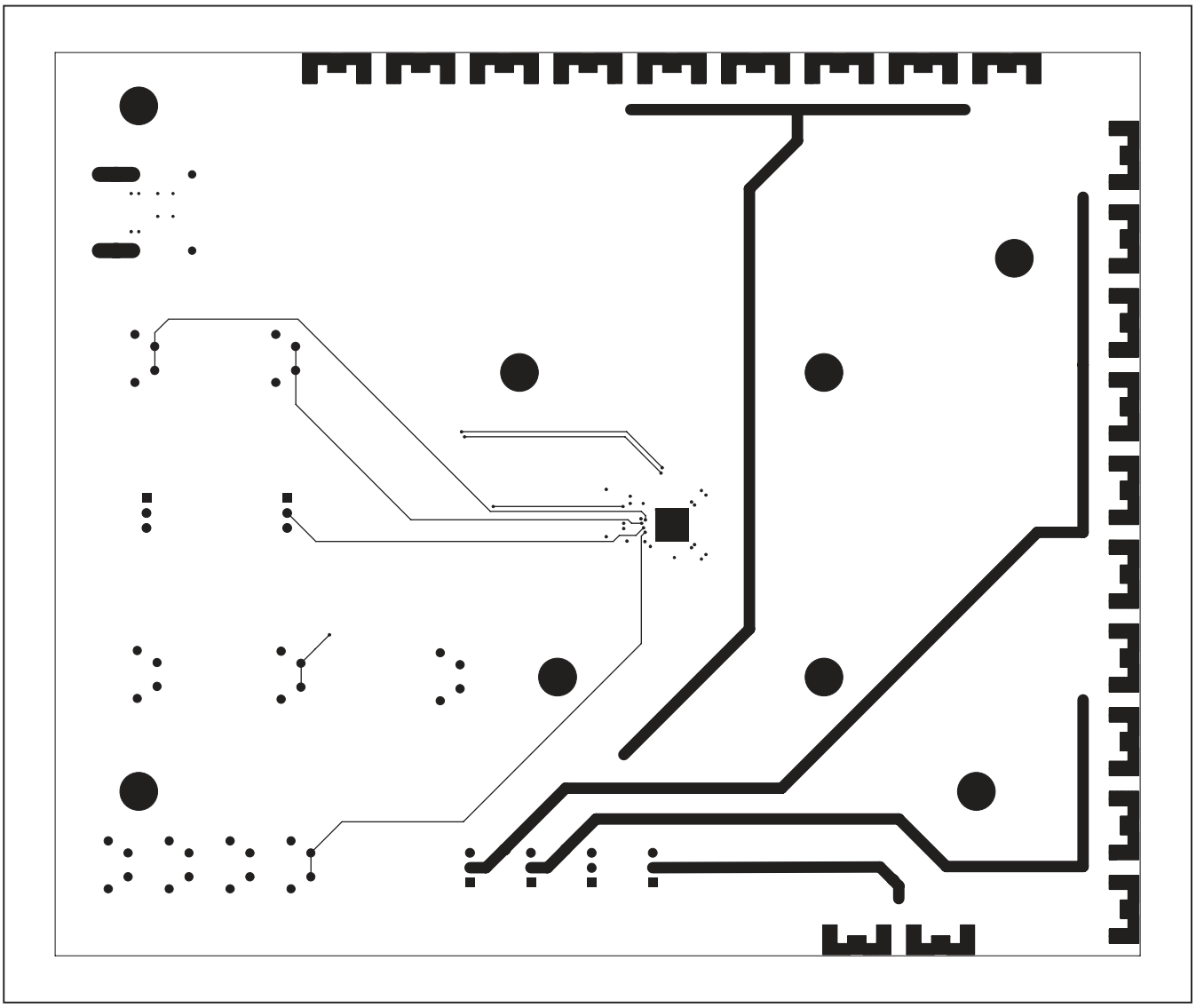
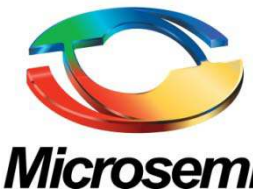


Figure 7. MAX3612 EV Kit PCB Layout—Solder Side

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/10	Initial release	—



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