Digital Phase Shifter
6-Bit, 2.4 - 5.1 GHz

MAPS-011019
Rev. V1

Features

- 6 Bit Digital Phase Shifter
- 360° Coverage with LSB = 5.625°
- Integrated Driver
- Serial or Parallel Control
- Low DC Power Consumption
- Minimal Attenuation Variation over Phase Shift Range
- 50 Ω Impedance
- EAR99
- Lead-Free 4 mm 24-Lead PQFN Package
- RoHS* Compliant

Applications

- Multi Market

Description

The MAPS-011019 is a GaAs pHEMT 6-bit digital phase shifter with an integrated driver in a lead-free 4 mm PQFN plastic surface mount package. The step size is 5.625° providing phase shift from 0° to 360° steps. This design has been optimized to minimize variation in attenuation over the phase shift range.

The MAPS-011019 is ideally suited for use where high phase accuracy with minimum loss variation over the phase shift range is required. The 4 mm PQFN package provides a smaller footprint than is typically available for a wideband digital phase shifter with an internal driver. Typical applications include 5G and test equipment.

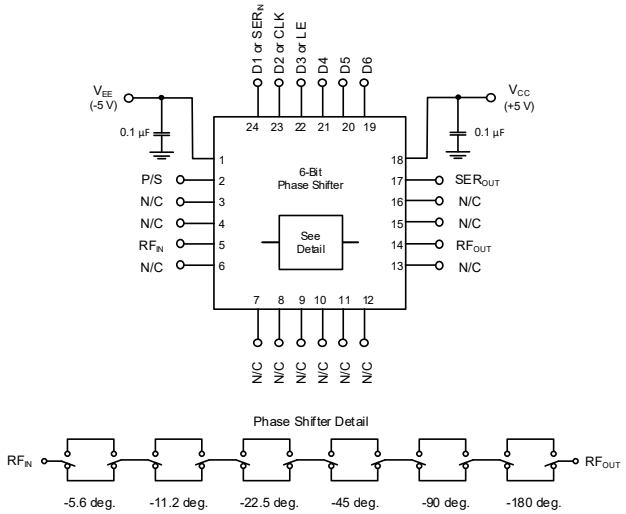
Ordering Information[1]

Part Number	Package
MAPS-011019-TR0500	500 piece reel
MAPS-011019-SMB	Sample Test Board

1. Reference Application Note M513 for reel size information.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Functional Schematic



Pin Configuration [2,3,4]

Pin #	Function
1	V_{EE}
2	P/S
3, 4, 6 - 13, 15, 16	N/C
5	RF_{IN}[5]
14	RF_{OUT}[5]
17	SER_{OUT}
18	V_{CC}
19	D6
20	D5
21	D4
22	D3 or LE
23	D2 or CLK
24	D1 or SER_{IN}

2. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.
3. Unused logic controls must be grounded.
4. MACOM recommends connecting unused package pins (N/C) to ground
5. RF_{IN} and RF_{OUT} are DC-coupled to ground and AC matched to 50 Ω. DC blocking capacitors are not necessary if the RF line DC potential is ground.

Electrical Specifications: Freq. = 2.4 - 5.1 GHz, T_A = 25°C, Z_0 = 50 Ω, V_{CC} = +5 V, V_{EE} = -5 V

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Operating Power [6]	2.4 to 5.1 GHz	dBm	—	—	27
Insertion Loss (Any Phase State)	Any Phase State	dB	—	4.5	6.0
Attenuation Variation	Peak to Peak Amplitude Change Across All Phase States	dB	—	1.5	—
RMS Attenuation Error [7]	All Values Relative to Insertion Loss at Reference Phase	dB	—	0.6	—
RMS Phase Error [7]	All Values Relative to Reference Phase	deg	—	4.0	—
Phase Accuracy Relative to Reference Loss State	5.6 Degree Bit 11.2 Degree Bit 22.5 Degree Bit 45 Degree Bit 90 Degree Bit 180 Degree Bit Sum of All Bits	deg	—	± 2 ± 2 ± 3 ± 3 ± 7 ± 10 ± 4	—
Phase Variation within Any 200 MHz Bandwidth	Peak to Peak Phase Change within Any 200 MHz Bandwidth for Any Phase State	deg	—	3	—
VSWR	RF Input RF Output	Ratio	—	1.6:1 1.6:1	—
T_{RISE}/T_{FALL}	10% to 90% RF / 90% to 10% RF	ns	—	20	—
T_{ON}/T_{OFF}	50% control to 90%/10% RF	ns	—	40	—
1 dB Compression	Reference State	dBm	—	29	—
Input IP3	Two-tone inputs up to +5 dBm	dBm	—	48	—
V_{CC} V_{EE}	—	V	3.0 -5.5	— -5.0	5.5 -3.0
V_{IL} V_{IH}	LOW-level input voltage HIGH-level input voltage	V	0.0 0.7 x V_{CC}	—	0.3 x V_{CC} V_{CC}
I_{IN} (Input Control Current)	V_{IN} = V_{CC} or GND	µA	—	1	—
V_{OH} V_{OL}	For serial out; I_{OH} = -100 µA For serial out; I_{OL} = 100 µA	V	V_{CC} - 0.2 —	—	— 0.2
I_{CC} (Quiescent Supply Current)	$V_{CONTROL}$ = V_{CC} or GND	µA	—	0.5	—
I_{EE}	V_{EE} min to max V_{IN} = V_{IL} or V_{IH}	µA	—	-5	—

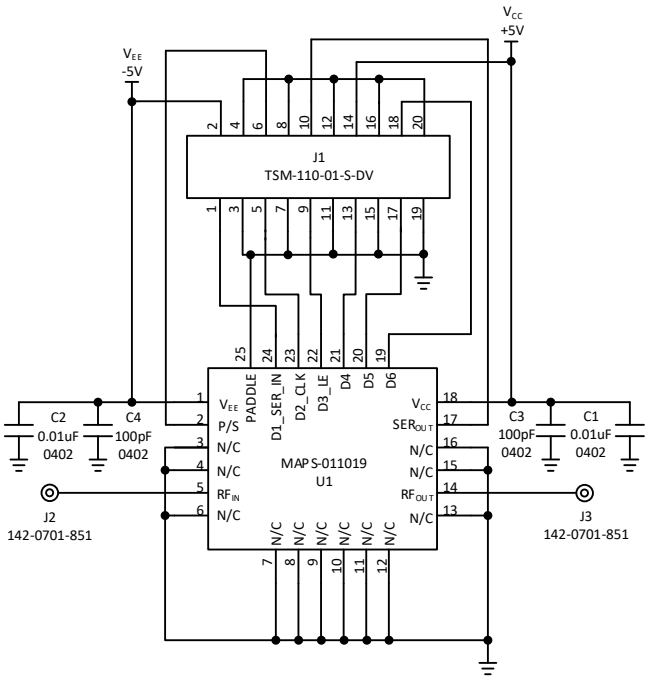
6. Maximum operating power is the maximum power where the specifications are guaranteed.
7. RMS is calculated across all 63 amplitude or phase states relative to the amplitude or phase in the 0° phase state at a given frequency.

Absolute Maximum Ratings[8,9]

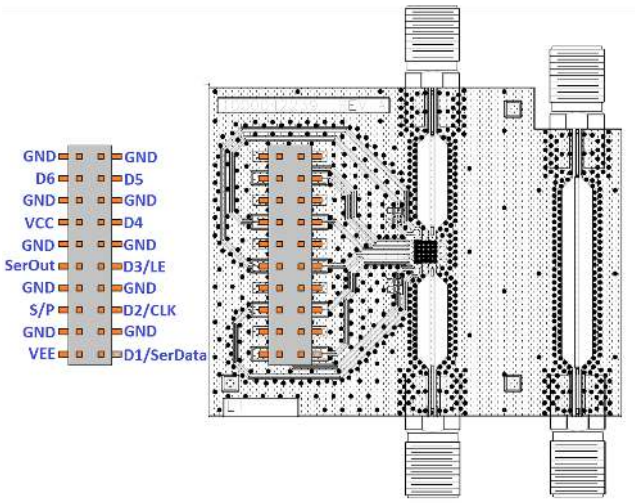
Parameter	Absolute Maximum
Input Power	+29 dBm
V_{CC}	-0.5 V ≤ V_{CC} ≤ +7.0 V
V_{EE}	-7.0 V ≤ V_{EE} ≤ +0.5 V
D1-D6, P/S, LE, CLK or SER_{IN}	-0.5 V ≤ V_{IN} ≤ V_{CC} + 0.5 V
SER_{OUT}	-0.5 V ≤ V_{OUT} ≤ V_{CC} + 0.5 V
Operating Temperature	-40ºC to +85ºC
Storage Temperature	-65ºC to +150ºC

8. Exceeding any one or combination of these limits may cause permanent damage to this device.
9. MACOM does not recommend sustained operation near these survivability limits.

Application Schematic



Sample Board Header Pin Labels



Parts List

Part	Value	Case Style
U1	MAPS-011019	4mm QFN-24LD
C1, C2	Capacitor, 0.01 µF, 50 V	0402
C3,C4	Capacitor, 100 pF, 50 V	0402
J1	Samtec TSM-110-01-S-DV	Two-row Header
J2,J3	SMA, 142-0701-851	End Launch

Handling Procedures

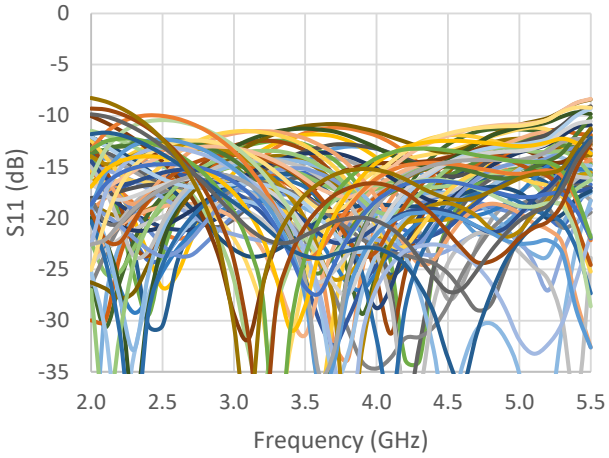
Please observe the following precautions to avoid damage:

Static Sensitivity

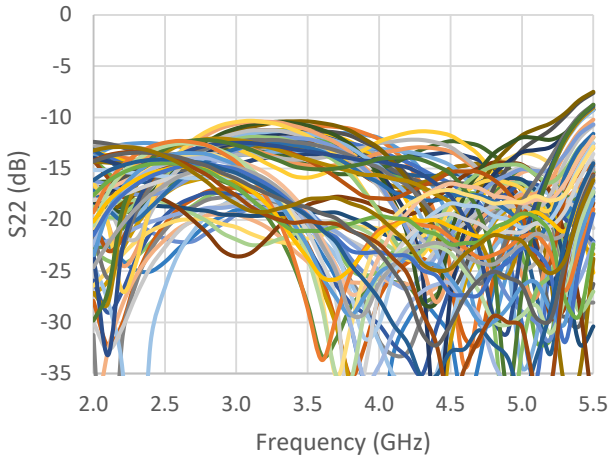
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1C devices.

Typical Performance Curves

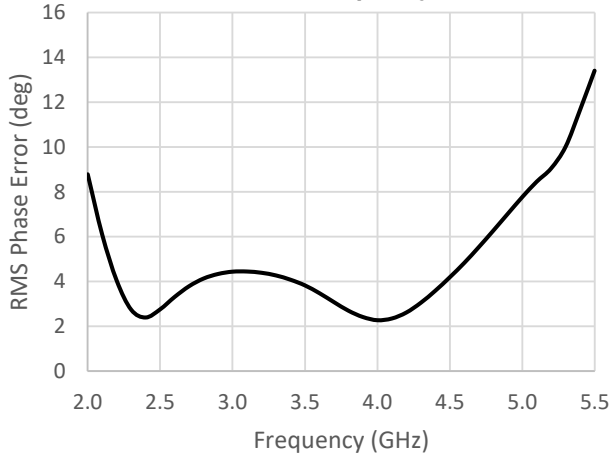
RF_{IN} Return Loss vs. Frequency (All States)



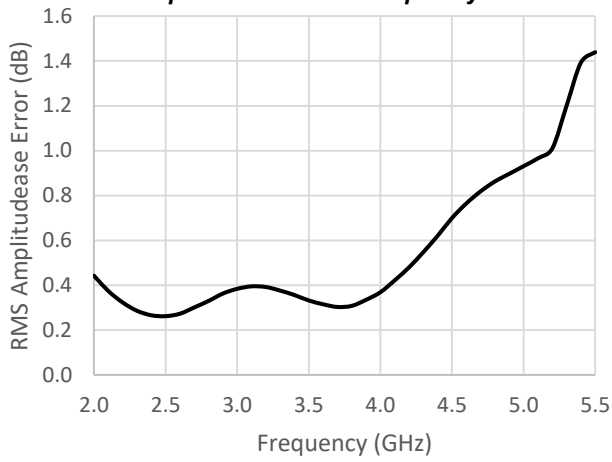
RF_{OUT} Return Loss vs. Frequency (All States)



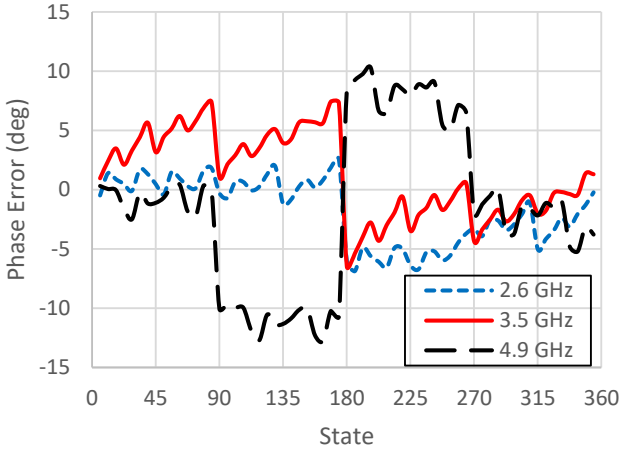
Mean RMS Phase Error vs. Frequency



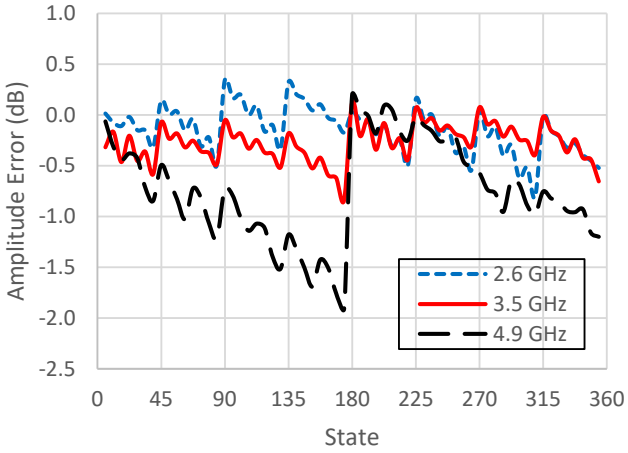
Mean RMS Amplitude Error vs. Frequency



Phase Error (degrees) vs. State

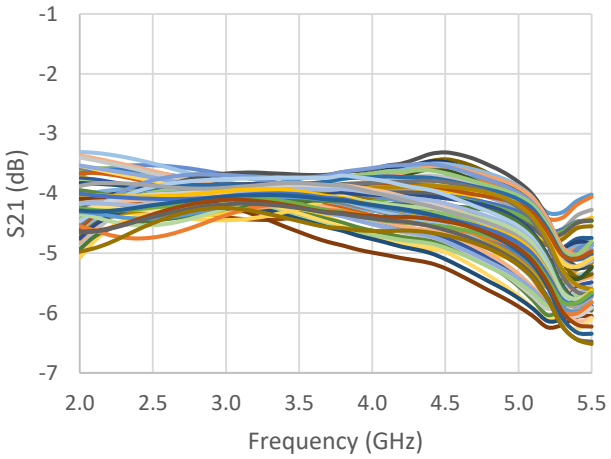


Amplitude Error (dB) vs. State

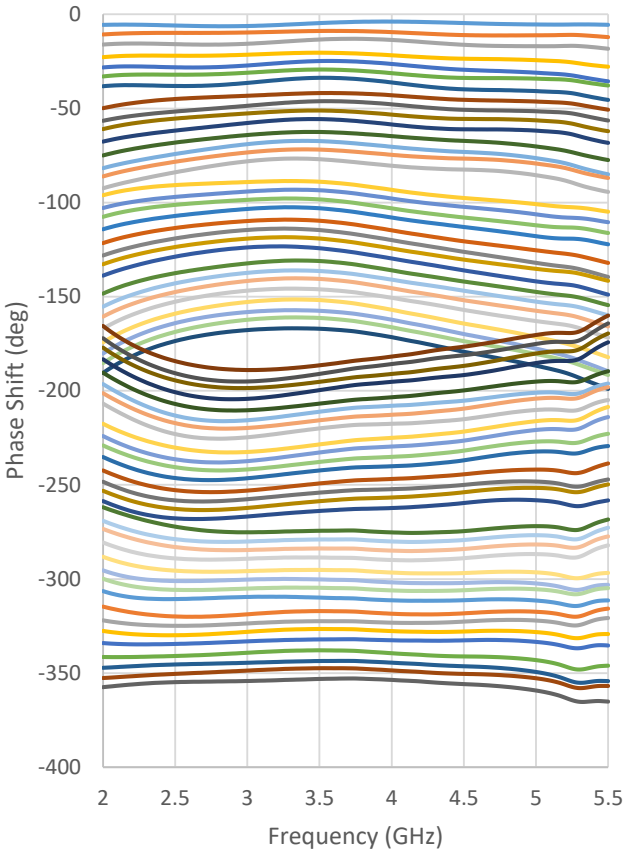


Typical Performance Curves

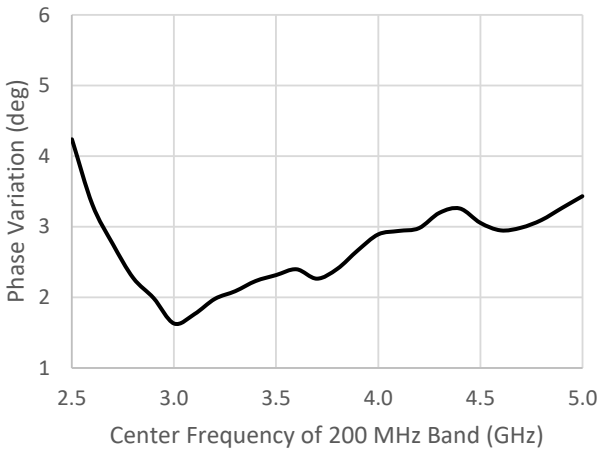
Amplitude Variation vs. Phase State



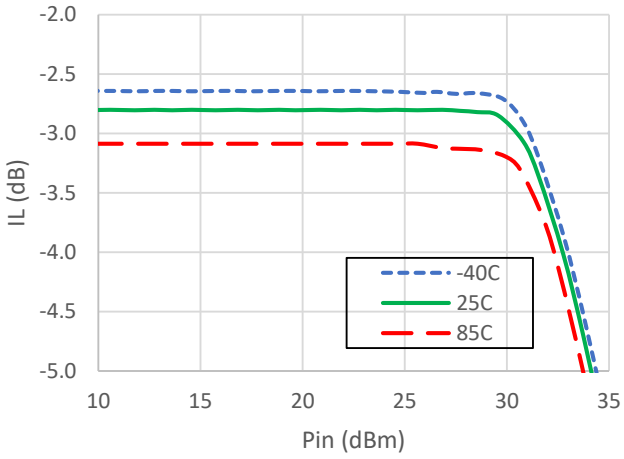
Phase Shift vs. Frequency (All States)



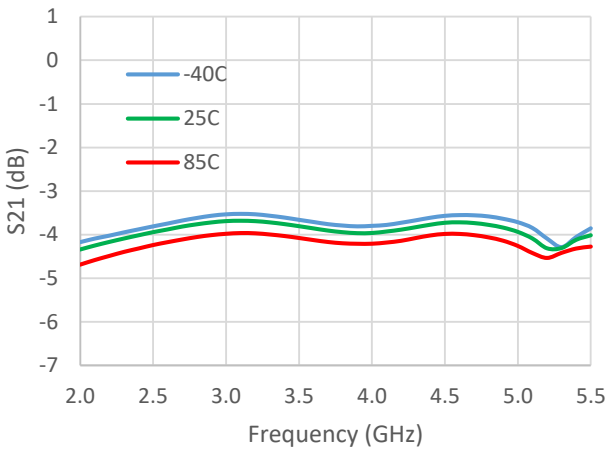
Phase Variation within any 200 MHz Band



Input P1dB at 3.5 GHz



Reference State Insertion Loss vs. Frequency



Modes of Operation: Serial and Direct Parallel

Bias Sequencing for both Modes

To avoid potential problems with application of supplies with floating controls, known logic levels (preferably 0 V) should be applied to the controls before the VDD and VEE are supplied. One easy way to do this is with pull down resistors. VDD an VEE can be applied in either order.

Serial Mode

The serial control interface (SERIN, CLK, LE, SEROUT) is compatible with the SPI protocol. SPI mode is activated when P/S is kept high. The 6-bit serial word must be loaded with the MSB first. After shifting in the 6 bit word, a rising edge on LE will set the phase shifter to the desired state. While LE is high the CLK is masked to protect the data while implementing the change. SEROUT is SERIN delayed by 6 clock cycles.

When P/S is low, the serial control interface is disabled. When P/S is set high, pins 22, 23, and 24 have the LE, CLK, and SER IN function.

In serial mode operation, the outputs will stay constant while LE is kept low.

Direct Parallel Mode

The parallel mode is enabled when P/S is set low. In the direct parallel mode, the phase shifter is controlled by the parallel control inputs directly. When P/S is set low, pins 22, 23, and 24 have the D3, D2, and D1 function.

Mode Truth Table

P/S	LE	Mode
1	X	Serial
0	N/A	Direct Parallel

Truth Table (Digital Phase Shifter) [10]

D6	D5	D4	D3	D2	D1	Phase Shift
0	0	0	0	0	0	Reference Phase
0	0	0	0	0	1	5.6°
0	0	0	0	1	0	11.2°
0	0	0	1	0	0	22.5°
0	0	1	0	0	0	45°
0	1	0	0	0	0	90°
1	0	0	0	0	0	180°
1	1	1	1	1	1	354.4°

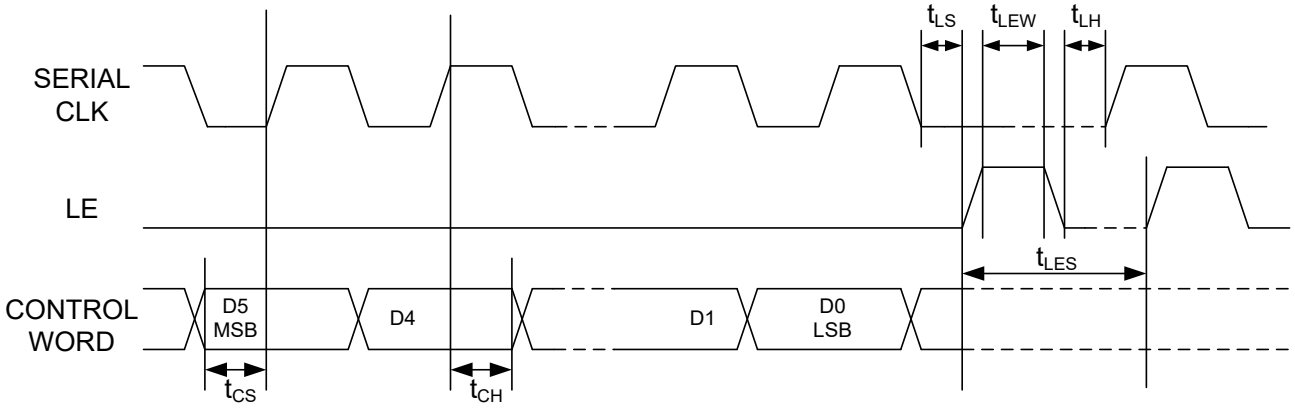
10. 0 = CMOS Low; 1 = CMOS High, X is CMOS Low or High.

Serial Interface Timing Characteristics

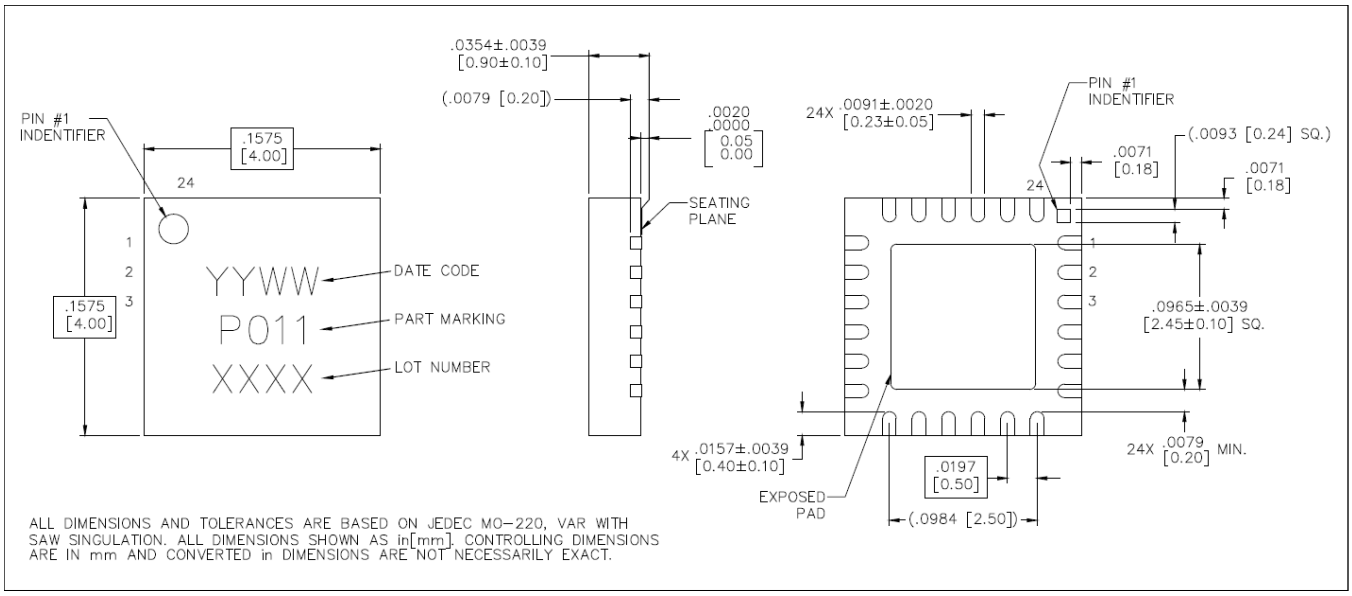
Symbol	Parameter	Typical Performance			Units
		-40°C	+25°C	+85°C	
t_{SCK}	Min. Serial Clock Period	100	100	100	ns
t_{CS}	Min. Control Set-up Time	20	20	20	ns
t_{CH}	Min. Control Hold Time	20	20	20	ns
t_{LS}	Min. LE Set-up Time	10	10	10	ns
t_{LEW}	Min. LE Pulse Width	10	10	10	ns
t_{LH}	Min. Serial Clock Hold Time from LE	10	10	10	ns
t_{LES}	Min. LE Pulse Spacing	630	630	630	ns

Functionality
Modes of Operation: Serial and Direct Parallel

Serial Input Interface Timing Diagram



Lead Free 4 mm 24-Lead PQFN †



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Plating is 100% matte tin over copper.