3- 5 cells Li-ion/polymer battery protection IC

MM3575 Series

Description

The MM3575 series are protection IC using high voltage CMOS process for overcharge,overdischarge and overcurrent protection of the rechargeable Lithium-ion or Lithium-polymer battery. The overcharge, overdischarge, discharging overcurrent, charging overcurrent, cell balance and from V5 to V3 pin disconnect of the rechargeable from 3 to 5cell Lithium-ion or Lithium-polymer battery can be detected. By using cascade connection, it is also possible to protect 6 or more cells rechargeable Lithium-ion battery. And the regulator can be constructed by using external Nch MOS FET. The internal circuit of IC is composed by the voltage detector, the reference voltage source, delay time control circuit, and the logical circuit, etc.

Features

1) Range and accuracy of detection/release voltage (Unless otherwise specified, Topr=+25°C)

Item	Range	Accuracy
・Overcharge detection voltage	3.6V to 4.5V, 5mV steps	±25mV (Topr=±0 to +50°C)
・Overcharge release voltage	3.4V to 4.5V, 50mV steps	±50mV
・Overdischarge detection voltage	2.0V to 3.0V, 50mV steps	±80mV
・Overdischarge release voltage *4	2.0V to 3.5V, 50mV steps	±100mV
・Discharging overcurrent detection voltage 1	30mV to 300mV, 5mV steps	±15mV (typ 50mV -)
・Discharging overcurrent detection voltage 2	Twice or 4 times of VDET3-1 *1	±15%
・Short detection voltage	4 or 8 times of VDET3-1 *1	±100mV
・Charging overcurrent detect voltage	-300mV to -20mV, 5mV steps	±10mV
・Cell balance detection voltage	3.6V to 4.5V, 5mV steps	±30mV (Topr=±0 to +50°C)

2) Range of detection delay time

Item	Range	Accuracy
・Overcharge detection delay time	Selection from 0.25s, 1.0s, 1.2s, 4.1s	±25%
・Overcharge release delay time	Selection from 10ms, 24ms, 48ms, 100ms	±25%
・Overdischarge detection delay time	Selection from 0.25s, 1.0s, 1.2s, 4.1s	±25%
・Overdischarge release delay time	Selection from 4ms, 8ms, 12ms, 24ms	±25%
・Discharging overcurrent detection delay time1	Setting by a capacitor of COC pin. *2	±30%
・Discharging overcurrent detection delay time2	Setting by a capacitor of COC pin. *2	±30%
・Short detection delay time	Selection from 100us, 200us, 300us	±50%
・Discharging overcurrent release delay time	Setting by a capacitor of COC pin. *2	±30%
・Charging overcurrent detection delay time	Setting by a capacitor of COC pin. *2	±30%
・Charging overcurrent release delay time	Setting by a capacitor of COC pin. *2	±30%
・Disconnect detection delay time	Selection from 25ms, 50ms, 100ms	±25%
・Disconnect release delay time	Selection from 1024ms, 2048ms, 4096ms	±25%
・Cell balance detection delay time	Selection from 0.1s, 0.25s, 0.5s *3	±25%
・Cell balance release delay time	Selection from 4ms, 8ms, 12ms	±25%

*1 Optional function

*2 Since the capacity is the same, each delay times will change when a value is changed without short detection delay time.

*3 Cannot do shorter than disconnect detection delay time.

*4 The discharge state release method can choose a voltage release and a load open.

Features

3) Protected operation can be detect of V5 to V1 pin disconnection

When any of V5～V1 pin open, it will detect disconnection and charge and discharge prohibited state.
Protection mode of disconnection can be chosen from three, prohibition of charge, prohibition of discharge and prohibition of charge and discharge (Optional)
The release from disconnection protection is done by disconnection point being connected.

4) The setting for three cell , for four cell , and for five cell protection can be set with the SEL pin.

5) The charge and discharge of the battery can be controlled with SDC pin and SOC pin.

6) 0V battery charge function Selection from "Prohibition" or "Permission"

7) Power save mode built-in

It is possible to make it shift to low consumption current mode arbitrarily. Transition of power save mode is used by SDC,SOC pins.It shifts to a power save mode by making SDC and SOC pin into a VSS level.

8) Regulator function built-in

Connecting drain of external Nch MOS FET gate to DRIVE pin and source to REG_IN pin, it can operate as a regulator.The regulator operates independently with protected operation, such as overcharge detection. Regulator voltage can be chosen at 0.1V step among 3.3V to 5.0V.

9) Low current consumption

・VDD pin current consumption(Vcell=4.3V)	Typ. 25.0uA	Max. 35.0uA
・VDD pin current consumption(Vcell=3.5V)	Typ. 20.0uA	Max. 30.0uA
・VDD pin current consumption(Vcell=2.0V)	Typ. 10.0uA	Max. 15.0uA
・VDD pin current consumption at power save1(Vcell=3.5V)	Typ. 12.0uA	Max. 16.0uA
・VDD pin current consumption at power save2(Vcell=3.5V)	Typ. 4.0uA	Max. 6.0uA
・V5 pin current consumption(Vcell=4.3V)	Typ. 4.0uA	Max. 6.0uA
・V5 pin current consumption(Vcell=3.5V)	Typ. 2.0uA	Max. 4.0uA
・V5 pin current consumption(Vcell=2.0V)	Typ. 1.0uA	Max. 1.5uA
・V5 pin current consumption at power save(Vcell=3.5V)		Max. 0.05uA

10) input current

・V1,V2,V3 and V4 pin input current(Vcell=3.5V)	Max. 1.0uA

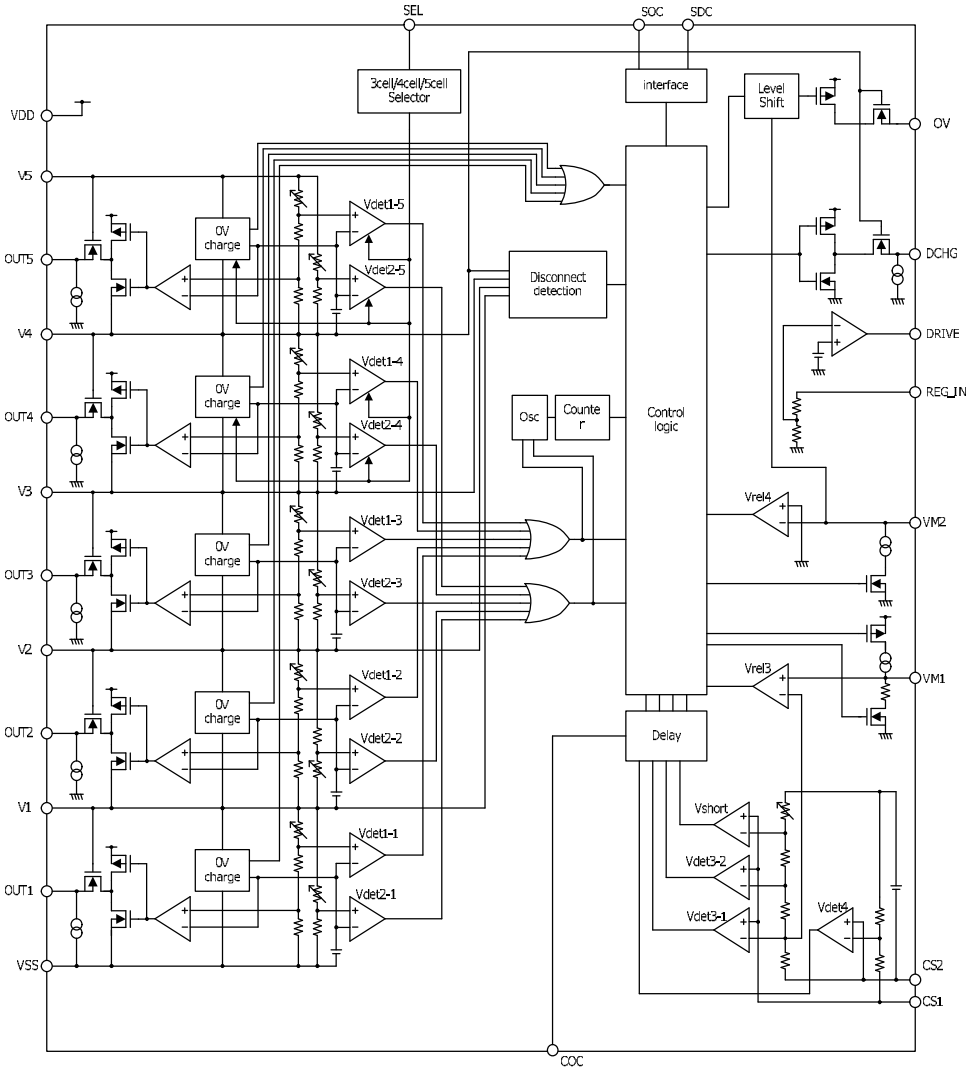
Applications

・Lithium-ion rechargeable battery pack
・Lithium polymer rechargeable battery pack

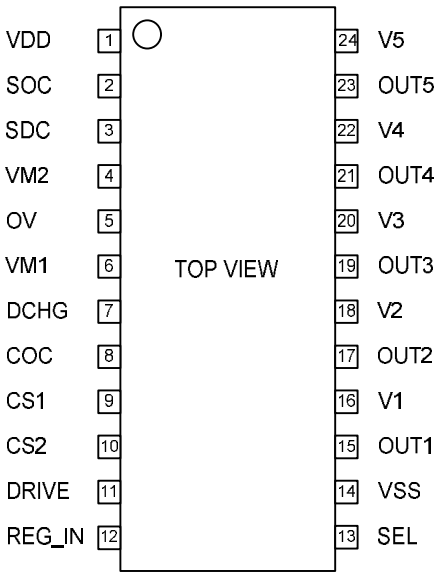
Package type

・VSOP-24A 7.90 × 7.60 × 1.25 [mm]

Block diagram



PIN CONFIGURATION



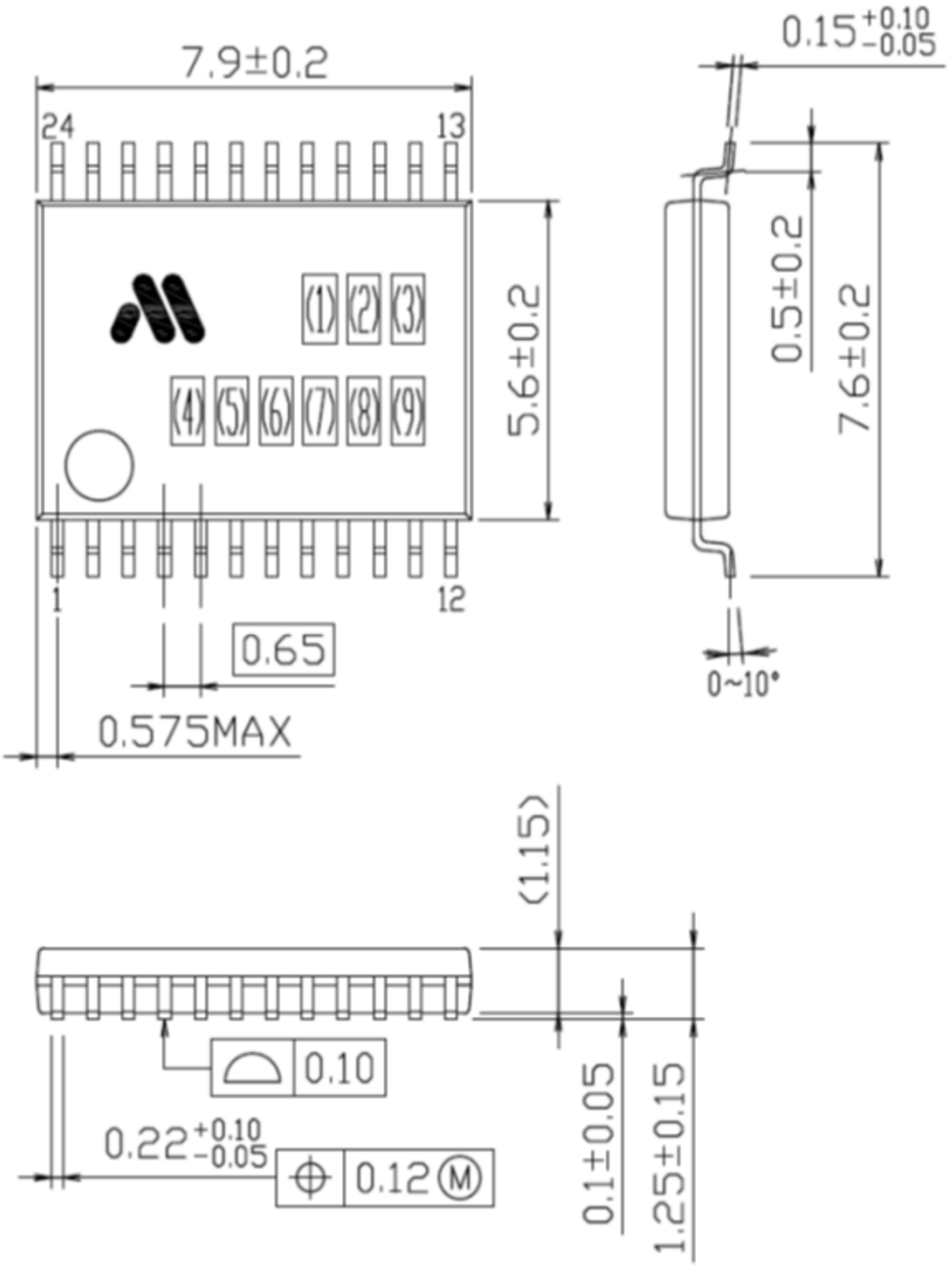
PIN EXPLANATIONS

Pin No.	Pin Name	Function
1	VDD	The input terminal of the power supply of IC.
2	SOC	The control terminal of output over charge detection. $I_{SOC} < I_{SOC}L \rightarrow$ OV=High impedance
3	SDC	The control terminal of output over discharge detection. $I_{SDC} < I_{SDC}L \rightarrow$ DCHG=Low
4	VM2	Input terminal connected to charger negative voltage. Detected charger connection.
5	OV	Charge control output terminal. Output type is Pch open drain. Normal mode→"High" Overcharge mode→"High impedance"
6	VM1	Input terminal connected to discharge voltage. Detected load connection.
7	DCHG	Discharge control output terminal. Output type is CMOS. Normal mode→"High" Overdischarge mode→"Low"
8	COC	A terminal which sets delay time of discharging overcurrent and charging overcurrent detection/release.It is able to set delay time by connecting a condenser between VDD and COC terminals.
9	CS1	Input of overcurrent detection. Detected overcurrent by sense resistor between CS1 pin and CS2 pin. And then the DCHG terminal outputs low level, and it protects from large current discharging.
10	CS2	Common terminal of overcurrent detection circuit.
11	DRIVE	The drive terminal of FET for regulator. Connect to gate of FET
12	REG_IN	The input terminal of regulator voltage. Connect to source of FET
13	SEL	This pin is for changing function for 3cell in series or 4cell in series , 5cell in series. Connect VSS→5cells in series Connect V2→4cells in series Connect VDD→3cells in series
14	VSS	The input terminal of the negative voltage of V1 cell. The input terminal of the ground of IC.
15	OUT1	V1 cell balance control output terminal. Output type is CMOS. Normal mode→"Low" Cell balance detect mode→"High"
16	V1	The input terminal of the positive voltage of V1 cell, and the negative voltage of V2 cell .
17	OUT2	V2 cell balance control output terminal. Output type is CMOS. Normal mode→"Low" Cell balance detect mode→"High"
18	V2	The input terminal of the positive voltage of V2 cell, and the negative voltage of V3 cell .
19	OUT3	V3 cell balance control output terminal. Output type is CMOS. Normal mode→"Low" Cell balance detect mode→"High"
20	V3	The input terminal of the positive voltage of V3 cell, and the negative voltage of V4 cell .
21	OUT4	V4 cell balance control output terminal. Output type is CMOS. Normal mode→"Low" Cell balance detect mode→"High"
22	V4	The input terminal of the positive voltage of V4 cell, and the negative voltage of V5 cell .
23	OUT5	V5 cell balance control output terminal. Output type is CMOS. Normal mode→"Low" Cell balance detect mode→"High"
24	V5	The input terminal of the positive voltage of V5 cell .

Package dimensions

Unit:mm

VSOP-24A



Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Supply voltage	VDD	VSS-0.3 to VSS+30	V
V5 terminal	V-	V4-0.3 to VDD+0.3	V
Voltage between the input pins of voltage of battery	Vcell	-0.3 to 10	V
OV terminal	VOV	VDD-30 to VDD+0.3	V
VM1 terminal	VVM1		
VM2 terminal	VVM2		
DCHG terminal	VDCHG	VSS-0.3 to VDD+0.3	V
CS1 terminal	VCS1		
CS2 terminal	VCS2		
OUT1 terminal	VOUT1	Vn-1 -0.3 to Vn+0.3	V
OUT2 terminal	VOUT2		
OUT3 terminal	VOUT3		
OUT4 terminal	VOUT4		
OUT5 terminal	VOUT5		
SEL terminal	VSEL	VSS-0.3 to VDD+0.3	V
SDC terminal	VSDC	VSS-0.3 to VDD+0.3	V
SOC terminal	VSOC		
DRIVE terminal	VDRIVE	VSS-0.3 to VDD+0.3	V
REG terminal	VREG		
Power dissipation	Pd	300	W

Recommend operating conditions

Parameter	Symbol	Rating	Unit
Operating ambient temperature	Topr	-40 to +85	degC
Operating voltage	Vop	VSS+3.5 to VSS+22.5	V

ELECTRICAL

Unless otherwise specified, Topr=+25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	unit
CURRENT CONSUMPTION						
Current consumption1(VDD)	I_{DD1}	V_{CELL}=4.3V	-	25.0	35.0	uA
Current consumption2(VDD)	I_{DD2}	V_{CELL}=3.5V	-	20.0	30.0	uA
Current consumption3(VDD)	I_{DD3}	V_{CELL}=2.0V	-	10.0	15.0	uA
Power save 1 Current consumption (VDD)	I_{DD_PS1}	V_{CELL}=3.5V SDC,SOC=OPEN	-	12.0	16.0	uA
Power save 2 Current consumption (VDD)	I_{DD_PS2}	V_{CELL}=3.5V SDC,SOC=VSS	-	4.0	6.0	uA
Current consumption1(V5)	I_{V5_1}	V_{CELL}=4.3V	-	4.0	6.0	uA
Current consumption2(V5)	I_{V5_2}	V_{CELL}=3.5V	-	2.0	4.0	uA
Current consumption3(V5)	I_{V5_3}	V_{CELL}=2.0V	-	1.0	1.5	uA
Power save Current consumption (V5)	I_{V5_PS}	V_{CELL}=3.5V	-	-	0.05	uA
V4・V3・V2・V1 pin input current	I_{V4}・I_{V3}・I_{V2}・I_{V1}	V_{CELL}=3.5V	-	-	1.0	uA
SEL pin input current	I_{SEL}	V_{CELL}=3.5V , SEL=VDD	-	0.150	0.225	uA
SDC pin input current	I_{SDC}	V_{CELL}=3.5V , R_{SDC}=1MΩ	-	-	1.5	uA
SOC pin input current	I_{SOC}	V_{CELL}=3.5V , R_{SOC}=1MΩ	-	-	1.5	uA
DETECTION/RELEASE VOLTAGE						
Overcharge detection voltage	V_{DET1}	Ta=±0degC to +50degC	Typ-0.025	V_{DET1}	Typ+0.025	V
Overcharge release voltage	V_{REL1}		Typ-0.050	V_{REL1}	Typ+0.050	V
Cell balance detection voltage	V_{DET_CB}		Typ-0.030	V_{DET_CB}	Typ+0.030	V
Overdischarge detection voltage	V_{DET2}		Typ-0.080	V_{DET2}	Typ+0.080	V
Overdischarge release voltage	V_{REL2}		Typ-0.100	V_{REL2}	Typ+0.100	V
Discharging overcurrent detection voltage 1	V_{DET3-1}		Typ-0.015	V_{DET3-1}	Typ+0.015	V
Discharging overcurrent detection voltage 2	V_{DET3-2}		Typ-15%	V_{DET3-2}	Typ+15%	V
Short detection voltage	V_{SHORT}		Typ-0.100	V_{SHORT}	Typ+0.100	V
VM1 pin discharging overcurrent release voltage	V_{REL3}		0.60	0.90	1.20	V
Charging overcurrent detect voltage	V_{DET4}		Typ-0.01	V_{DET4}	Typ+0.01	V
VM2 pin charging overcurrent release voltage	V_{REL4}		-0.10	0.00	0.10	V
SDC pin detection current	$I_{SDC}L$	V_{CELL}=3.5V	-	-	0.1	uA
SDC pin release current	$I_{SDC}H$	V_{CELL}=3.5V	0.75	-	-	uA
SOC pin detection current	$I_{SOC}L$	V_{CELL}=3.5V	-	-	0.1	uA
SOC pin release current	$I_{SOC}H$	V_{CELL}=3.5V	0.75	-	-	uA
DETECTION/RELEASE DELAY TIME						
Overcharge detection delay time	t_{VDET1}		Typ-25%	t_{VDET1}	Typ+25%	sec
Overcharge release delay time	t_{VREL1}		Typ-25%	t_{VREL1}	Typ+25%	msec
Cell balance detection delay time	t_{VDET_CB}		Typ-25%	t_{VDET_CB}	Typ+25%	msec
Cell balance release delay time	t_{VREL_CB}		Typ-40%	t_{VREL_CB}	Typ+40%	msec
Overdischarge detection delay time	t_{VDET2}		Typ-25%	t_{VDET2}	Typ+25%	sec
Overdischarge release delay time	t_{VREL2}		Typ-25%	t_{VREL2}	Typ+25%	msec
Discharging overcurrent detection delay time1 *5	t_{DET3-1}	C_{COC}=0.001uF	Typ-30%	t_{DET3-1}	Typ+30%	msec
Discharging overcurrent detection delay time2 *5	t_{DET3-2}	C_{COC}=0.001uF	Typ-30%	t_{DET3-2}	Typ+30%	msec

*5 Delay time can be set by external capacitor.

Electrical characteristics

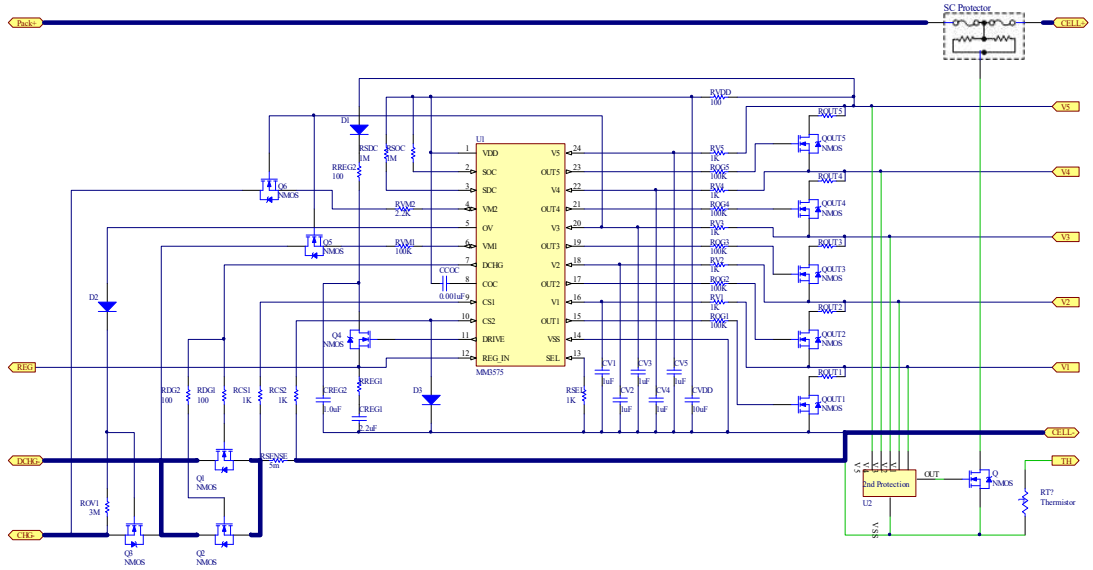
Unless otherwise specified, Topr=+25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	unit
DETECTION/RELEASE DELAY TIME						
Short detection delay time	t_{SHORT}		Typ-50%	t_{SHORT}	Typ+50%	usec
Charging overcurrent detection delay time *5	t_{VDET4}	C_{COC}=0.001uF	Typ-30%	t_{VDET4}	Typ+30%	msec
Charging overcurrent release delay time *5	t_{VREL4}	C_{COC}=0.001uF	Typ-30%	t_{VREL4}	Typ+30%	msec
Disconnect detection delay time	t_{VDET5}		Typ-25%	t_{VDET5}	Typ+25%	msec
Disconnect release delay time	t_{VREL5}		Typ-25%	t_{VREL5}	Typ+25%	msec
SDC pin detection delay time	t_{SDC_DET}		Typ-25%	t_{SDC_DET}	Typ+25%	msec
SDC pin release delay time	t_{SDC_REL}		Typ-25%	t_{SDC_REL}	Typ+25%	msec
SOC pin detection delay time	t_{SOC_DET}		Typ-25%	t_{SOC_DET}	Typ+25%	msec
SOC pin release delay time	t_{SOC_REL}		Typ-25%	t_{SDC_REL}	Typ+25%	msec
Power save mode release delay time	t_{PS_REL}		Typ-25%	t_{PS_REL}	Typ+25%	msec
Output pin・SEL pin						
DCHG pin output voltage H	V_{DCHG_H}	V_{CELL}=3.5V , I_{DCHG}=-20uA	V4-1.1	-	-	V
DCHG pin output voltage L	V_{DCHG_L}	V_{CELL}=2.0V , I_{DCHG}=20uA	-	-	0.5	V
OV pin output voltage H	V_{OV_H}	V_{CELL}=3.5V , I_{OV}=-20uA	V4-1.1	-	-	V
OV pin Leak current	I_{LEAKOV}	V_{OV}=VSS	-0.1	-	-	uA
OUT5 pin output voltage H	V_{OUT5_H}	V_{CELL}=4.25V , I_{OUT5}=-20uA	V5-1.2	-	V5	V
OUT5 pin output voltage L	V_{OUT5_L}	V_{CELL}=3.5V , I_{OUT5}=20uA	V4	-	V4+0.5	V
OUT4 pin output voltage H	V_{OUT4_H}	V_{CELL}=4.25V , I_{OUT4}=-20uA	V4-1.2	-	V4	V
OUT4 pin output voltage L	V_{OUT4_L}	V_{CELL}=3.5V , I_{OUT4}=20uA	V3	-	V3+0.5	V
OUT3 pin output voltage H	V_{OUT3_H}	V_{CELL}=4.25V , I_{OUT3}=-20uA	V3-1.2	-	V3	V
OUT3 pin output voltage L	V_{OUT3_L}	V_{CELL}=3.5V , I_{OUT3}=20uA	V2	-	V2+0.5	V
OUT2 pin output voltage H	V_{OUT2_H}	V_{CELL}=4.25V , I_{OUT2}=-20uA	V2-1.2	-	V2	V
OUT2 pin output voltage L	V_{OUT2_L}	V_{CELL}=3.5V , I_{OUT2}=20uA	V1	-	V1+0.5	V
OUT1 pin output voltage H	V_{OUT1_H}	V_{CELL}=4.25V , I_{OUT1}=-20uA	V1-1.2	-	V1	V
OUT1 pin output voltage L	V_{OUT1_L}	V_{CELL}=3.5V , I_{OUT1}=20uA	-	-	VSS+0.5	V
SEL pin input voltage L	V_{SEL}L		-	-	0.5	V
SEL pin input voltage M	V_{SEL}M		1.4	-	VDD-1.4	V
SEL pin input voltage H	V_{SEL}H		VDD-0.5	-	-	V
VM1 pin						
VM1 pin pulldown resistance	R_{VM1PD}	V_{CELL}=3.5V , VM1=1V	37.5	50.0	62.5	kΩ
Regulator						
Regulator output voltage	V_{REG}		4.75	5.00	5.25	V

*5 Delay time can be set by external capacitor.

Typical application circuit

5 cells protection circuit.



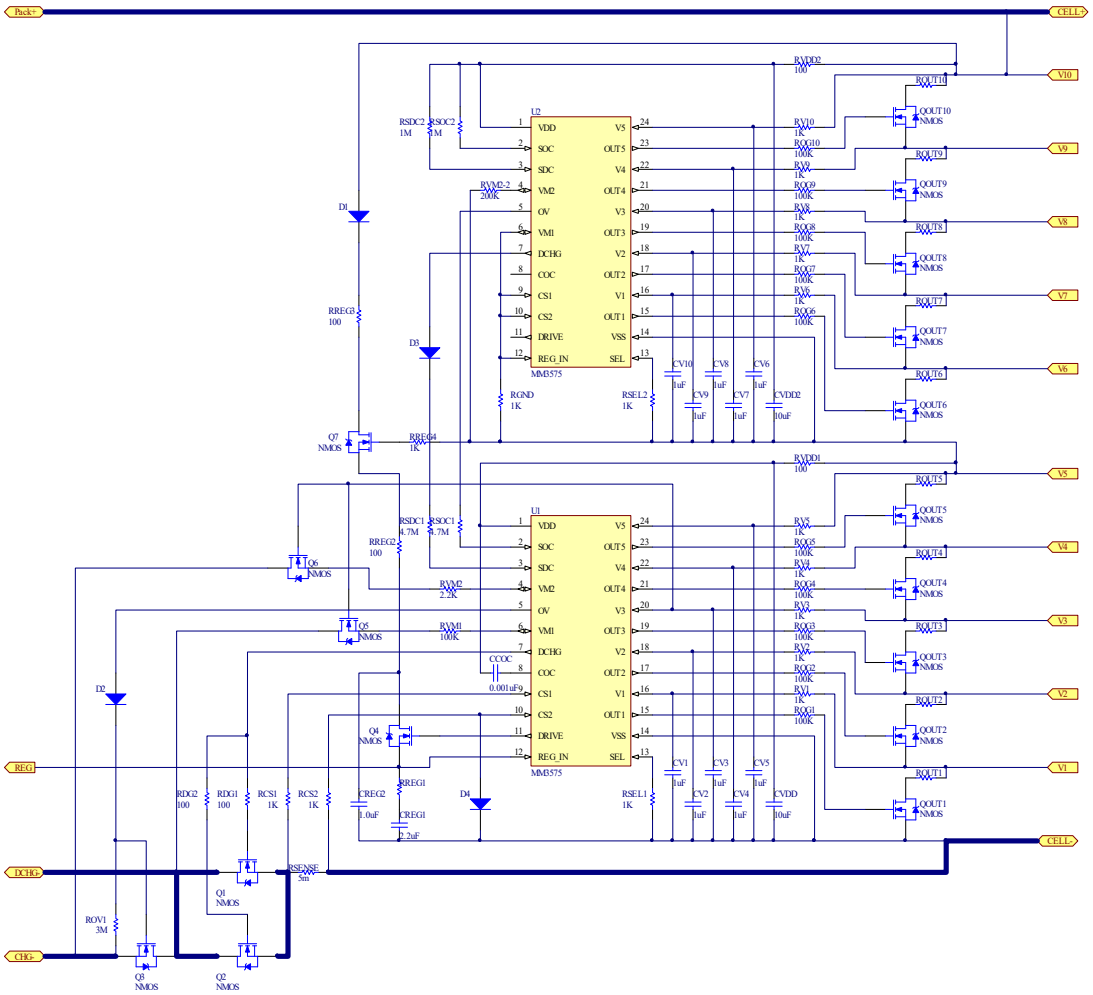
Explanation of external parts

Parts name	Roles of parts
R_{VDD}・R_{V5}・R_{V4}・R_{V3}・R_{V2}・R_{V1}	CR low-pass filter to stabilize a supply ripple of VDD pin･V5pin･V4pin･V3pin･V2pin･V1pin.
C_{VDD}・C_{V5}・C_{V4}・C_{V3}・C_{V2}・C_{V1}	
R_{OUT1}・R_{OUT2}・R_{OUT3}・R_{OUT4}・R_{OUT5}	Resistance of discharging during cell balance control.
R_{OG1}・R_{OG2}・R_{OG3}・R_{OG4}・R_{OG5}	Resistor to protect $Q_{OUT1\text{-}OUT5}$ Gate.
R_{SEL}・R_{CS1}・R_{CS2}・R_{VM1}・R_{VM2}	Resistor to protect terminal.
R_{SDC}・R_{SOC}	Current limitation resistor. (The voltage signal is converted into the current signal by this resistor at the cascading connection.)
C_{COC}	Capacitor to sets discharging overcurrent , charging overcurrent detection/release dead time.
R_{SENSE}	Sense resistance to observe charging/discharging current.
R_{DG1}・R_{DG2}	Resistor for preventing the gate destruction due to parasitic oscillation.
R_{OV1}	Pulldown resistance of OV pin
R_{REG1}	Resistance of regulator for phase compensation.
R_{REG2}	Resistance of current control when Q4 shorted out.
C_{REG1}	Capacity of regulator for phase compensation.
C_{REG2}	Capacitor to stabilize drain electric potential of Q4.
D1	Diode for preventing backflow from regulator.
D2	Diode for preventing voltage more than VDD pin voltage from applying to OV pin
Q_1・Q_2	Nch MOS FET to control discharging current.
Q_3	Nch MOS FET to control charging current.
Q_4	Power transistor of regulator
Q_5	FET for preventing voltage more than VDD pin voltage from applying to VM1 pin
Q_6	FET for preventing voltage more than VDD pin voltage from applying to VM2 pin
Q_{OUT1}・Q_{OUT2}・Q_{OUT3}・Q_{OUT4}・Q_{OUT5}	FET for controling discharging switch during cell balance control.

These circuits are typical examples provided for reference purposes, so in actual applications, the circuit constants, conditions and operations should be thoroughly studied. Mitsumi Electric Co., Ltd. Assumes no responsibility for any trouble or damage as a result of the use of these circuits.

Typical application circuit

10 cells protection circuit.



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Lineup

Product name (MM3575***WBH)	detection voltage/release voltage									Overdischarge release *6	0V battery charge function *7	Protection mode of disconnection *8
	Overcharge detection voltage	Overcharge release voltage	Overdischarge detection voltage	Overdischarge release voltage	Discharging overcurrent detection voltage1	Discharging overcurrent detection voltage2	Short detection voltage	Charging overcurrent detection voltage	Cell balance detection voltage			
	V_{DET1}	V_{REL1}	V_{DET2}	V_{REL2}	V_{DET3-1}	V_{DET3-2}	V_{SHORT}	V_{DET4}	V_{DET_CB}			
	V	V	V	V	V	V	V	V	V			
A02	4.250	4.175	2.800	2.900	0.100	0.200	0.400	-0.02	4.180	Non Latch	N	3
A08	4.250	4.100	2.600	3.200	0.090	0.180	0.360	-0.03	4.180	Non Latch	N	3
A13	4.270	4.170	2.800	3.200	0.050	0.100	0.300	-0.030	4.180	Non Latch	N	NA
A14	4.270	4.170	2.400	2.900	0.050	0.100	0.300	-0.030	4.180	Non Latch	N	NA
D01	4.230	4.180	2.800	3.000	0.100	0.400	0.800	-0.10	4.180	Non Latch	Y	NA

Product name (MM3575***WBH)	detection/release delay time													
	Overcharge detection delay time	Overcharge release delay time	Overdischarge detection delay time	Overdischarge release delay time	*9 Discharging overcurrent detection delay time1	*9 Discharging overcurrent detection delay time2	*9 Discharging overcurrent release delay time coefficient	Short detection delay time	*9 Charging overcurrent detection delay time coefficient	*9 Charging overcurrent release delay time coefficient	Disconnect detection delay time	Disconnect release delay time	Cell balance detection delay time	Cell balance release delay time
	t_{VDET1}	t_{VREL1}	t_{VDET2}	t_{VREL2}	$k_{VDET3-1}$	$k_{VDET3-2}$	k_{VREL3}	t_{SHORT}	k_{VDET4}	k_{VREL4}	t_{VDET5}	t_{VREL5}	t_{VDET_CB}	t_{VREL_CB}
	sec	msec	sec	msec	-	-	-	usec	-	-	msec	msec	msec	msec
A02	1.0	100	1.0	4.0	10.0	2.0	4.0	200	1024	128	200	4096	256	8.0
A08	1.0	100	2.0	4.0	1536	60.0	4.0	200	100	128	200	4096	256	8.0
A13	0.2	5	0.2	2.0	5.0	1.0	4.0	200	1024	50	NA	NA	200	8.0
A14	0.2	5	0.2	2.0	5.0	1.0	4.0	200	1024	50	NA	NA	200	8.0
D01	1.0	100	0.1	4.0	2048	20.0	8.0	200	512	128	NA	NA	256	4096

*6 Non Latch :voltage release
Latch :voltage release + Load release

*7 Y : Permission
N : Prohibition

*8 1 : Prohibition of charge
2 : Prohibition of discharge
3 : Prohibition of charge and discharge

*9 Discharging overcurrent, charging overcurrent detect and release delay time are calculated from the following equation by capacitor(CCOC) of connectting to VDD-COC pins and each delay time coefficient. Since the capacitor is the same, all delay times below will change when a value is changed.

$t_{VDET3-1}[ms]=k_{VDET3-1}\times C_{COC}[uF]\times 1000$ Discharging overcurrent detection delay time1
$t_{VDET3-2}[ms]=k_{VDET3-2}\times C_{COC}[uF]\times 1000$ Discharging overcurrent detection delay time2
$t_{VREL3}[ms]=k_{VREL3}\times C_{COC}[uF]\times 1000$ Discharging overcurrent release delay time2
$t_{VDET4}[ms]=k_{VDET4}\times C_{COC}[uF]\times 1000$ Charging overcurrent detection delay time
$t_{VREL4}[ms]=k_{VDET4}\times C_{COC}[uF]\times 1000$ Charging overcurrent release delay time

NOTES

【Safety Precautions】

- Though Mitsumi Electric Co., Ltd. (hereinafter referred to as "Mitsumi") works continually to improve our product's quality and reliability, semiconductor products may generally malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of this product could cause loss of human life, bodily injury, or damage to property, including data loss or corruption. Before customers use this product, create designs including this product, or incorporate this product into their own applications, customers must also refer to and comply with (a) the latest versions or all of our relevant information, including without limitation, product specifications, data sheets and application notes for this product and (b) the user's manual, handling instructions or all relevant information for any products which is to be used, or combined with this products. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. Mitsumi assumes no liability for customers' product design or applications.

- This product is intended for applying to computers, OA units, communication units, instrumentation units, machine tools, industrial robots, AV units, household electrical appliances, and other general electronic units.

【Precautions for Product Liability Act】

- No responsibility is assumed by us for any consequence resulting from any wrong or improper use or operation, etc. of this product.

【ATTENTION】

- This product is designed and manufactured with the intention of normal use in general electronics. No special circumstance as described below is considered for the use of it when it is designed. With this reason, any use and storage under the circumstances below may affect the performance of this product. Prior confirmation of performance and reliability is requested to customers.
  Environment with strong static electricity or electromagnetic wave
  Environment with high temperature or high humidity where dew condensation may occur

- This product is not designed to withstand radioactivity, and must avoid using in a radioactive environment.

- This specification is written in Japanese and English. The English text is faithfully translated into the Japanese. However, if any question arises, Japanese text shall prevail.