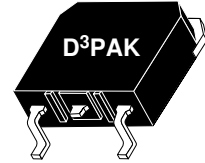
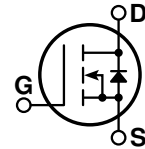




Power MOS V[®] is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V[®] also achieves faster switching speeds through optimized gate layout.



- **Faster Switching**
- **100% Avalanche Tested**
- **Lower Leakage**
- **Surface Mount D³PAK Package**



MAXIMUM RATINGS

All Ratings: T_C = 25°C unless otherwise specified.

Symbol	Parameter	APT6025SVR	UNIT
V _{DSS}	Drain-Source Voltage	600	Volts
I _D	Continuous Drain Current @ T _C = 25°C	25	Amps
I _{DM}	Pulsed Drain Current ^①	100	
V _{GS}	Gate-Source Voltage Continuous	±30	Volts
V _{GSM}	Gate-Source Voltage Transient	±40	
P _D	Total Power Dissipation @ T _C = 25°C	370	Watts
	Linear Derating Factor	2.96	W/°C
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C
T _L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I _{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	25	Amps
E _{AR}	Repetitive Avalanche Energy ^①	30	mJ
E _{AS}	Single Pulse Avalanche Energy ^④	1300	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV _{DSS}	Drain-Source Breakdown Voltage (V _{GS} = 0V, I _D = 250μA)	600			Volts
I _{D(on)}	On State Drain Current ^② (V _{DS} > I _{D(on)} × R _{DS(on)} Max, V _{GS} = 10V)	25			Amps
R _{DS(on)}	Drain-Source On-State Resistance ^② (V _{GS} = 10V, 0.5 I _{D[Cont.]})			0.250	Ohms
I _{DSS}	Zero Gate Voltage Drain Current (V _{DS} = V _{DSS} , V _{GS} = 0V)			25	μA
	Zero Gate Voltage Drain Current (V _{DS} = 0.8 V _{DSS} , V _{GS} = 0V, T _C = 125°C)			250	
I _{GSS}	Gate-Source Leakage Current (V _{GS} = ±30V, V _{DS} = 0V)			±100	nA
V _{GS(th)}	Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1.0mA)	2		4	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

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DYNAMIC CHARACTERISTICS

APT6025SVR

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1\text{ MHz}$		4300	5160	pF
C_{oss}	Output Capacitance			525	735	
C_{rss}	Reverse Transfer Capacitance			220	330	
Q_g	Total Gate Charge ③	$V_{GS} = 10V$ $V_{DD} = 0.5 V_{DSS}$ $I_D = I_{D[Cont.]} @ 25^\circ C$		185	275	nC
Q_{gs}	Gate-Source Charge			23	35	
Q_{gd}	Gate-Drain ("Miller") Charge			85	125	
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 15V$ $V_{DD} = 0.5 V_{DSS}$ $I_D = I_{D[Cont.]} @ 25^\circ C$ $R_G = 1.6\Omega$		14	28	ns
t_r	Rise Time			12	28	
$t_{d(off)}$	Turn-off Delay Time			55	80	
t_f	Fall Time			10	20	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

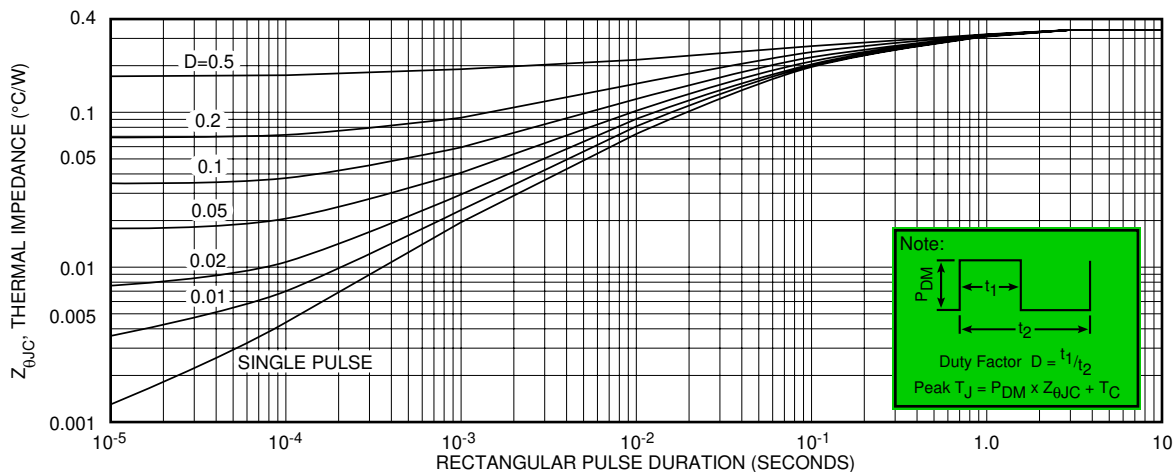
Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			25	Amps
I_{SM}	Pulsed Source Current ① (Body Diode)			100	
V_{SD}	Diode Forward Voltage ② ($V_{GS} = 0V, I_S = -I_{D[Cont.]}$)			1.3	Volts
t_{rr}	Reverse Recovery Time ($I_S = -I_{D[Cont.]}, di_S/dt = 100A/\mu s$)		580		ns
Q_{rr}	Reverse Recovery Charge ($I_S = -I_{D[Cont.]}, di_S/dt = 100A/\mu s$)		12		μC

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.34	$^\circ C/W$
$R_{\theta JA}$	Junction to Ambient			40	

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%
- ③ See MIL-STD-750 Method 3471
- ④ Starting $T_j = +25^\circ C$, $L = 4.16mH$, $R_G = 25\Omega$, Peak $I_L = 25A$

APT Reserves the right to change, without notice, the specifications and information contained herein.



APT6025SVR

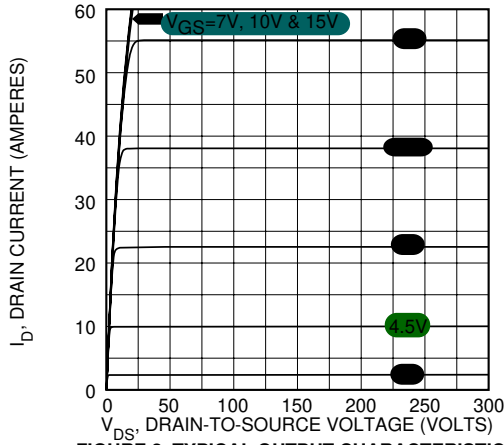


FIGURE 2, TYPICAL OUTPUT CHARACTERISTICS

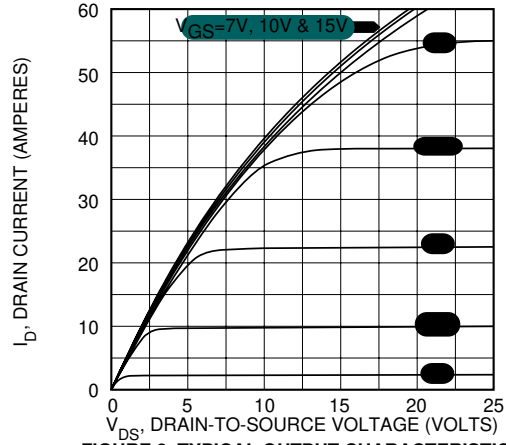


FIGURE 3, TYPICAL OUTPUT CHARACTERISTICS

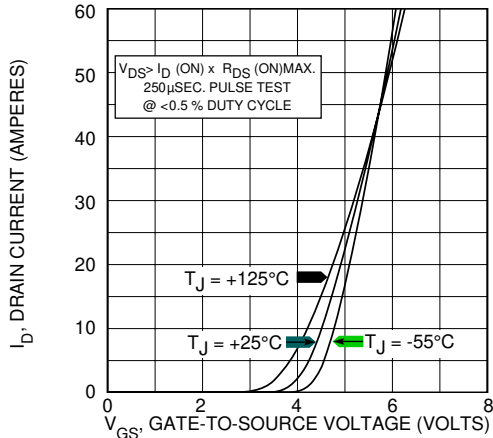


FIGURE 4, TYPICAL TRANSFER CHARACTERISTICS

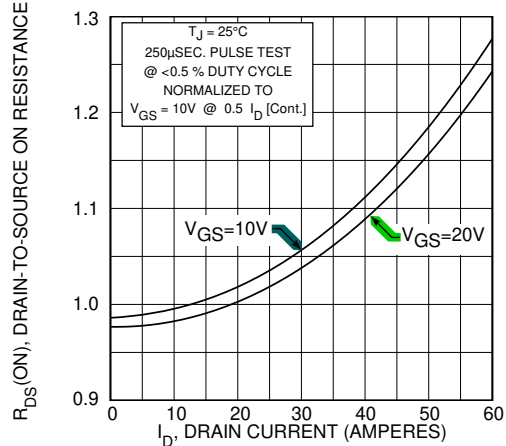


FIGURE 5, $R_{DS(ON)}$ vs DRAIN CURRENT

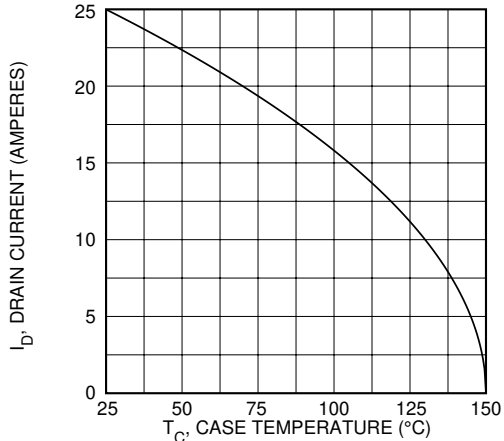


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

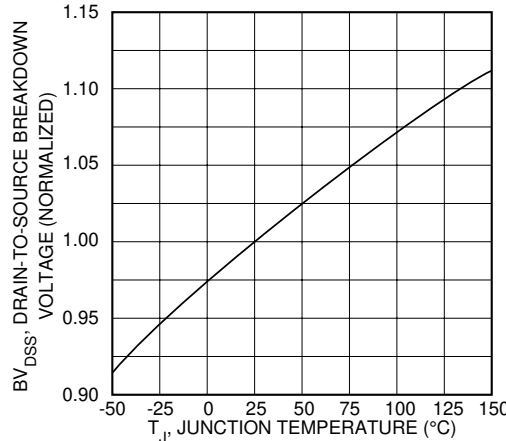


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

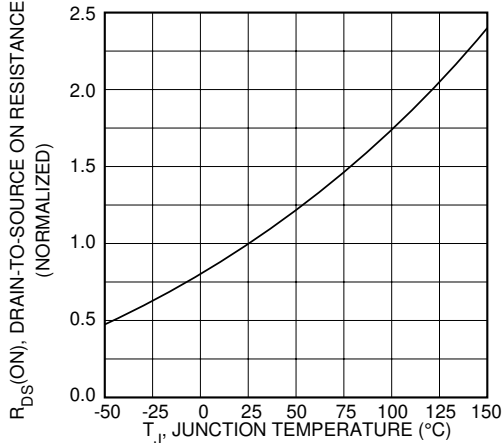


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

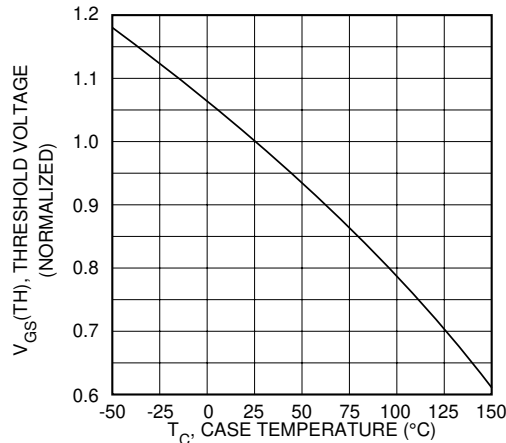


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

APT6025SVR

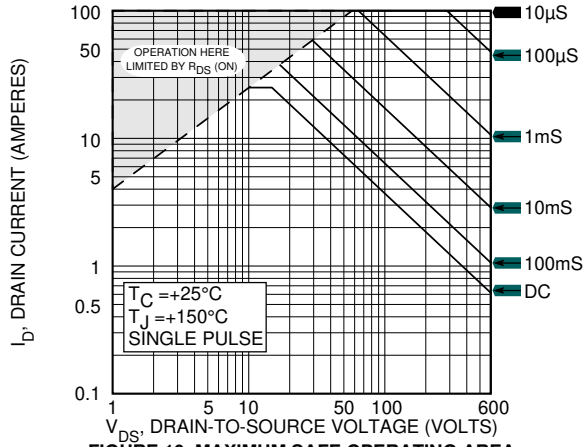


FIGURE 10, MAXIMUM SAFE OPERATING AREA

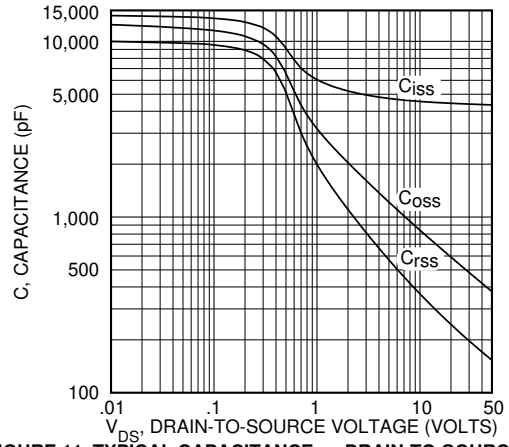


FIGURE 11, TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

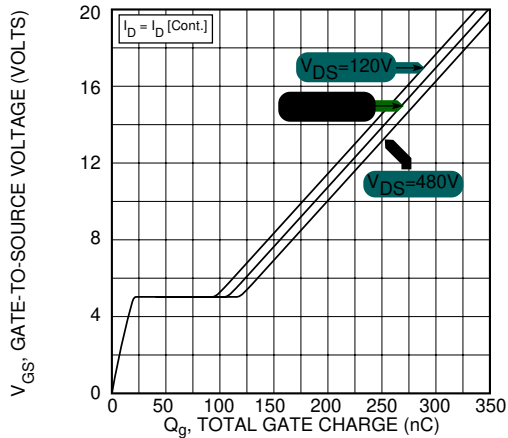


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

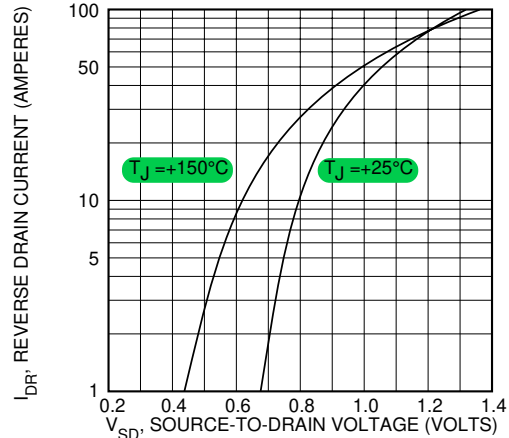


FIGURE 13, TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

D³PAK Package Outline

