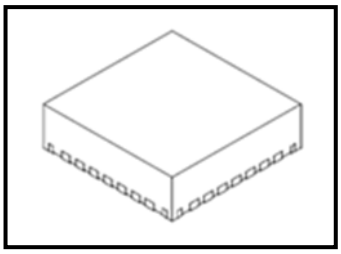
Toshiba Bi-CMOS Linear Integrated Circuit Silicon Monolithic

TB9051FTG

PWM type single channel H-Bridge DC brushed motor driver for automotive use



P-QFN28-0606-0.65-001

1. Outline

This product is a motor driver IC which incorporates the output driver for the direct drive of a DC brushed motor intended for the automotive use.

The motor drive output can be highly efficient operation by the PWM control which realizes low-on resistance.

Forward / Reverse / brake mode can be selected according to PWM1 signal and PWM2 signal, and the motor operation mode and stop mode can be selected by ENABLE pin.

Moreover, the output current capacity is 5A (max), it is suitable for various automotive applications such as a throttle and valve control, various engine bulbs, storing of door mirrors, and a seat positioning.

2. Application

Automotive applications such as a throttle and valve control, various engine bulbs, and storing of door mirrors

3. Feature

- Motor driver block: Single channel H-Bridge driver (Ron(Pch+Nch))<0.45 Ω (Max @Tj = 150°C, VBAT = 8 V)
- Abnormality detection function: Over-current detection, over-temperature detection, VBAT undervoltage detection, VCC undervoltage detection, and VCC high voltage detection
- Built-in initial diagnosis function: Power supply abnormality detection circuit (VBAT undervoltage, VCC undervoltage and VCC high voltage.)
- Output type: PWM control output
- Motor operation: Forward /Reverse/ Brake
- Current limitation control: Current limiter with chopper type
- Output high-side current monitoring function (OCM pin)
- DIAG output
- Built-in the through current prevention circuit
- Operating voltage range: VBAT = 4.5 to 28 V (Maximum ratings of power supply voltage 40V (max): 0.5 sec.)
- Operating temperature range: Ta = -40°C to 125°C
- Compact type flat package: P-QFN28-0606-0.65-001
- AEC-Q100 Qualified

・If the label of shipping box is indicated to be “[[G]]/RoHS COMPATIBLE2”, “[[G]]/RoHS [[Chemical symbol(s) of controlled substance(s)”, and “RoHS COMPATIBLE” or “RoHS COMPATIBLE, [[Chemical symbol(s) of controlled substance(s)]]>MCV”, this product is compliant with the EU RoHS Directive (2011 / 65 / EU) in the meaning of the statement.

4. Block Diagram

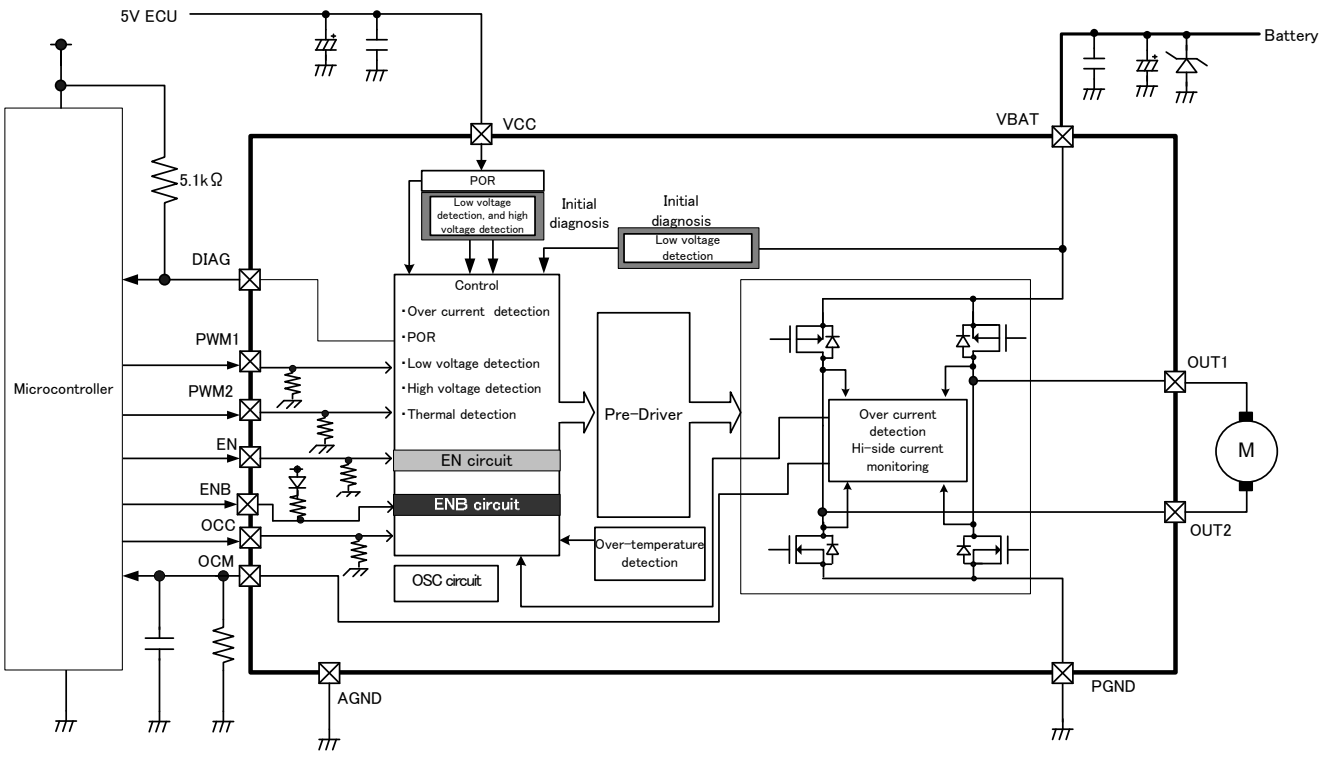


Figure 4.1 Block diagram

Note: Some of the functional blocks, circuits in the block diagram may be omitted or simplified for explanatory purposes.
The signal which is performed the logical operation of the EN and ENB pin input, is not connected to each driver output circuit. However, each EN and ENB signal is connected independently to the output circuit of each driver.

5. Pin Assignment

Pin assignment (Top View)

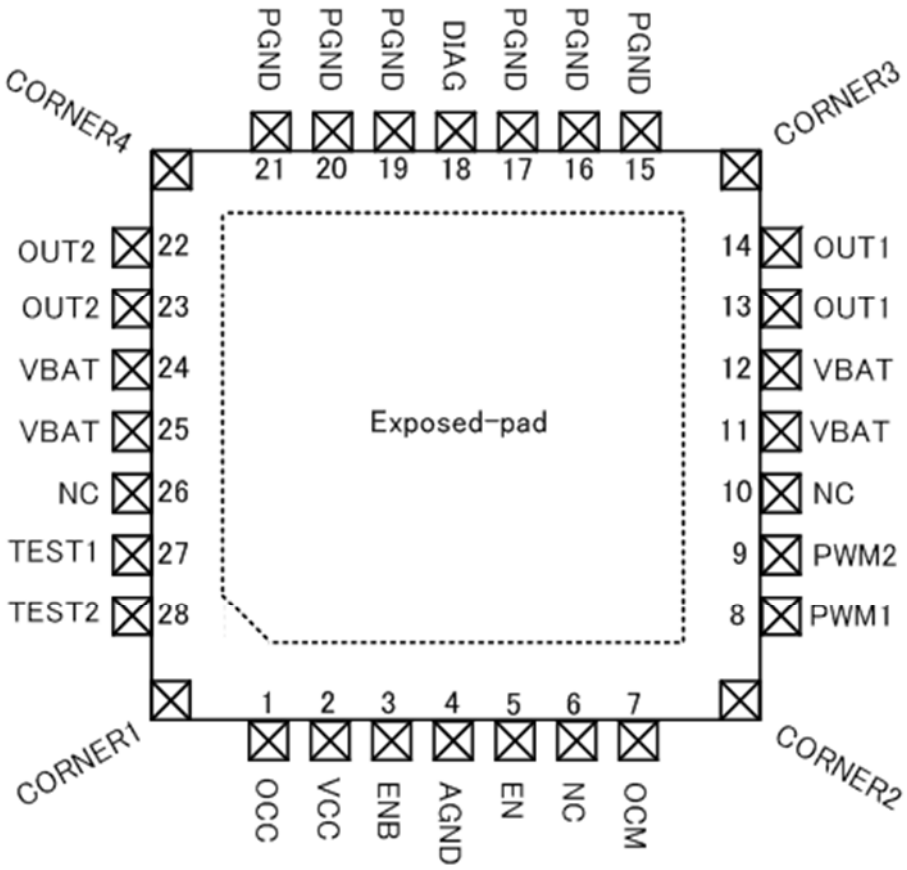


Figure 5.1 Pin assignment

6. Pin Description

Pin description

Table 6 Pin description

Pin No.	Pin name	Pin description
1	OCC	Motor drive output control pin at the time of the over-current detection (This pin is used for the judgement of whether the motor control output is ON or OFF by this IC or by the MCU.)
2	VCC	5V power supply pin. This pin is used for internal logic and analog circuit.
3	ENB	Inverted input pin of driver operation permission
4	AGND	Ground pin for analog and digital circuit
5	EN	Input pin of driver operation permission
7	OCM	Current monitoring pin at High-side. This pin can monitor the current which flows from the voltage generated to an external resistor into the H-side.
8	PWM1	Driver control signal input pin 1
9	PWM2	Driver control signal input pin 2
11, 12, 24, 25	VBAT	Battery power supply
13, 14	OUT1	H-bridge driver output pin 1
15, 16, 17, 19, 20, 21	PGND	Power ground pin (used as the ground of H-bridge)
18	DIAG	Diagnostic signal output pin Open drain type of output pin
22, 23	OUT2	H-bridge driver output pin 2
27	TEST1	Test pin This pin should be used connecting to GND.
28	TEST2	Test pin This pin should be used connecting to GND.
6, 10, 26	NC	This pin should be used open.
C1	CORNER1	These pins are connected to E-Pad.
C2	CORNER2	
C3	CORNER3	
C4	CORNER4	
-	E-Pad	This pin is used for a heat dissipation.

* The CORNER1 to 4, and E-Pad pins should be used connecting to GND. In addition, these pins are not tested for a shipment.

6.1. Protection Element Arrangement

Table 6.1 Protection element arrangement

Pin Name	Pull down /Pull up	I/O	Max rating [V]	Protection element		Protection element connection destination	
				Power supply side	GND side	Power supply side	GND side
OCC	Pull down	I	6	-	B	-	AGND
ENB	Pull up	I	6	-	B	-	AGND
EN	Pull down	I	6	-	B	-	AGND
PWM1	Pull down	I	6	-	B	-	AGND
PWM2	Pull down	I	6	-	B	-	AGND
OUT1	-	O	40	-	-	-	-
OUT2	-	O	40	-	-	-	-
DIAG	-	O	6	-	-	-	-
OCM	-	O	6	C	B	VCC	AGND
TEST1	Pull down	I	6	-	B	-	AGND
TEST2	Pull down	I	6	-	B	-	AGND
VBAT	-	Power supply	40	-	A	-	AGND/PGND
VCC	-	Power supply	6	-	B	-	AGND/PGND
NC	-	-	-	-	-	-	-
PGND	-	GND	-	-	D	-	AGND
AGND	-	GND	-	-	D	-	PGND

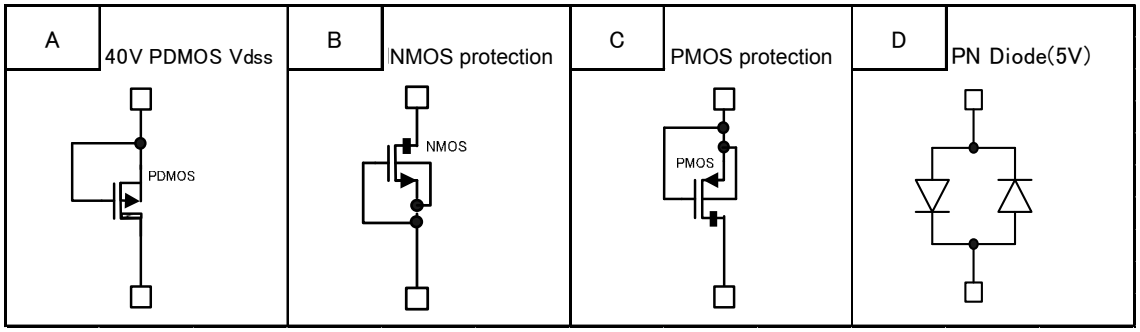


Figure 6.1 Protection element type

7. Functional Description

7.1. Motor Driver Output Circuit

The output circuit operates according to the following function (Table 7.1-1). In the Table 7.1-1 to 7.1-3, each letter means; X: Don't care, H: High, L: Low, and Z: High impedance.

Table 7.1-1 Motor function

	PWM1	PWM2	EN	ENB	DIAG pin	OUT1	OUT2
Forward	H	L	H	L	**H**	**H**	**L**
Short brake	L	L	H	L	**H**	**L**	**L**
Reverse	L	H	H	L	**H**	**L**	**H**
Short brake	H	H	H	L	**H**	**L**	**L**
EN Disable	X	X	L	X	**L**	**Z**	**Z**
ENB Disable	X	X	X	H	**L**	**Z**	**Z**
EN Disconnected	X	X	Z	X	**L**	**Z**	**Z**
ENB Disconnected	X	X	X	Z	**L**	**Z**	**Z**
PWM1 Disconnected	Z	L/H	H	L	**H**	**L**	**L/H**
PWM2 Disconnected	L/H	Z	H	L	**H**	**L/H**	**L**

Note 1: When the motor is set to the reverse from the forward, or to the forward from the reverse, be sure to perform after setting the brake between them. Otherwise the IC may be broken.

Note 2: In the current limitation control, the operation is different from the above table of the motor function. For details, refer to current limitation control (Section 7.3).

Table 7.1-2 Function operation at abnormality detection

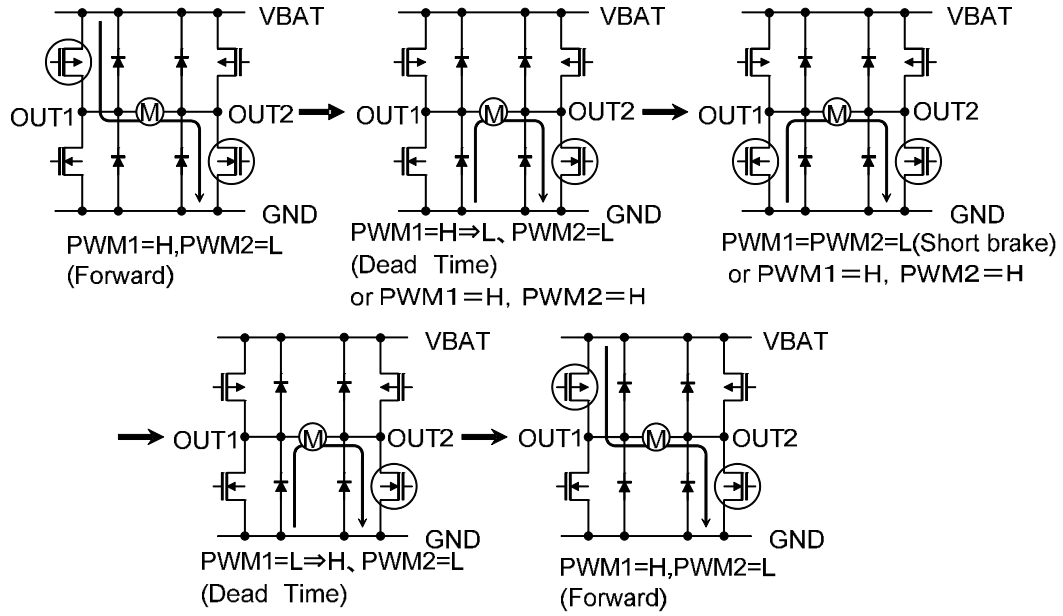
	PWM1	PWM2	EN	ENB	DIAG pin	OUT1	OUT2
Over-temperature detection (Note)	Output is OFF regardless of input signals.				**L**	**Z**	**Z**
Over-current detection (Note)					**L**	**Z**	**Z**
VBAT undervoltage detection					**L**	**Z**	**Z**
VCC undervoltage detection					**L**	**Z**	**Z**
VCC high voltage detection					**L**	**Z**	**Z**

Note: When the voltage is dropping less than the VBAT undervoltage, the over-temperature detection circuit holds the state before detecting VBAT. When the voltage is dropping less than the VBAT undervoltage, the Over-current detection circuit is forced to be undetected state.

Table 7.1-3 Output state

OUT	High-side Driver	Low-Side Driver
H	ON	OFF
L	OFF	ON
High-Z	OFF	OFF

(1) PWM function (in the case of Forward) (EN: H, ENB: L)

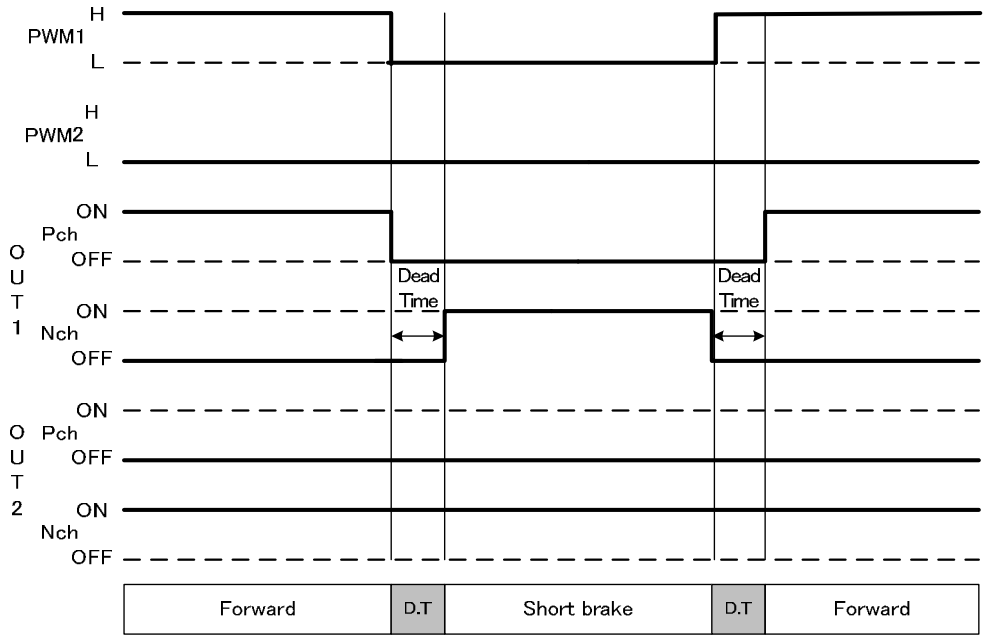


* The mark of a circle shows DMOS Tr which is ON.

Figure 7.1-1 Current flow at the time of PWM function (Forward)

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

- PWM function (Forward) timing chart (in the case of short brake operation, PWM1 = PWM2 = L)

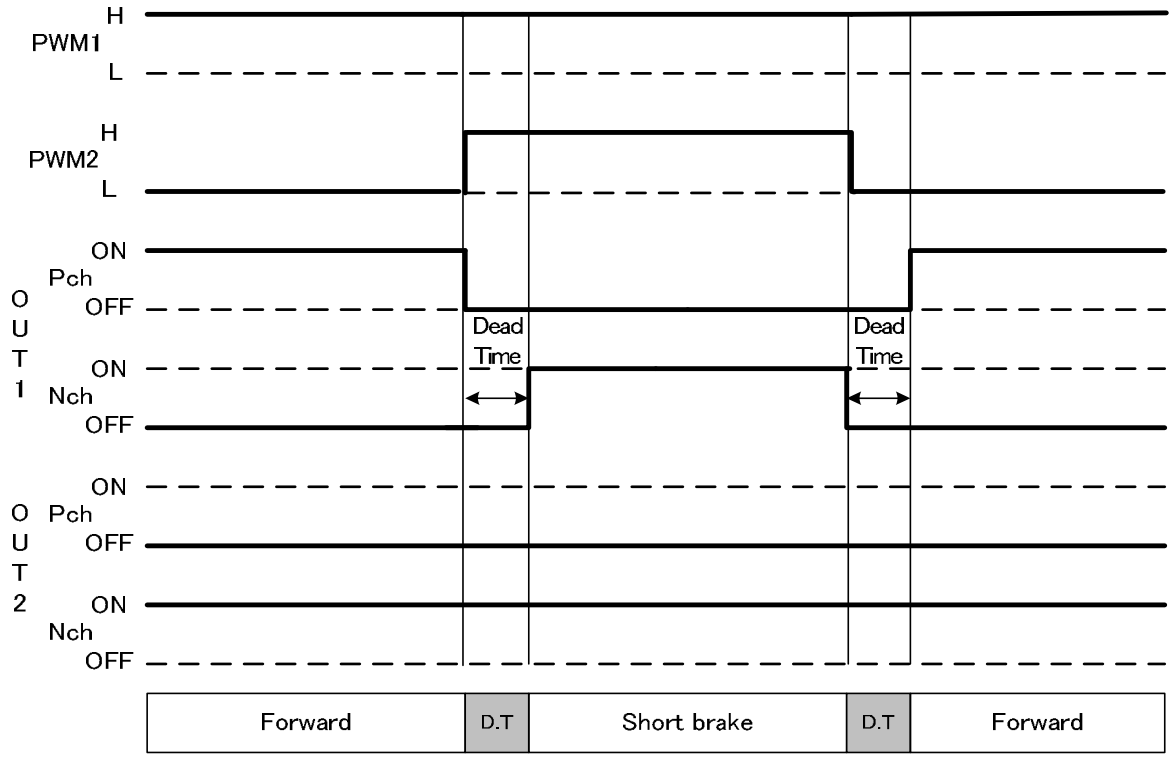


*D.T (Dead Time): In order to prevent the through current by simultaneous ON of Hi-side Pch Tr and Lo-side Nch Tr, Pch Tr off and Nch Tr off time (4 μs (typ.)) are prepared.

Figure 7.1-2 (1) Timing chart at the time of PWM function (Forward)

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

- PWM function (Foward) timing chart (in the case of short brake operation, PWM1 = PWM2 = H)

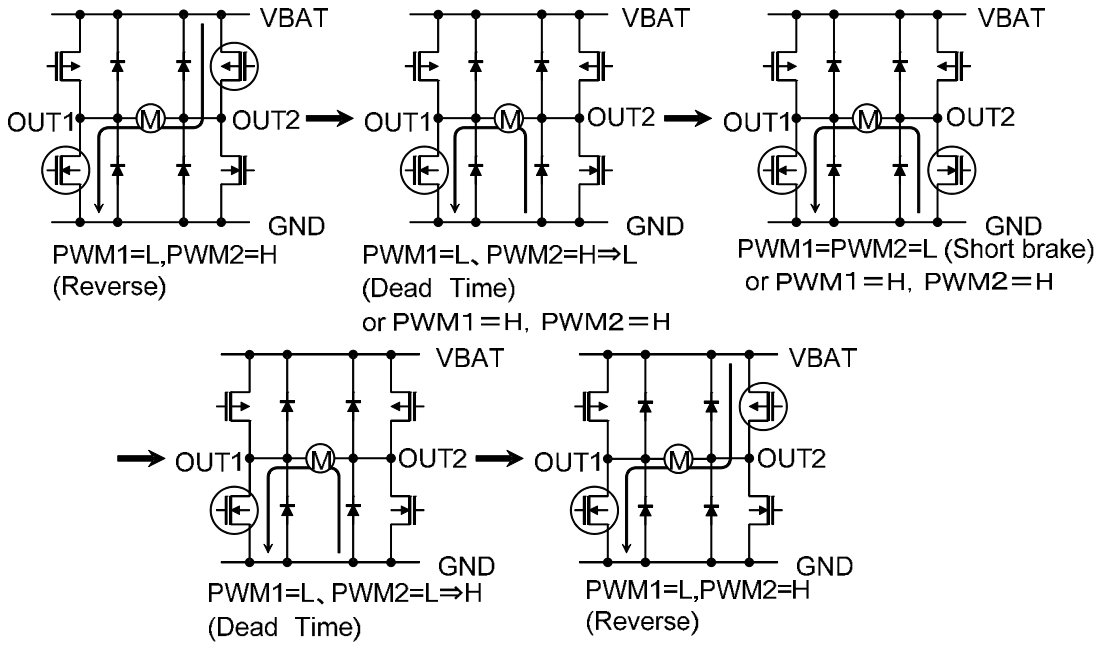


*D.T (Dead Time): In order to prevent the through current by simultaneous ON of Hi-side Pch Tr and Lo-side Nch Tr, Pch Tr off and Nch Tr off time (4 μs (typ.)) are prepared.

Figure 7.1-2 (2) Timing chart at the time of PWM function (Forward)

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

(2) PWM function (in the case of Reverse) (EN: H, ENB: L)

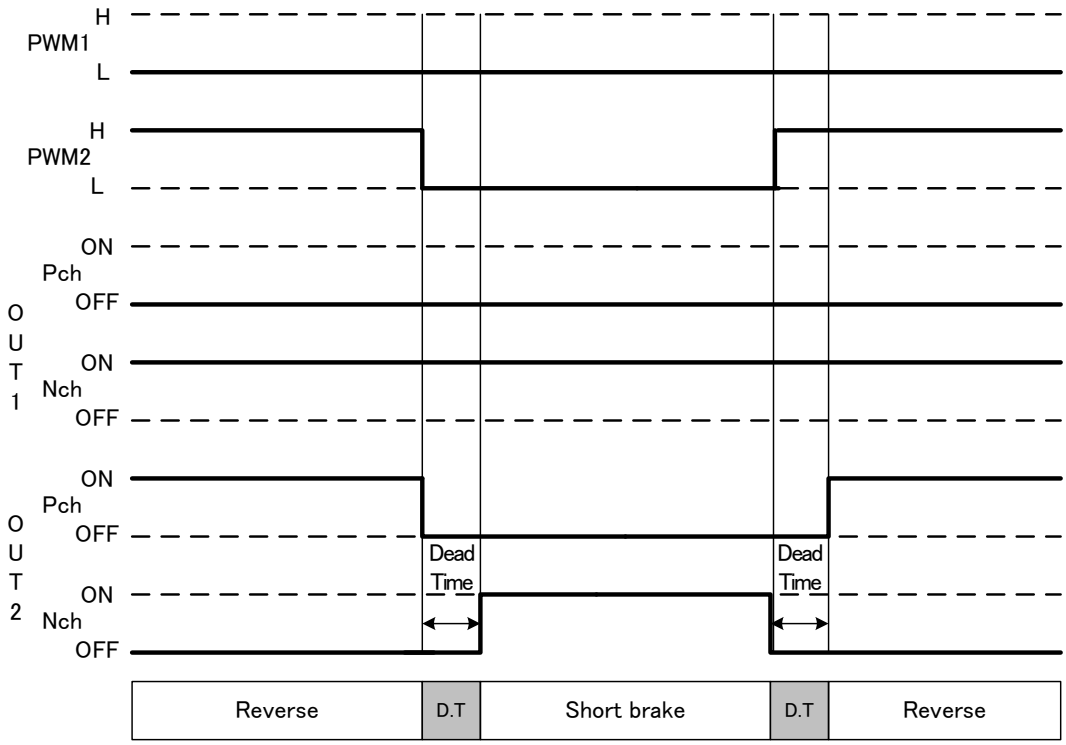


* The mark of a circle shows DMOS Tr which is ON.

Figure 7.1-3 Current flow at the time of PWM function (Reverese)

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

- PWM function (Reverse) timing chart (in the case of short brake operation, PWM1 = PWM2 = L)



*D.T (Dead Time): In order to prevent the through current by simultaneous ON of Hi-side Pch Tr and Lo-side Nch Tr, Pch Tr off and Nch Tr off time (4 μs (typ.)) are prepared.

Figure 7.1-4 (1) Timing chart at the time of PWM function (Reverse)

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes
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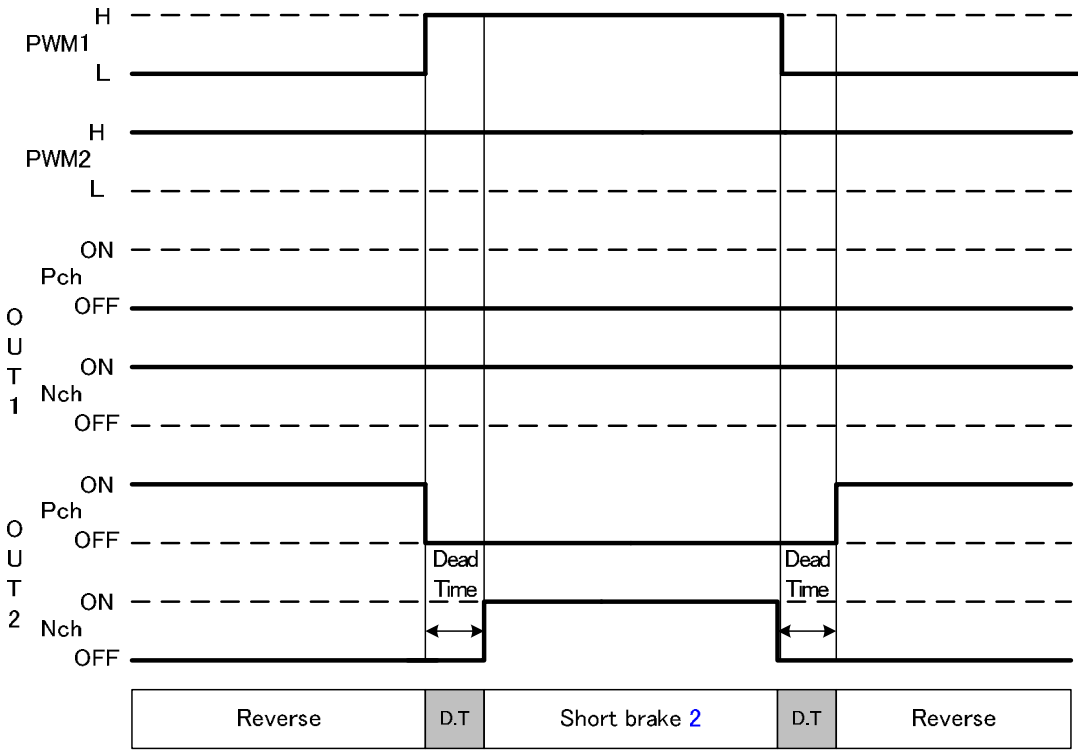
- PWM function (Reverse) timing chart (in the case of short brake function, PWM1 = PWM2 = H)



*D.T (Dead Time): In order to prevent the through current by simultaneous ON of Hi-side Pch Tr and Lo-side Nch Tr, Pch Tr off and Nch Tr off time (4 μs (typ.)) are prepared.

Figure 7.1-4 (2) Timing chart at the time of PWM function (Reverse)

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes

7.2. DIAG Output

This pin is an open drain type output pin and should be used connecting to a MCU power supply through a pull-up resistor. When the following errors occur, this pin outputs "L."

Table 7.2 DIAG function

Function		EN	ENB	DIAG	Motor drive output	
				Pin	OUT1	OUT2
Normal operation	Forward	H	L	H	H	L
	Reverse	H	L	H	L	H
	Short brake	H	L	H	L	L
	EN Disable	L	X	L	High-Z	High-Z
	ENB Disable	X	H	L	High-Z	High-Z
Error detection	At the time of VBAT undervoltage detection	X	X	L	High-Z	High-Z
	At the time of VCC undervoltage detection	X	X	L	High-Z	High-Z
	At the time of VCC high voltage detection	X	X	L	High-Z	High-Z
Error detection (DIAG output latch available) *1	At the time of over-temperature detection (TSD)	X	X	L	High-Z	High-Z
	At the time of over-current detection (Iovc)	X	X	L	High-Z	High-Z
Diagnosis operation (DIAG output latch available) *2	At the time of initial diagnosis, and restart diagnosis abnormality	X	X	L	*3	*3
	During initial diagnosis, and diagnosis restart operation	X	X	L	High-Z	High-Z
POR operation	At the time of VCC undervoltage POR detection	X	X	L	High-Z	High-Z

*1: For the clearing condition of the DIAG output latch, refer to Section 7.7.1 "DIAG function release operation after the over-temperature detection" at the time of the over-temperature detection. At the time of the over-current detection, refer to the Section 7.8.3 "Timing chart of restart from the motor output OFF state at the time of over-current detection."

*2: The clearing conditions of DIAG output latch are as follows: VCC undervoltage POR detection, EN Disable , and ENB Disable.

*3: In the case of initial diagnosis abnormality, or diagnosis restart abnormal value
In the diagnosis abnormality, when the abnormal state is fixed to VBAT undervoltage detection state, VCC undervoltage detection state, and VCC high voltage detection state, the motor drive output is in the abnormal state, and OUT1 and OUT2 output High-Z.
In the diagnosis abnormality, when the abnormal state is fixed to VBAT undervoltage undetection state, VCC undervoltage undetection state, and VCC high voltage undetection state, the motor drive output, OUT1 and OUT2 output according to Table 7.1-1 "Motor function."

*4: Each letter in Table 7.2 means; X: Don't care, H: High, L: Low, and High-Z: High impedance.

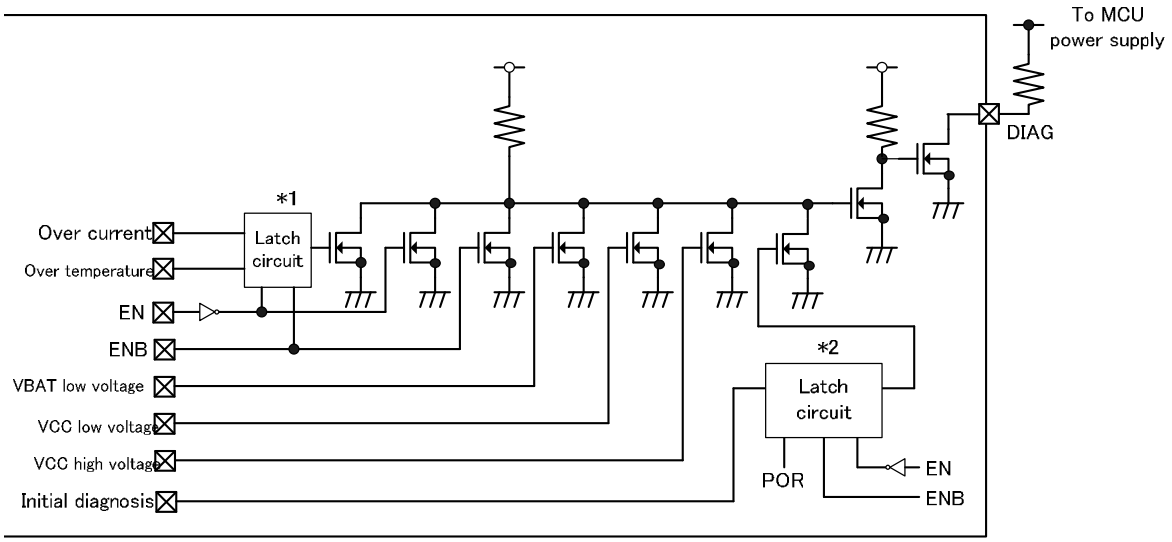


Figure 7.2-1 Example of DIAG output circuit configuration

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

In the case of the over-current detection and over-temperature detection, DIAG output is latched (*1) (the motor drive output becomes an OFF operation).

The “L” output latch (*1) of the DIAG pin is cleared with the rising edge of EN pin or the falling edge of ENB pin.

Moreover, for the VBAT and VCC voltage abnormality, they are returned automatically after returning normal voltage.
In the automatic returning operation, the DIAG output returns the normal operation in the response to the release voltage of each power supply monitoring function.

If the VCC voltage is dropping still in the abnormal state, “L” holding circuit holds the DIAG output = L.

DIAG=”L”(*2) is latched when set to fail situation in initial diagnosis and diagnostic restart operation. This latch (* 2) is cleared at VCC low voltage POR detection, EN Disable, or ENB Disable.

7.3. Current Limitation Control

This IC uses a chopper type control as a current limitation control. The current limitation control makes it operate in the large current flowing at the time of locking a motor when the motor shaft operation cannot be performed. Then the actuator is protected and the dissipation of this IC is reduced. (An additional over-current protection circuit is prepared in other block at the time of the power supply short or GND short.)
The current limitation comparator is arranged to the low side, and higher threshold is defined as Ilim-H, and lower one is defined as Ilim-L.
Moreover blanking time is prepared inside, and if exceeding the time, it will be considered that the current limitation is operated.
The value of Ilim-H is set to 6.5 A (typ.), and Ilim-L = Ilim-H - 0.25 A (typ.).

7.3.1. Chopper type current limitation control

The basic operation of chopper type current limitation is as follows.

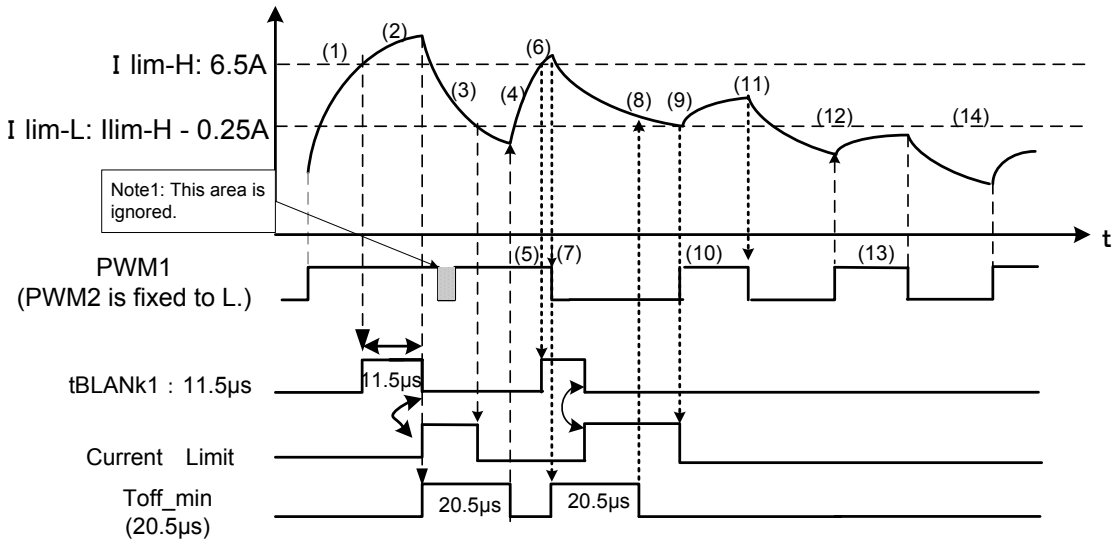


Figure 7.3-1 Chopper type current limitation control

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes

<Basic operaton>
(1) Current is detected with Ilim-H(6.5A).
(2) The Blanking counter starts counting after the detection. The Current Limit signal rises at the falling edge of tBLANK1 because the current flows more than Ilim-H(6.5 A) after passing the time (tBLANK1: 11.5 µs).
(3) After Blanking, the motor drive output is set to the short brake mode (lower simultaneous ON) automatically. Then the current is regained.
At the same time, Toff_min also rises to "H" and starts counting.
The PWM1 signal of Note1 is ignored in this case. (Toff_min is given the priority.)
(4) After passing the time of Toff_min (20.5 µs) the normal mode (Forward) returns if the value is lower than Ilim-L.
(5) The motor drive current is increasing because PWM1 becomes "H."

<When a PWM signal is input at the time of Forward>
(6) It is detected that the current flows more than Ilim-H (6.5 A) after restarting the motor operation at Toff_min falling edge.
tBLANK1(11.5 µs) counter starts.
(7) If PWM1 becomes "L" during Blanking, the motor output is set to the short brake (lower similtaneous ON), and the current is regained.
(8) The short brake is held because the current value after Toff_min (20.5 µs) is more than Ilm-L.
(9) The current Limit becomes "L" since the Ilim-L is detected, and the normal mode returns.
(10) Since the PWM holds "H", the motor drive current is increasing.

(11) Shift to the short brake mode at the PWM1 falling edge.
(12) The normal operation returns by PWM1 = H signal.
(13) Since PWM1 hold “H”, the motor drive current is increasing.
(14) Then the operation becomes the short brake mode operation, and the motor drive current is reduced by PWM1 = L signal.

7.3.2. Thermal Adjustment Function of Current Limitation Control

When the junction temperature Tj rises in the operation of the current limitation control circuit, the current limitation threshold falls to 2.5A (typ.) after detecting Twar temperature (150°C to 170°C).
The Ilim-L may be also lowered by falling of the threshold of Ilim-H.

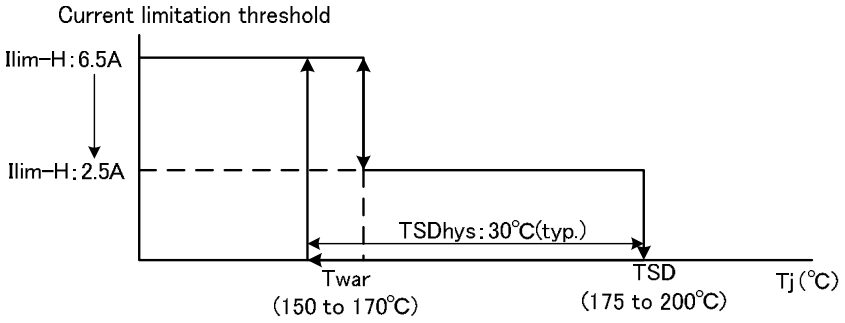


Figure 7.3-2 Thermal adjustment function of current limitation control

7.3.3. Current monitoring block at the time of current limitation control

It is detected at Low-side driver of the motor drive output.

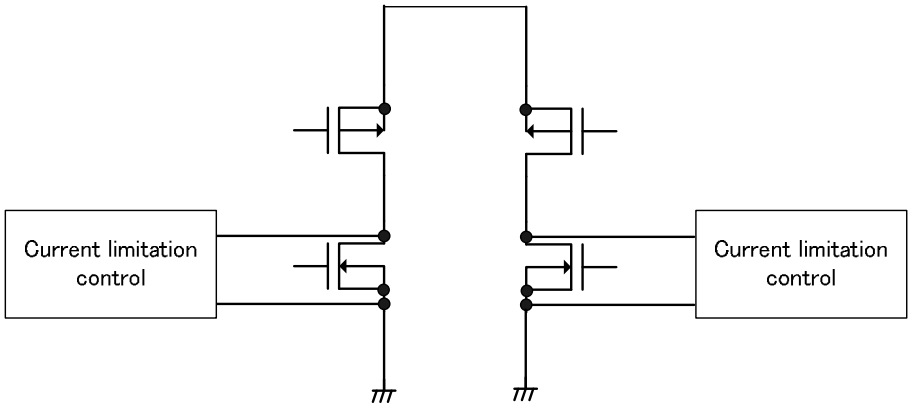


Figure 7.3-3 Current monitoring block at the time of current limitation control

Note: Some of the functional blocks of circuits in the block diagram may be omitted or simplified for explanatory purposes.

7.3.4. Operating flow

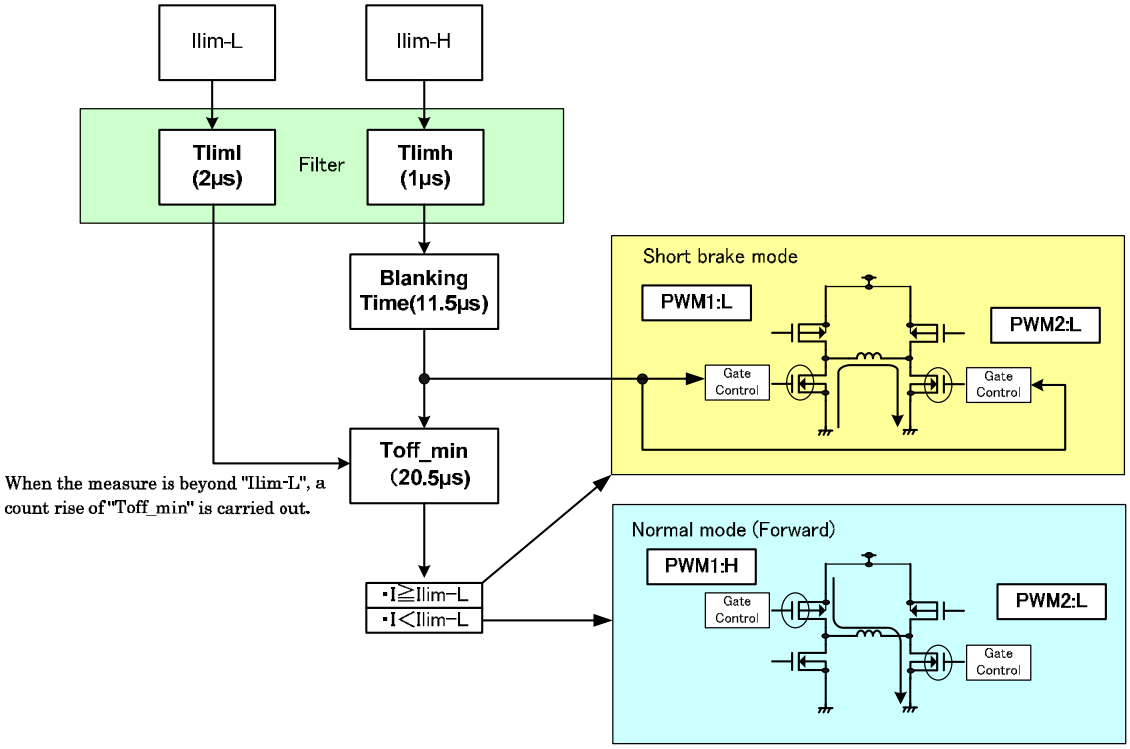


Figure 7.3-4 Operation flow of current limitation control circuit

Note: Some of the functional blocks or circuits in the block diagram may be omitted or simplified for explanatory purposes.

7.4. High-side current monitor: OCM pin

The current which flows to high side Tr (Pch) in H-bridge of motor-driven output (0A-6A) is monitored in real time. Then a current value of 0.223% (0 to 13.38mA) of its current value is output in aOCM pin. The current can be monitored by inserting an external resistance (220Ω*1) between OCM pin and GND. Additionally this voltage is input to MCU, and the motor state (such as motor lock, the load OPEN when operating, and angle detection of a throttle) can be monitored.

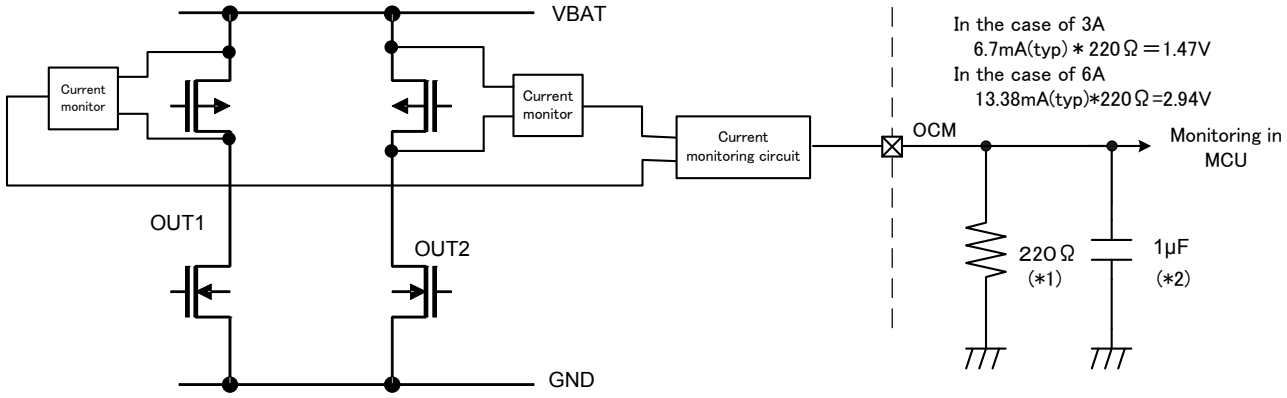


Figure 7.4-1 Block diagram of high-side current monitoring

Note: Some of the functional blocks or circuits in the block diagram may be omitted or simplified for explanatory purposes.

* This resistance (220Ω*1) assumes in the case that the power supply of MCU (ADC) is 5V.
  When the power supply of MCU is less than 5V, use adjusting of ressistance value.
  Be careful for the external resistance (220Ω). Sufficient evaluation is required since not only the resistance value fluctuates but also the output voltage also fluctuates.
* The external capacitor (*2) should select whether it connects according to the purpose of system use.
  For example, the operation in the case of flowing a current of 3A is as follows. However, repeating from forward to reverse is inhibited, and it assumes that the short brake is inserted between them and operated .

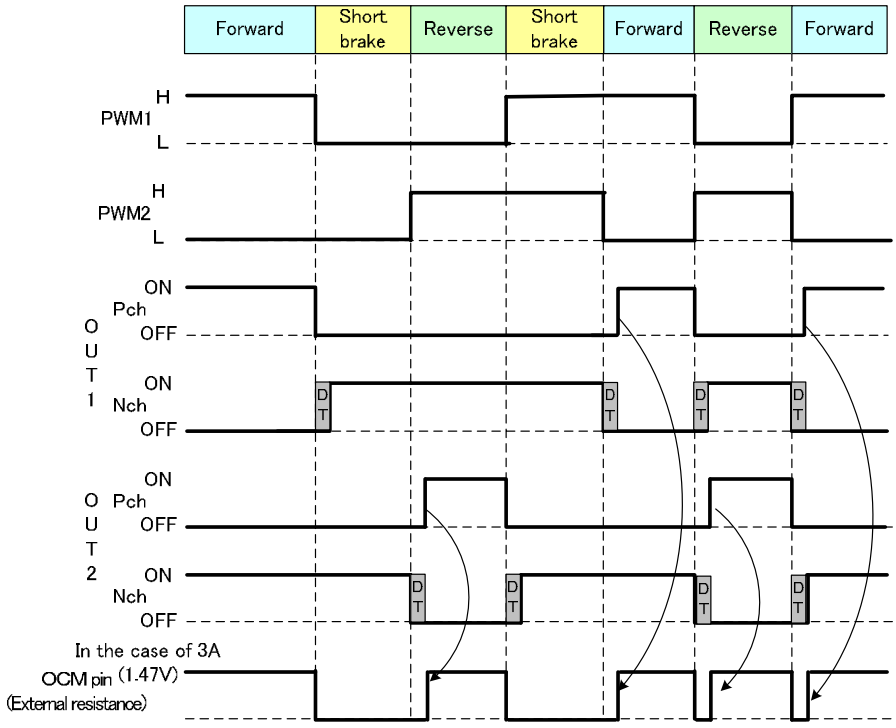


Figure 7.4-2 Timing chart of high-side current monitoring

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

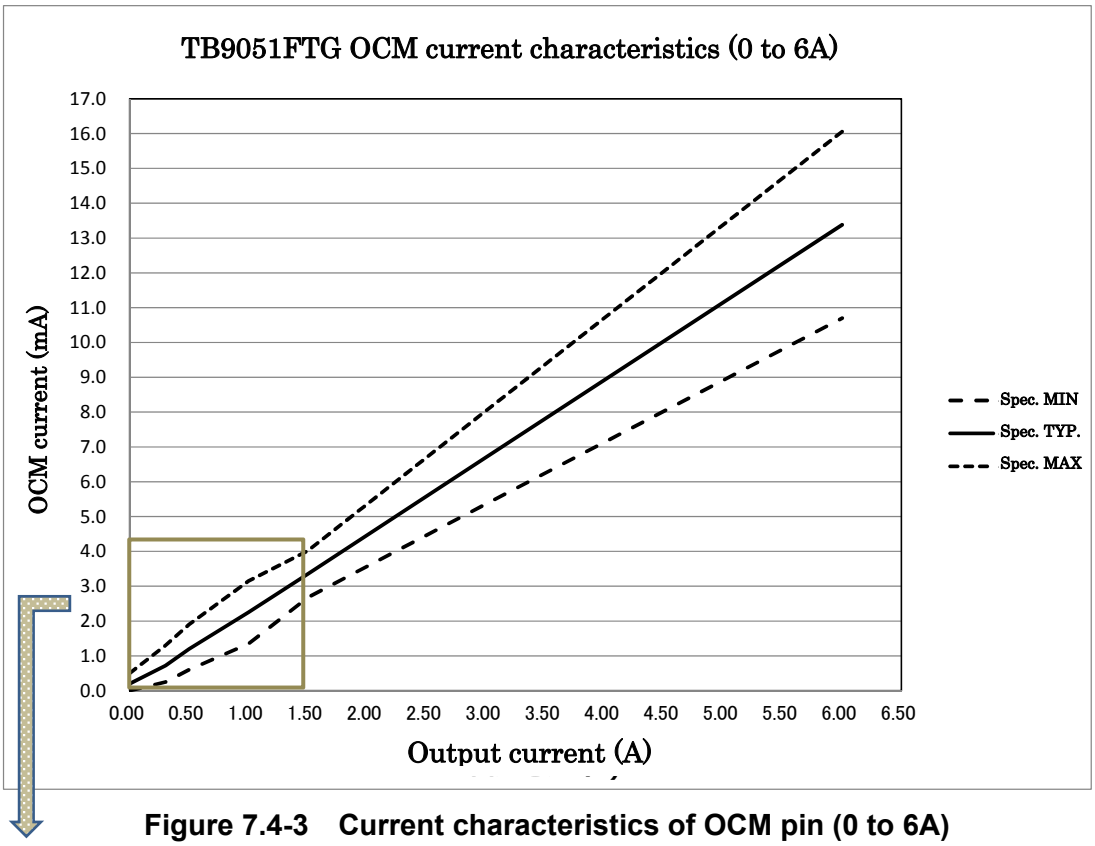


Figure 7.4-3 Current characteristics of OCM pin (0 to 6A)

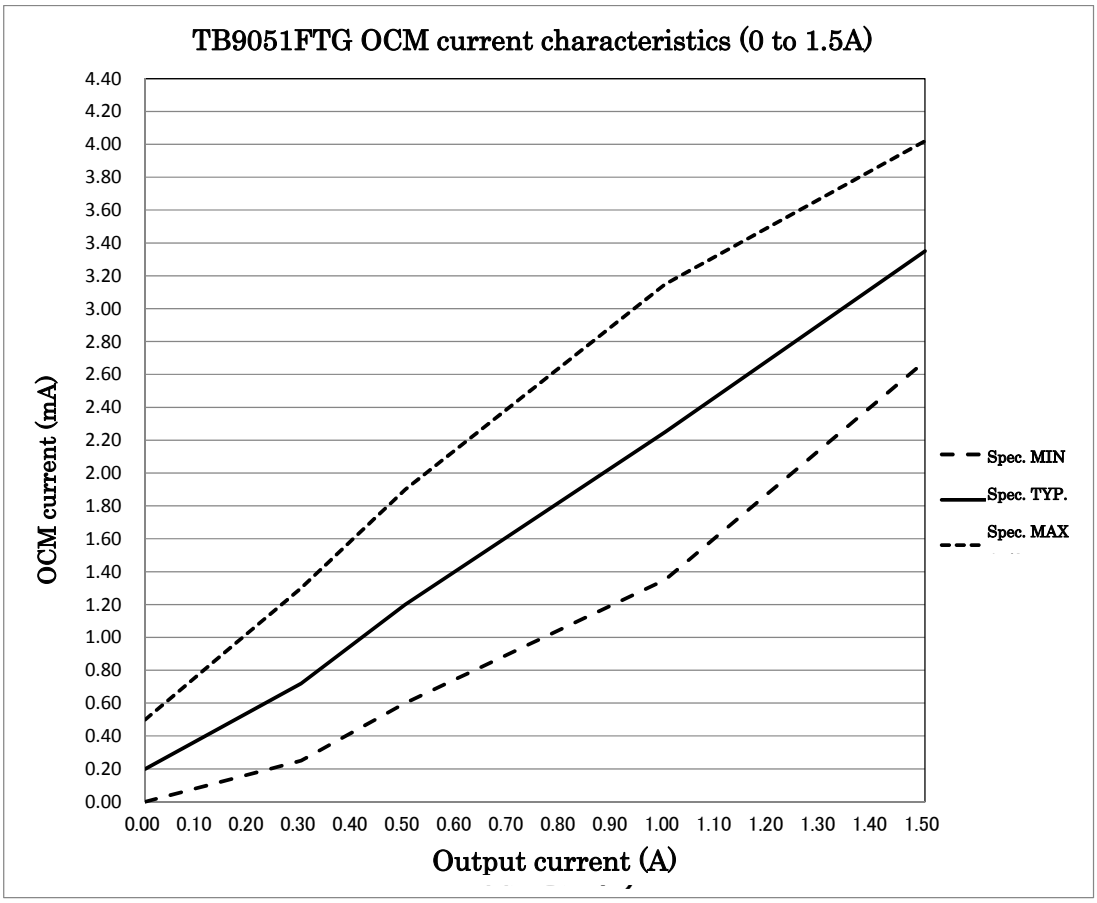
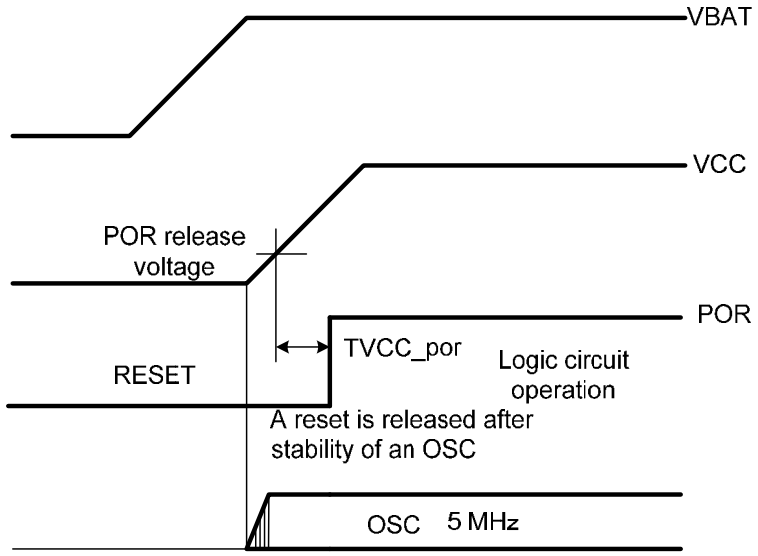


Figure 7.4-4 Current characteristics of OCM pin (0 to 1.5A)

7.5. OSC circuit (oscillation circuit)

An OSC circuit consists of CR oscillators of internal resistance and an internal capacitor, and performs a 5 MHz (typ.) oscillation.
Without a trigger of oscillation starting, a oscillation starts automatically according to the rise of supply voltage(VCC).



Fibure 7.5-1 Operation at the time of OSC circuit starting

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

7.6. Power supply monitoring function

This IC incorporates the power supply monitoring function.

7.6.1. VBAT undervoltage detection circuit

・When the VBAT voltage falls and becomes less than the low detection voltage, OUT1/2 becomes “OFF”(High-Z state).
Moreover, in order to prevent chattering, a filter (TVBAT_uv:2μs (typ.)) is built in. If the VCC voltage is more than the POR detecting voltage value of VCC undervoltage even when output is in the "OFF" (High-Z) state by undervoltage detection of VBAT, a Logic circuit is able to operate.

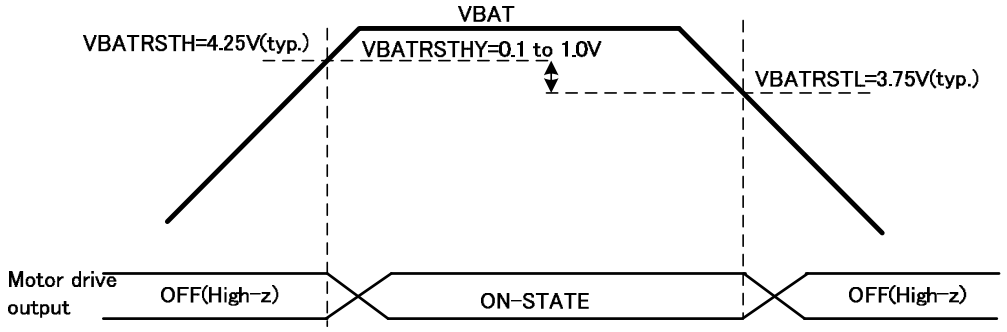


Figure 7.6.1-1 Threshold characteristics of VBAT undervoltage detection

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

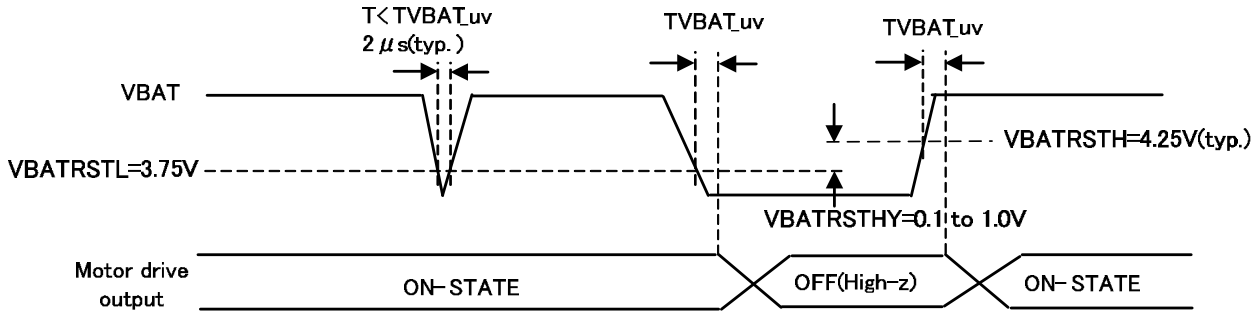


Figure 7.6.1-2 Timing chart of VBAT undervoltage detection

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

7.6.2. VCC undervoltage detection circuit

When the VCC voltage falls and becomes less than the low detection voltage, OUT1/2 becomes "OFF"(High-Z state).Moreover, in order to prevent chattering, a filter (TVCC_uv:2.5ms (typ.)) is built in. For a logic circuit, it is reset in the case of VCCRHL (3.07V (typ.)) or less. Moreover, in order to prevent chattering, a filter (TVCC_por:13.0 μ s (typ.)) is built in.

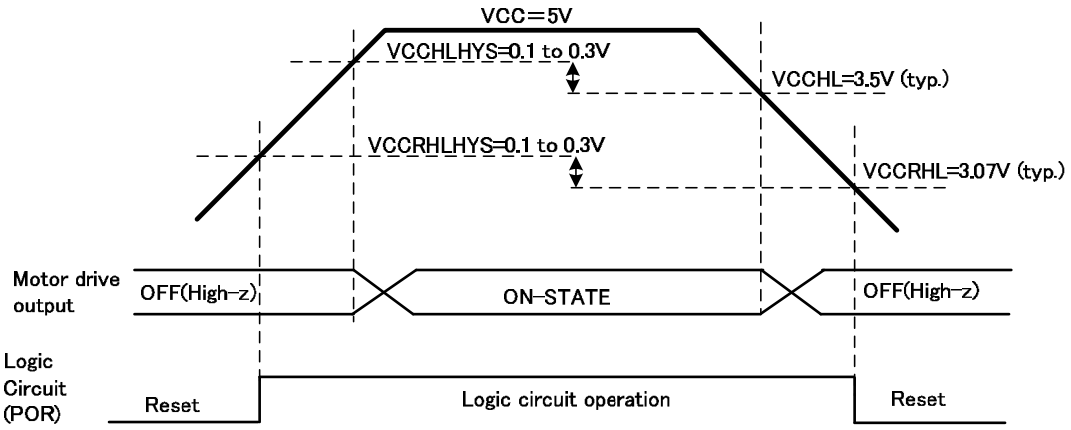


Figure 7.6.2-1 VCC undervoltage detection and POR threshold characteristics

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

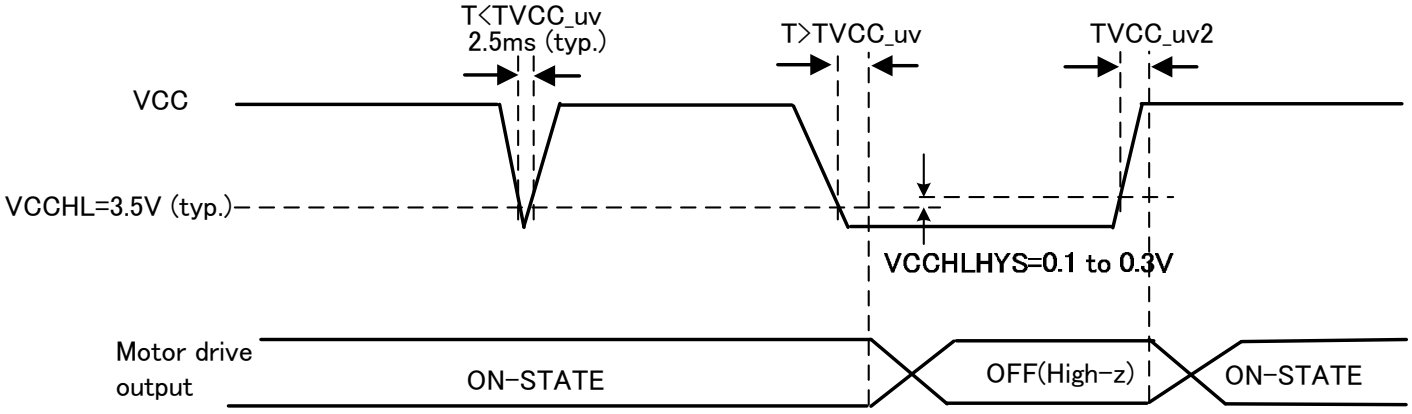


Figure 7.6.2-2 Timing chart of VCC undervoltage detection

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

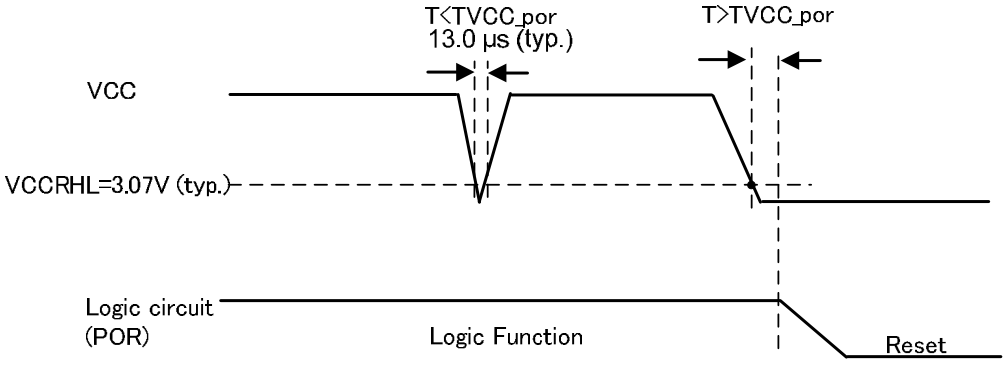


Figure 7.6.2-3 POR timing chart of VCC undervoltage

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

7.6.3. VCC high voltage detection circuit

When the VCC voltage rises and becomes more than the high detection voltage, OUT1/2 becomes "OFF"(High-Z state).
Moreover, in order to prevent chattering, a filter (TVCC_up:2.5ms (typ.)) is built in.
Even if the motor drive output is in the "OFF" (High-Z) state by a VCC high voltage detection, a logic circuit can operate.

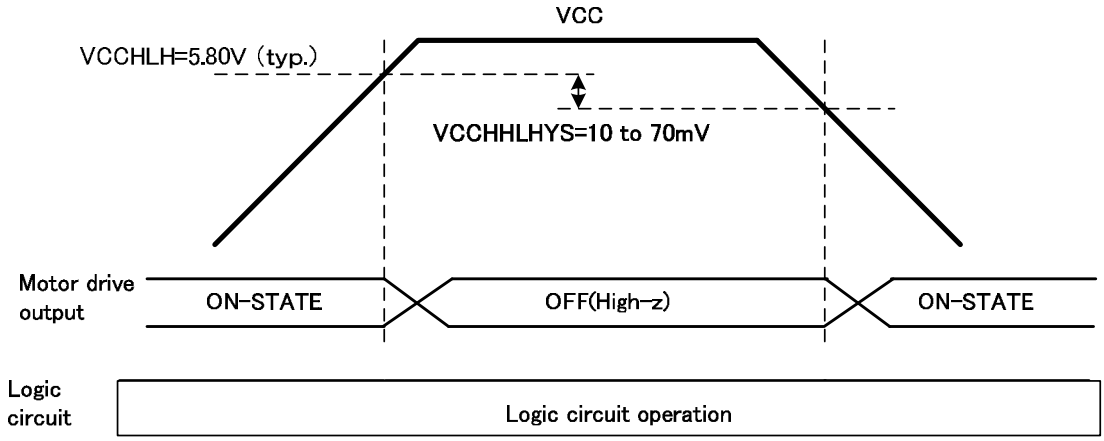


Figure 7.6.3-1 VCC high voltage detection circuit

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

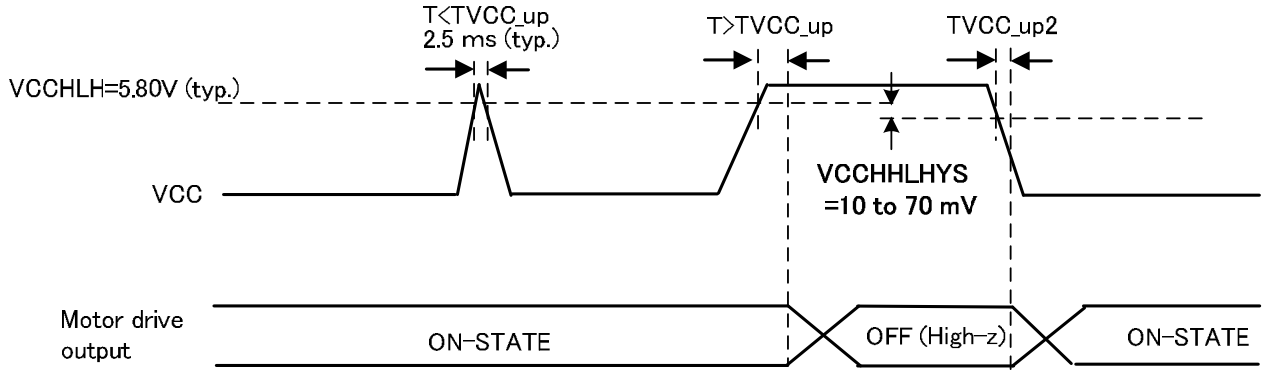


Figure 7.6.3-2 Timing chart of VCC high voltage detection

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

Note: The VCC high voltage detection function is not a function which clamps power supply voltage. The protection is required externally so that it may not become more than absolute maximum ratings.

7.6.4. DIAG function release after VBAT, VCC voltage abnormal function

For VBAT and VCC abnormal voltage, it returns automatically when being normal voltage.
The DIAG output returns a normal operation when the automatic return receives abnormal release signals from each power supply monitoring function.

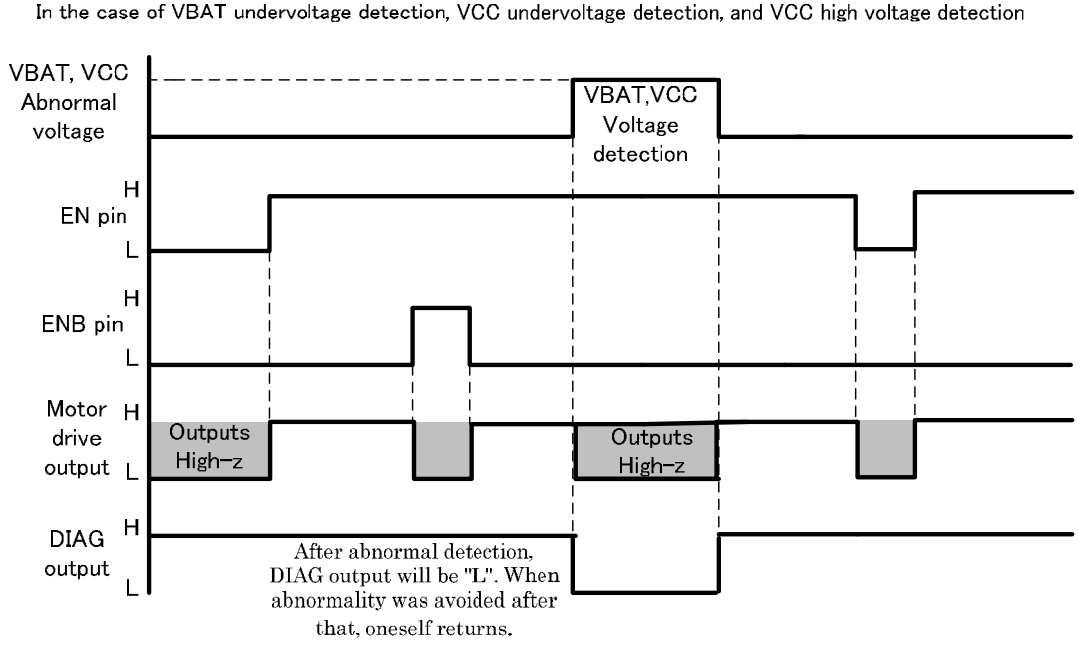


Figure 7.6-4 DIAG function when VBAT and VCC voltage is abnormal

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

7.7. Over-temperature detecion circuit

(1) This IC builds in the over-temperature detection circuit. When the temperature becomes more than TSD, the motor drive output, OUT1/2 changes to High-Z state, and the IC is protected.
(2) "L" is output from DIAG pin on this time.
(3) Moreover, even if temperature falls less than TSD-TSDhys by a functional operation of the over-temperature detection, the IC does not return automatically, and the output state holds latching High-Z.
(4) DIAG output pin also latches the abnormal state.
(5) "L" output latch state of DIAG pin is cleared with a rising edge of the EN pin or a falling edge of the ENB pin.
(6) For the chattering prevention at the time of over-temperature detection, a filter circuit is built-in.

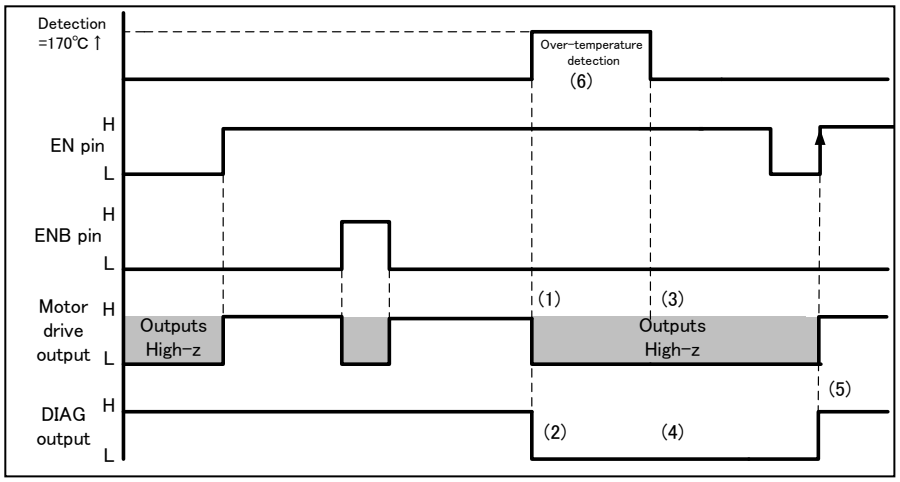


Figure 7.7 Timing chart of over-temperature detection operation

Note: When detection signals of the over-temperature detection circuit become less than the VBAT undervoltage, the state before the VBAT detection is held.
The detection signals of over-temperature detection circuit are made into undetected state forcibly during an initial diagnosis and a re-start.
Note: PWM input is not available at the time of TSD generation.

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

Note: The guarantee storage temperature range of the absolute maximum ratings of this product is maximum 150°C. The storage and use exceeding this temperature are not guaranteed a normal operation of the IC. It also may occur smoke and fire. Do not store and use exceeding this temperature in any cases.
Moreover although this IC builds in the over-temperature detection function, this function is not a function of which the temperature of this IC is suppressed less than thermal shutdown temperature.
This function is out of operation guarantee ranges and provided as an auxiliary only.
(For this function, the TEST is not performed with actual difference in temperature individually. Only detection circuit operation is confirmed tentatively by the TEST function.)

7.7.1. DIAG function release operation after the over-temperature detection

L output latch of DIAG pin is cleared at the rising edge of EN pin or the falling edge of ENBpin.

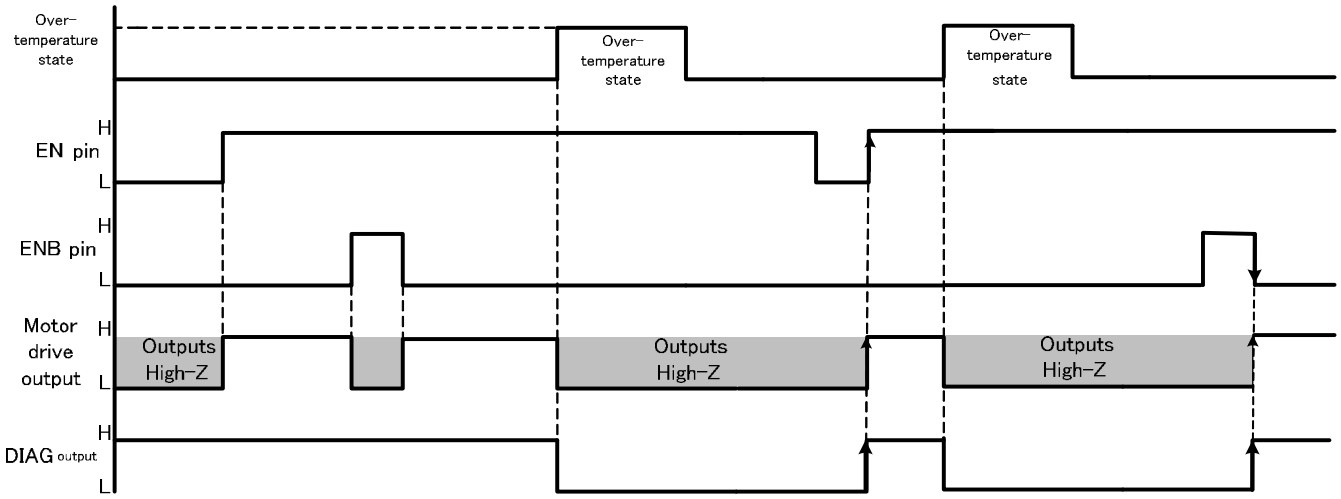


Figure 7.7-1 DIAG function in the over temperature detection

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

7.8. Over-current detection circuit at the time of power supply short, GND short, and load short

This IC incorporates the over-current detection for High-side and Low-side of each motor drive output driver.
Therefore, if each motor drive output pin is short to the power supply, short to GND, and a load short, then the over-current threshold(11A(typ.)) is exceeded, the over-current detection circuit operates and lets the motor drive output OFF. All drivers of High-side/Low-side of OUT1/OUT2 pin become "OFF."
Moreover “L” is output from DIAG pin simultaneously.
Setting OCC (Over Current Control) pin to “H” or “L” enables correspondence to two modes.
Note: If detection signals of over-current detection circuit are less than the VBAT undervoltage, they are forced to be undetected state.
Detection signals of over-current detection circuit are forced to be undetected state during an initial diagnosis and a re-start.

7.8.1. In the case of OCC; H

- When the motor drive output is short to power supply or short to GND, tBLANK2 = 1μs is set to the threshold of over-current (Iovc), and the prevention time of the malfunction is set by noise. Then if a current flows longer than the setting time, the output is in the OFF state. After passing 500 ms (typ.), it returns automatically and repeats operations until instructions from external MCU. The OUT1/OUT2 outputs return the normal operation when an output current is in the normal range at the time of automatic returning.
- The output is in the OFF state by instructions from MCU.
  The signals from MCU are output to EN/ENB signals, and they perform OFF operation.
- For returning from OFF state, each function restarts according to input instructions from MCU.
  Each function re-starts with one pulse signal of EN falling or one pulse signal of ENB rising.
- When tBLANK2 operates, tBLANK1 is ignored, and give priority to tBLANK2 and operate.
  (For tBLANK1, refer to the section 7.3.1 . Chopper type current limitation control.)

<In the case of OCC pin; H 1 (Example: Low-side)>

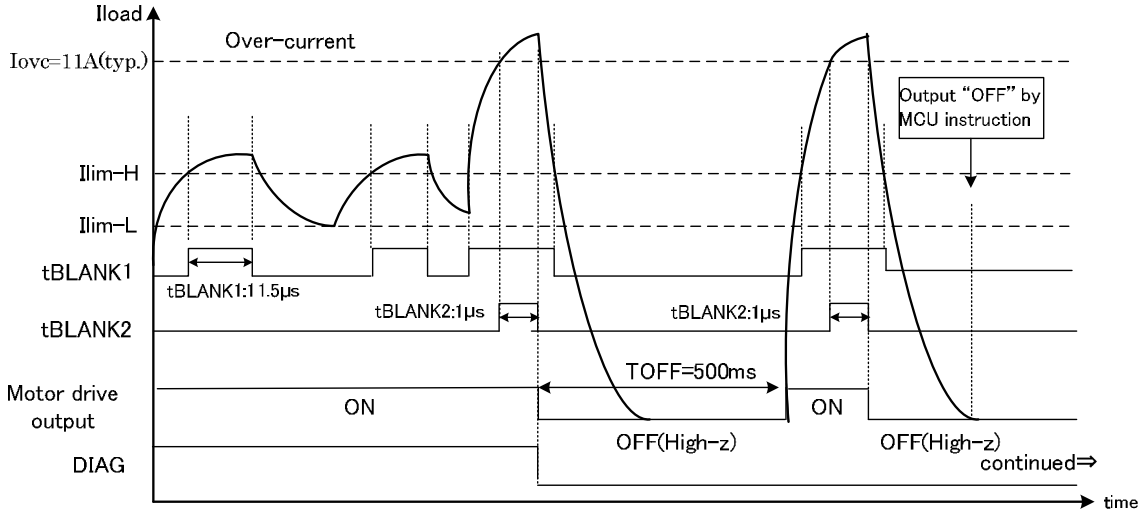


Figure 7.8-1 (1) Timing chart 1 (OCC = High) of current limitation detection operation at the time of short to power supply, short to GND, and load short

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

<In the case of OCC pin; "H" 2 (Example: Low-side)>

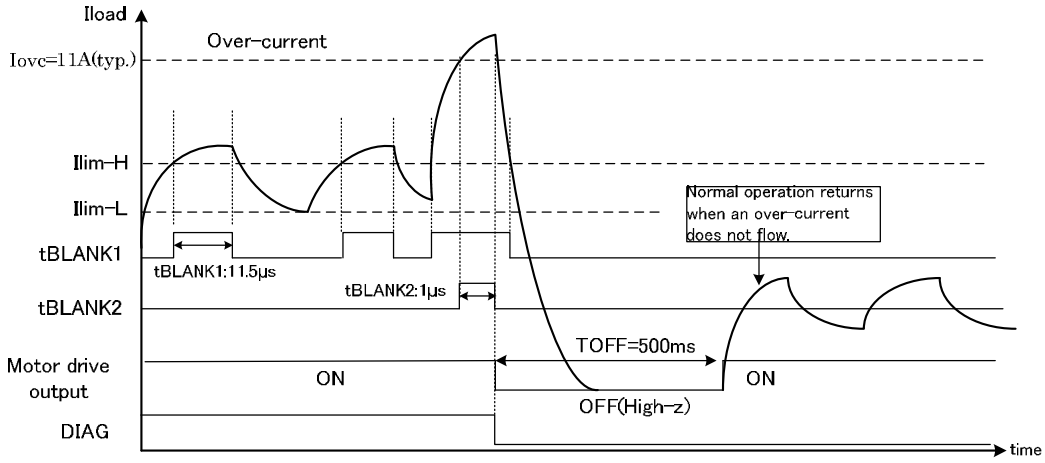


Figure 7.8-1 (2) Timing chart 2 (OCC = High) of current limitation detection operation at the time of short to power supply, short to GND, and load short

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

7.8.2. In the case of OCC; L

- When the motor drive output is short to power supply or short to GND, tBLANK2 = 1µs (Tovc) is set to the threshold of over-current (Iovc), and the prevention time of the malfunction is set by noise. Then if a current flows longer than the setting time, the output is in the OFF state.
- For returning from OFF state, each function restarts according to input instructions from MCU. Each function re-starts with one pulse signal of EN falling or one pulse signal of ENB rising.
- When tBLANK2 operates, tBLANK1 is canceled.

<In the case of OCC pin; "L" (Example: Low-side)>

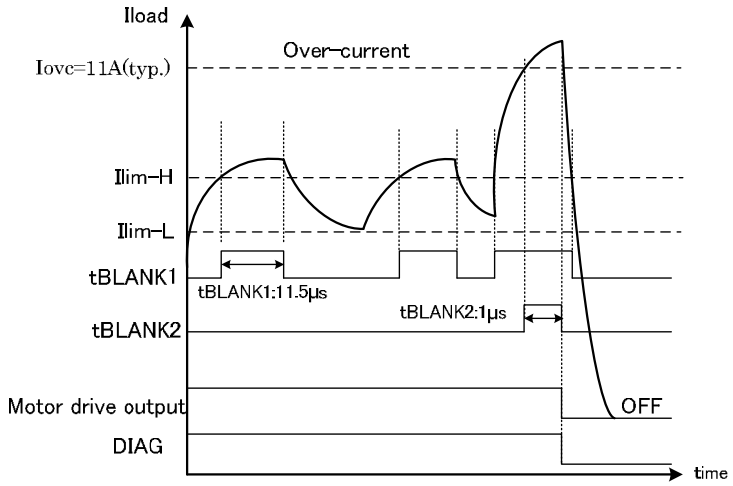


Figure 7.8-2 Timing chart 2 (OCC = Low) of current limitation detection operation at the time of short to power supply, short to GND, and load short

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

7.8.3. Timing chart of restart from the motor output OFF state at the time of over-current detection

L output latch state of the DIAG pin is cleared at the rising edge of EN pin and falling edge of ENB pin.

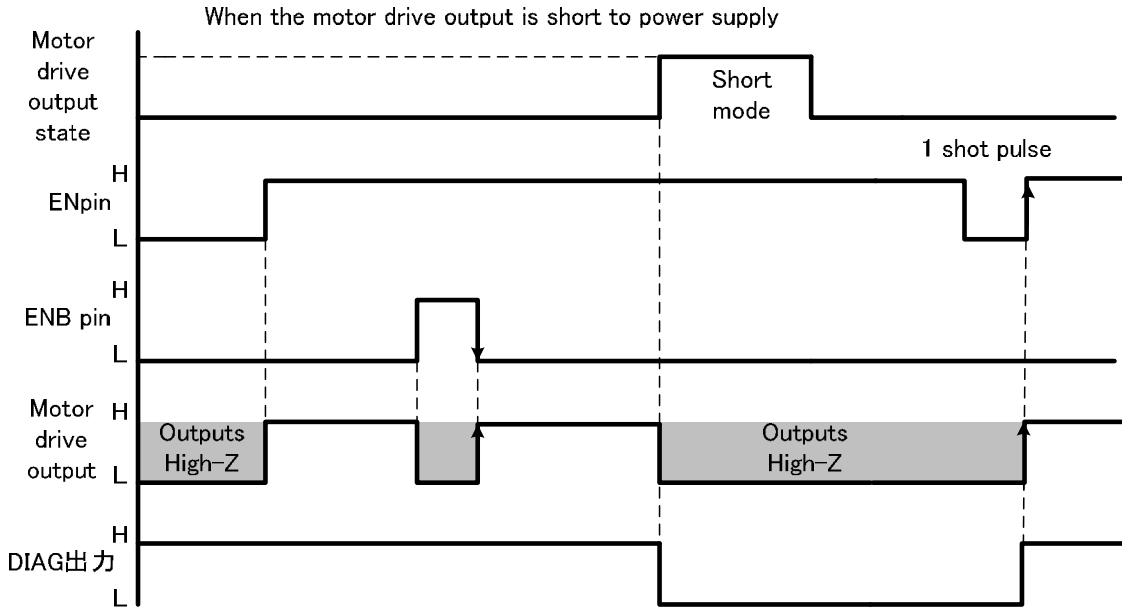


Figure 7.8-3 Timing chart of returning from OFF state at the time of short to power supply, short to GND, and load short

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

Note: This detection circuit is a function to avoid abnormal conditions such as output short-circuit, temporarily and does not guarantee that the IC does not break. Therefore utmost care is necessary in the design of output lines, VBAT, VCC and substrate leading of GND traces since the IC may be destroyed by short-circuiting to the power supply or ground.

7.9. Regeneration operation

At the time of VBAT voltage detection operation, VCC high voltage detection operation, VCC voltage detection operation, TSD detection operation, and over-current detection operation, before a High-Z output, regeneration operation that sends a coil current for outputs (OUT1, OUT2) to VBAT and a GND pin are put into effect to suppress the reverse electromotive current.

Regeneration operation has two kinds of operation, those are low side regeneration operation (OUT1 Nch ON, OUT2 Nch ON) and high side regeneration operation (OUT1 Pch ON, OUT2 Pch ON).

High side regeneration operation (OUT1 Pch ON, OUT2 Pch ON) is done regeneration operation at the time of OUT1/OUT2 short to the power supply. At the time of other detection operations, it becomes low side regeneration operation (OUT1 Nch ON, OUT2 Nch ON).

Note: When the VCC voltage falls and the VCC undervoltage POR detection is detected, the regeneration is not operated and an output is set to the High-Z state.

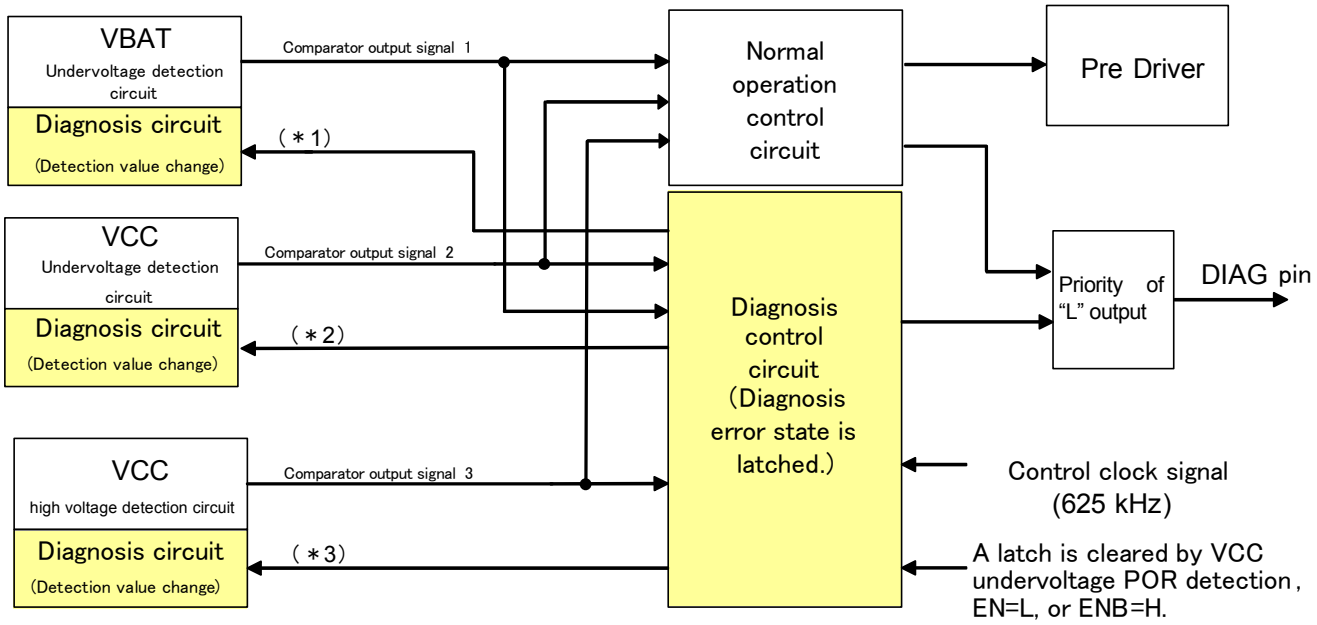
Note: When Pch over-current detection and Nch over-current detection occur, OUT1 and OUT2 output are all in "OFF" state.

7.10. Initial diagnosis and diagnostic restart sequence operation

The diagnosis function, which changes threshold and checks operations of each comparator of the power supply monitoring circuits (VBAT undervoltage detection, VCC undervoltage detection, and VCC high voltage detection) in the normal or abnormal state, is built-in.
The conditions to start diagnosis function are two kinds. One starts when VBAT power supply and VCC power supply are turned on (initial diagnosis). The other starts when EN:H state and ENB:L state are changed to EN: L and ENB:H, and the IC is in the Disable state (diagnosis restart).

The initial diagnosis starts when each comparator of the power supply monitoring circuit is in the normal state (undetected state) after power supply startup VCC undervoltage detection POR release. When the VBAT power supply and VCC power supply startup is too late, it starts after waiting until each comparator is in the normal state (undetected state).

Diagnostic restart starts when the IC is in the Disable state by EN pin or ENB pin and each comparator of the power supply monitoring circuit is in the normal state (undetected state). The diagnostic time of initial diagnosis and a diagnostic restart is about 80 μs.
During diagnostic operation, EN and an ENB pin input are not received any signal, OUT1 and OUT2 output turn into a High-Z output, and DIAG output becomes “L” output. In the termination of diagnostic operation, when "H" is input to a EN pin and "L" is input to a ENB pin, a check result is output in the DIAG pin. When a comparator circuit is a normal performance, H output of DIAG is done, and when there is unusual operation, L output of DIAG is done.“L” output of the DIAG is latched in the initial diagnosis control circuit. The latch result is latched until VCC undervoltage POR detection or diagnosis restart operation.



*1 to 3: Threshold change signal of initial diagnosis and normal operation (same as diagnositic restart)
H: Threshold for diagnosis => “detected state” at VCC and VBAT normal voltage
L: Threhosld for normal operation => “undetected state” at VCC and VBAT normal voltage

Figure 7.10-1 Configuration figure of initial diagnosis and diagnostic restart sequence operation

Note: When a startup of VBAT power supply or VCC power supply in the initial diagnosis operation is too late, the "undetected" and "detected" may occur, the initial diagnosis may be failure, and the DIAG may be "L" output by influence of power supply fluctuating. In this case, comparator diagnosis should be performed again with the diagnostic restart function.

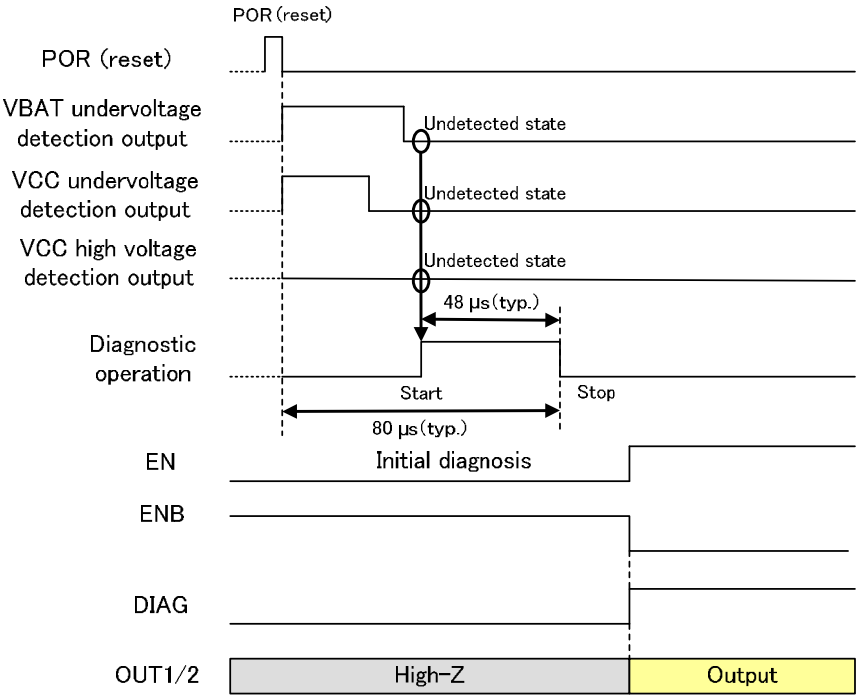


Figure 7.10-2 Initial diagnosis operation

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

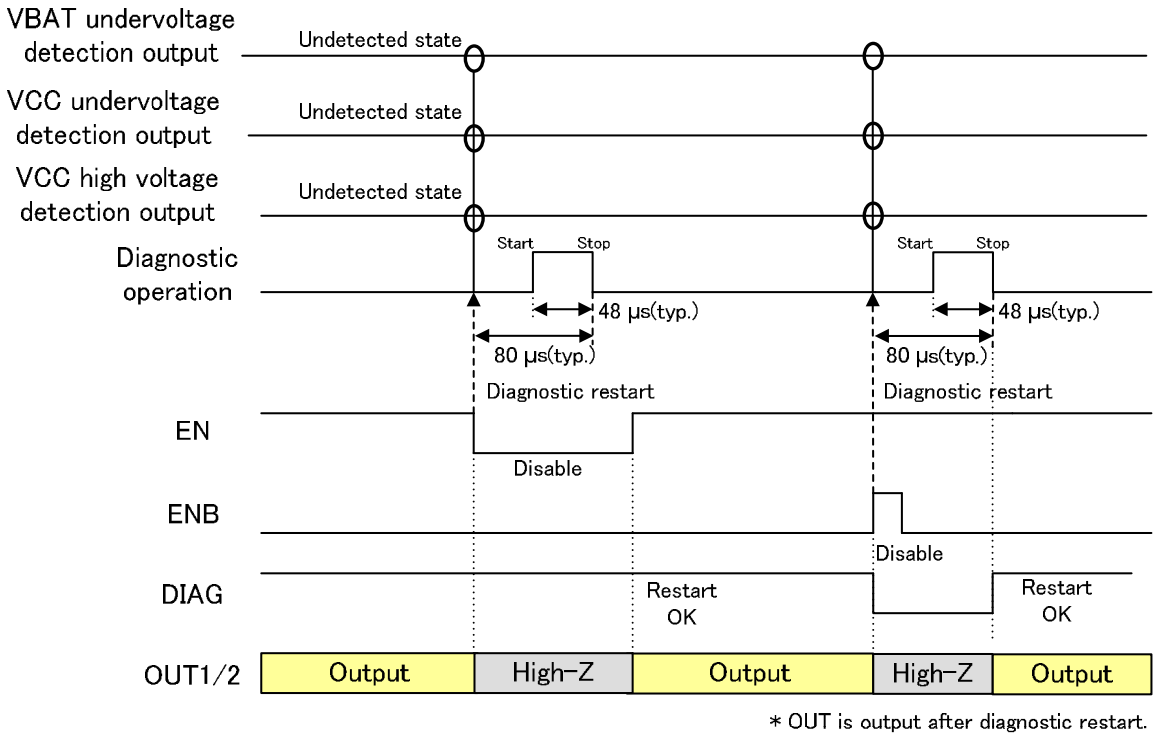


Figure 7.10-3 Diagnostic restart operation

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

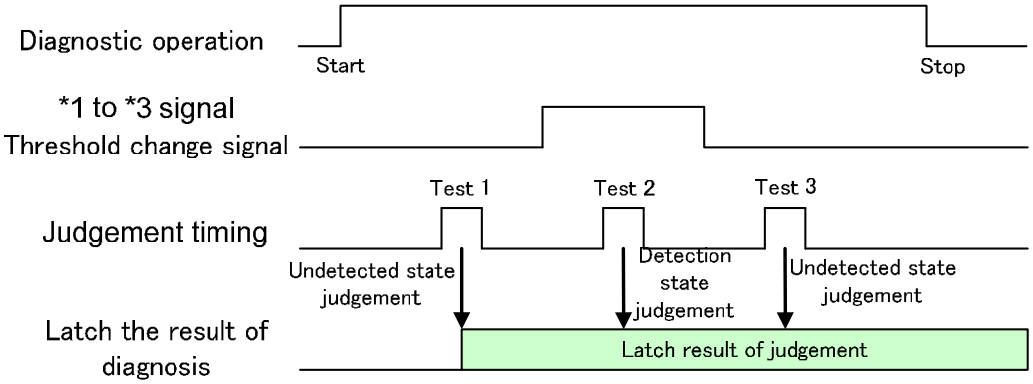


Figure 7.10-4 Description of diagnositic operation

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

Condition	Each detector	Start-after POR formation conditions	The state where it does not detect Test 1 (Normal threshold)	The state where it does not detect Test 2 (A threshold is changed)	The state where it does not detect Test 3 (Normal threshold)	Diagnostic result	Under diagnostic operation		After termination of initial diagnostic		Memo
							DIAG PIN	OUT1/2 PIN	DIAG PIN	OUT1/2 PIN	
1	VBAT Low voltage	○	○	○	○	Normal	L	High-z	H	Output Function	
	VCC Low voltage	○	○	○	○						
	VCC High voltage	○	○	○	○						
2	VBAT Low voltage	○	In the case of NG, it is also at any 1 conditions.	○	○	Abnormal	L	High-z	L	Output Function	
	VCC Low voltage	○		○	○						
	VCC High voltage	○		○	○						
3	VBAT Low voltage	○	○	In the case of NG, it is also at any 1 conditions.	○	Abnormal	L	High-z	L	Output Function	
	VCC Low voltage	○	○		○						
	VCC High voltage	○	○		○						
4	VBAT Low voltage	○	○	○	In the case of NG, it is also at any 1 conditions.	Abnormal	L	High-z	L	Output Function	
	VCC Low voltage	○	○	○							
	VCC High voltage	○	○	○							
5	VBAT Low voltage	When at least one condition continues the state where it does not detect	–	–	–	Abnormal	L	High-z	L	High-z	Initial diagnosis does not start. It becomes an unusual function of Table 7.1-2.
	VCC Low voltage		–	–	–						
	VCC High voltage		–	–	–						

Table 7.10-5 Summary of initial diagnostic operation

Notes of Table 7.10-5

* "○" means normal value (undetected state), and "-" means that a test is not performed.
* In the case of 5, three detection circuits continue waiting until being normal value (undetected state). When it becomes normal value, diagnosis operation starts at that timing, and end the initial diagnosis for about 48 μs.
* It does not operate with voltage less than the VCC undervoltage POR detection voltage.

Condition	Each detector	Initial diagnostic restart formation conditions	The state where it does not detect Test 1 (Normal threshold)	The state where it does not detect Test 2 (A threshold is changed)	The state where it does not detect Test 3 (Normal threshold)	Diagnostic result	Under diagnostic operation		After termination of a restart		Memo
							DIAG PIN	OUT1/2 PIN	DIAG PIN	OUT1/2 PIN	
1	VBAT Low voltage	○	○	○	○	Normal	L	High-z	H	Output Function	
	VCC Low voltage	○	○	○	○						
	VCC High voltage	○	○	○	○						
2	VBAT Low voltage	○	In the case of NG, it is also at any 1 conditions.	○	○	Abnormal	L	High-z	L	Output Function	
	VCC Low voltage	○		○	○						
	VCC High voltage	○		○	○						
3	VBAT Low voltage	○	○	In the case of NG, it is also at any 1 conditions.	○	Abnormal	L	High-z	L	Output Function	
	VCC Low voltage	○	○		○						
	VCC High voltage	○	○		○						
4	VBAT Low voltage	○	○	○	In the case of NG, it is also at any 1 conditions.	Abnormal	L	High-z	L	Output Function	
	VCC Low voltage	○	○	○							
	VCC High voltage	○	○	○							
5	VBAT Low voltage	When at least one condition continues the state where it does not detect	—	—	—	Abnormal	L	High-z	L	High-z	It does not restart. It becomes an unusual function of Table 7.1-2.
	VCC Low voltage		—	—	—						
	VCC High voltage		—	—	—						

Table 7.10-6 Summary of diagnostic restart operation

Notes of Table 7.10-6

* "○" means normal value (undetected state), and "-" means that a test is not performed.
* In the case of 5, three detection circuits continue waiting until being normal value (undetected state). When it becomes normal value, diagnosis operation starts at that timing, and end the restart diagnosis for about 48 μs.
* It does not operate with voltage less than the VCC undervoltage POR detection voltage.

8. Absolute maximum ratings

Table 8.1 Absolute maximum ratings

(Unless otherwise specified, Ta = 25°C)

Parameter	Symbol	Pin name	Condition	Rating	Unit
Power supply voltage	VBAT	VBAT	DC	-0.3 to +28.0	V
			Transient: 0.5 s	-0.3 to +40.0 (Note 5)	
	VCC	VCC	DC (Note 3)	-0.3 to +6.0 (Note 6)	
Input voltage	VIN	PWM1, PWM2, EN, ENB, OCC	DC	-0.3 to VCC+VF and VCC+VF≤+6.0 (Note 6)	
		TEST1, TEST2	DC	-0.3 to VCC+VF and VCC+VF≤+6.0 (Note 6)	
Output voltage 1	VOUT	DIAG	DC	-0.3 to +6.0 (Note 6)	
Output voltage 2		OCM	DC	-0.3 to VCC (Note 6)	V
Output voltage 3		OUT1, OUT2	DC, (Note4)	-VF to VBAT+VF and VBAT+VF≤+40.0 (Note 5)	V
Output voltage 4		OUT1, OUT2	DC, VBAT-OUT1/2, (Note4)	-VF to +40.0	V
Output current 1	IOUT	OUT1, OUT2	(Note 2)	Over-current detection current	A
Output current 2		DIAG		+2.5	mA
Output current 3		OCM		-18.0	mA
Storage temperature	Tstg	-	-	-55 to +150	°C
Lead temperature and time	Tsol	-	At the time of manual soldering	260 (10 s)	
Power dissipation	PD	-	JEDEC board (4 layers), (Note 7)	4.7	W

* For the current items, the current flowed into the IC is described plus, and the current flowed out from the IC is described minus.

Note 1) Do not exceed the maximum ratings including in Back EMF.
Absolute maximum ratings:
The maximum rating is the rating that should never be exceeded, even for a shortest of moments.
If the maximum rating is exceeded, it could result in damage and/or deterioration of the IC as well as other devices beside the IC. Regardless of the operating conditions, please design so that the maximum rating is never exceeded. Please use within the specified operating range.

Note 2) For using with continuous output current, use after considering the heat design of the board and evaluating enough so that the junction temperature should be within 150°C.

Note 3) The power supply for VCC of 5 V should be generated in the internal. Any kinds of surge to be applied to the ECU connector should not be applied.

Note 4) The VF value assumes the voltage which occurs by the current flows to a body diode of DMOS output with a regeneration.

Note 5) The voltage difference between PGND and VBAT should be less than maximum 40V.
Note 6) The voltage difference between AGND and VCC should be less than maximum 6V.
Note 7) PCB size: 114.3 mm x 76.2 mm x 1.6 mm
Multi layer Cu 4 layers, Cu layer area: 74 × 74mm^2

8.1. Heat resistance characteristics

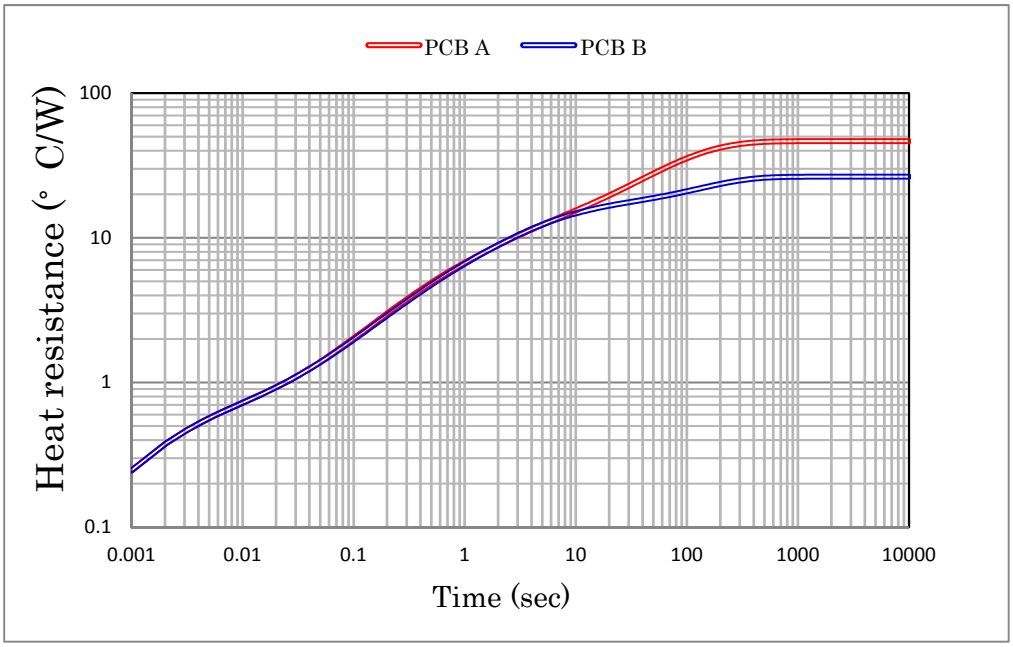
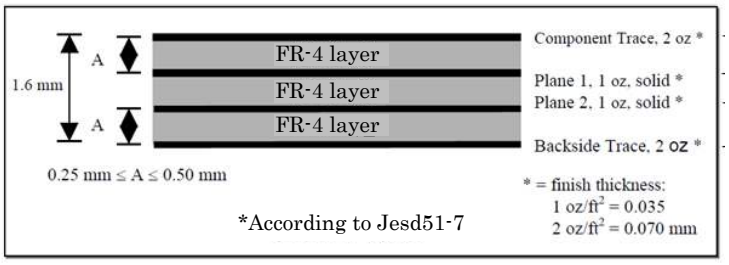


Figure 8.1 Heat resistance characteristics

◆PCB A: θja=46.6°C/W, θjc=1°C/W(Junction – E-Pad)
PCB size: 110 mm x 80 mm x 1.6 mm
Number of layers: Single Layer (Cu 1 layer)
Layer thickness of Cu: 70μm
Layer area of Cu: 600mm²

◆PCB B: θja=26.4°C/W, θjc=1°C/W(Junction – E-Pad)
PCB size: 114.3 mm x 76.2 mm x 1.6 mm (JDEC: Jesd51-7)
Number of layers: Multi Layer (Cu 4 layers)
Layer thickness of Cu: 35μm (1/4 layers), 70 μm (2/3 layers)
Layer area of Cu: 74 x 74 mm²



Condition: Power consumption 1W
Ambient (environment) temperature 25°C
Windless

9. Operating range

9.1. Power supply

This IC is supplied two power supply voltages (VBAT and VCC) from the outside of IC.

(1) VBAT power supply
Connect to a battery power supply as the power supply for a motor drive output.
The VBAT undervoltage detection function is also built in.

(2) VCC power supply
The VCC is used as a power supply for digital I/O of the internal IC, and should be supplied 5V from external.
The VCC is used as the power supply of internal analog system and each kind of monitoring circuit.
The VCC undervoltage detection and VCC high voltage detection functions are also built in as the monitoring function.

Table 9.1 Operating range

Parameter	Symbol	Rating	Unit	Note
Power supply voltage	VBAT	4.5 to 28.0	V	The motor function can operate until VBAT undervoltage detection or VCC undervoltage detection.
	VCC	4.5 to 5.5		
Operating temperature	Topr	-40 to 125	°C	-

Table 9.2 Slew rate of power supply

Test condition unless otherwise specified, VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, Ta = -40 to 125°C

Parameter	Symbol	Pin name	Test condition	MIN	TYP.	MAX	Unit
Slew rate of power supply	VBSLEW	VBAT, VCC	-	-2	-	2	V/μs

10. Electrical characteristics

10.1. Input circuit

Table 10.1 Electrical characteristics of input circuit

Test condition unless otherwise specified, VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, Ta = -40 to 125°C

Parameter	Symbol	Pin name	Test condition	MIN	TYP.	MAX	Unit
Input voltage	VIH	PWM1/PWM2/ EN /ENB/OCC	-	1.75	-	VCC	V
	VIL		-	-0.3	-	0.75	V
	Vhys		-	0.1	0.35	1.0	V
Input current	IIH1	OCC/PWM1/ PWM2 /EN	VIN = VCC = 5 V	25	50	100	μA
	IIH2	ENB		-5	0	5	μA
	IIL1	ENB	VIN = GND	-88	-42	-20	μA
	IIL2	OCC/PWM1/ PWM2 /EN		-5	0	5	μA
PWM input maximum frequency (Note 1)	PWMMAX	PWM1/PWM2	-	-	-	20	kHz
EN/ENB logic definite time	TEN_ENB	EN, ENB	Logic definite time at thte time of changing EN and ENB pin logic	-	-	5.0	μs
Consumption current	ICC	VCC	VCC = 5 V, Figure 11.1	-	2.9	5.0	mA
	IBAT	VBAT	VBAT = 14 V, Figure 11.1	-	1.0	2.0	mA

(Note 1) For the width of the PWM1/PWM2, use so that both of upper and lower are more than 10 μs (min) width.

- PWM1 and PWM2 pins build in a pull-down resistance.
- The EN pin builds in a pull-down resistance. The ENB pin builds in a pull-up resistance.
- The OCC pin builds in a pull-down resistance.

10.2. Power supply monitoring function

Table 10.2 Electrical characteristics of power supply monitoring function

Test condition unless otherwise specified, VBAT = 4.5 to 28 V,VCC = 4.5 to 5.5 V, Ta = -40 to 125°C

Parameter	Symbol	Pin name	Test condition	MIN	TYP.	MAX	Unit
VBAT undervoltage detection voltage	VBATRSTL	VBAT	Figure 7.6.1-1	3.5	3.75	4.0	V
VBAT undervoltage release voltage	VBATRSTH	VBAT	Figure 7.6.1-1	4.0	4.25	4.5	V
Hysteresis width of VBAT undervoltage detection	VBATRSTHY	VBAT	Figure 7.6.1-1	0.1	0.50	1	V
VBAT undervoltage detection filter	TVBAT_uv	VBAT	Figure 7.6.1-2	1.0	2.0	3.5	μs
VCC undervoltage detection voltage	VCCHL	VCC	Figure 7.6.2-1	3.3	3.5	3.7	V
Hysteresis width of VCC undervoltage detection	VCCHLHYS	VCC	Figure 7.6.2-1	0.1	0.20	0.3	V
VCC undervoltage detection filter	TVCC_uv	VCC	Figure 7.6.2-2	1.56	2.5	4.2	ms
VCC undervoltage detection filter (at release)	TVCC_uv2	VCC	Figure 7.6.2-2	0	100	167	μs
VCC undervoltage POR detection voltage	VCCRHL	VCC	Figure 7.6.2-1	2.85	3.07	3.25	V
Hysteresis width of VCC undervoltage POR detection	VCCRHLHYS	VCC	Figure 7.6.2-1	0.1	0.20	0.3	V
VCC undervoltage POR detection filter	TVCC_por	VCC	Figure 7.6.2-3	5.0	13.0	20.0	μs
VCC high voltage detection voltage	VCCHLH	VCC	Figure 7.6.3-1	5.57	5.80	5.97	V
Hysteresis width of VCC high voltage detection	VCCHHLHYS	VCC	Figure 7.6.3-1	10	30	70	mV
VCC high voltage detection filter	TVCC_up	VCC	Figure 7.6.3-2	1.56	2.5	4.2	ms
VCC high voltage detection filter (at released)	TVCC_up2	VCC	Figure 7.6.3-2	0	100	167	μs

10.3. Motor drive output circuit

Table 10.3 Electrical characteristics of motor drive output circuit

Test condition unless otherwise specified, VBAT = 4.5 to 28 V,VCC = 4.5 to 5.5 V,Ta = -40 to 125°C

Parameter	Symbol	Pin name	Test condition	MIN	TYP.	MAX	Unit
H-Bridge Output ON resistance (High Side +Low Side)	Ron (H+L)	OUT1, OUT2	Tj = +25°C Iout = 3 A, VBAT = 8 V	-	-	340	mΩ
			Tj = +150°C Iout = 3 A, VBAT = 8 V	-	-	450	
			Tj = +150°C Iout = 3 A, VBAT = 4.5 V	-	-	510	
Output leakage current	Ioutleak	OUT1, OUT2	OUT1/2: OFF (High-Z) Vout = VBAT = 28 V	-	0	100	μA
			OUT1/2: OFF (High-Z) Vout = GND	-100	0	-	
Output Slew Rate	trD/tfD	OUT1, OUT2	VBAT = 14 V, Figure 10.9-1	0.3	0.8	1.6	μs
Delay time of driver output	tD(on)	PWM1, PWM2 OUT1, OUT2	RL = 3 Ω, VBAT = 14 V Figure 10.9-2	-	8.0	13	μs
	tD(off)			-	8.0	13	μs
	ΔtD		tD(on)-tD(off)	-	0	5	μs
Delay time of Enable/Disable	tDEN	EN, ENB OUT1, OUT2	Figure 10.9-3, Test circuit is shown in Figure 11.2.	-	-	5	μs

10.4. Current limitation control

Table 10.4 Electrical characteristics of current limitation control

Test condition unless otherwise specified, VBAT = 4.5 to 28 V,VCC = 4.5 to 5.5 V, Ta = -40 to 125°C

Parameter	Symbol	Pin name	Test condition	MIN	TYP.	MAX	Unit
H-side of current limitation threshold	Ilim-H	OUT1, OUT2	-	5.0	6.5	8.2	A
H-side filter *	Tlimh	OUT1, OUT2	-	0.1	1.0	2.0	μs
Detection filter time	tBLANK1	OUT1, OUT2	-	7.5	11.5	17.5	μs
Current Limitation time	Toff_min	OUT1, OUT2	-	15	20.5	32	μs
L-side of current limitation threshold	Ilim-L	OUT1, OUT2	-	-	Ilim-H -0.25	-	A
L-side filter (Note 1)	Tliml	OUT1, OUT2	-	0.8	2.0	3.5	μs

(Note 1): The filter is built in.

Table 10.5 Electrical characteristics of current limitation control (when current limitation temperature is detected)

Test condition unless otherwise specified, VBAT = 4.5 to 28 V,VCC = 4.5 to 5.5 V, Ta = -40 to 125°C

Parameter	Symbol	Pin name	Test condition	MIN	TYP.	MAX	Unit
H-side of current limitation threshold	Ilim-H	OUT1, OUT2	-	1.8	2.5	3.5	A
Current limitation temperature (Note 1)	Twar	-	-	150	160	170	°C
Detection filter of current limitation temperature	Twarfil	-	-	2.66	4.0	6.67	μs

(Note 1): This cahacteristic is disign value. It is impossible to test under mass production.

10.5. Over-temperature detection circuit

Table 10.6 Electrical characteristics of over-temperature detection circuit

Test condition unless otherwise specified, VBAT=4.5 to 28V, VCC=4.5 to 5.5V,Ta=-40 to 125°C

Parameter	Symbol	Pin name	Test condition	MIN	TYP.	MAX	Unit
Shutdown temperature of over-temperature detection (Note 1)	TSD	-	-	175	-	200	°C
Hysteresis temperature of over-temperature detection (Note 1)	TSDhys	-	-	-	30	-	°C
Over-temperature detection filter	TTSD	-	-	5.0	8.0	16.0	μs

(Note 1): This cahacteristic is disign value. It is impossible to test under mass production.

10.6. Over-current detection circuit at the time of short to power supply, short to GND, and load short

Table 10.7 Electrical characteristics of over-current detection circuit at the time of short to power supply, short to GND, and load short

Test condition unless otherwise specified, VBAT = 4.5 to 28 V,VCC = 4.5 to 5.5 V, Ta = -40 to 125°C

Parameter	Symbol	Pin name	Test condition	MIN	TYP.	MAX	Unit
Over current circuit threshold	Iovc	OUT1, OUT2	-	8.5	11.0	14.0	A
OFF time	TOFF	OUT1, OUT2	OCC: H, Figure 7.8-1	330	500	860	ms

10.7. DIAG output

Table 10.8 Electrical characteristics of DIAG output

Test condition unless otherwise specified, VBAT=4.5 to 28V, VCC=4.5 to 5.5V,Ta=-40 to 125°C

Parameter	Symbol	Pin name	Test condition	MIN	TYP.	MAX	Unit
Leakage current of DIAG output	Idiag(leak)	DIAG	Vdiag = 5V	-	0	5.0	μA
L-level output voltage	Vdiag	DIAG	RL = 5.1 kΩ	-	0.02	0.4	V
Response time	Tpddiag	DIAG	-	-	-	8.0	μs

10.8. High-side current monitoring

Table 10.9 Electrical characteristics of output (High-side) current monitoring

Test condition unless otherwise specified, VBAT = 4.5 to 28 V,VCC = 4.5 to 5.5 V, Ta = -40 to 125°C

Parameter	Symbol	Pin name	Test condition	MIN	TYP.	MAX	Unit
OCM output current 1	VOCM	OCM	R = 220 Ω, Iout = 0 mA	-	-	500	μA
OCM output current 2			R = 220 Ω, Iout = 300 mA	250	720	1300	μA
OCM output current 3			R = 220 Ω, Iout = 500 mA	0.60	1.20	1.90	mA
OCM output current 4			R = 220 Ω, Iout = 1.5 A	2.68	3.35	4.02	mA
OCM output current 5			R = 220 Ω, Iout = 3.0 A	5.36	6.70	8.04	mA
OCM output current 6			R = 220 Ω, Iout = 6.0 A	10.70	13.38	16.06	mA
Dynamic range	DROCM	OCM	-	0	-	4	V

Note) The voltage (min) of VCC is using 4.5 V. Even if it attaches higher resistance than 220Ω for an external resistor,please keep in mind that voltage is reaching the ceiling in use.

10.9. AC characteristics of driver output

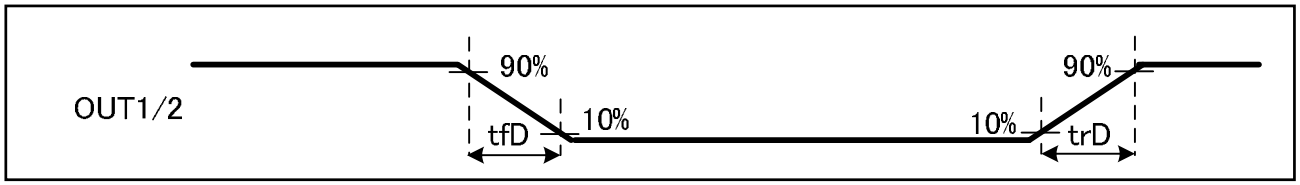


Figure 10.9-1 Slew rate of driver output (SR)

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

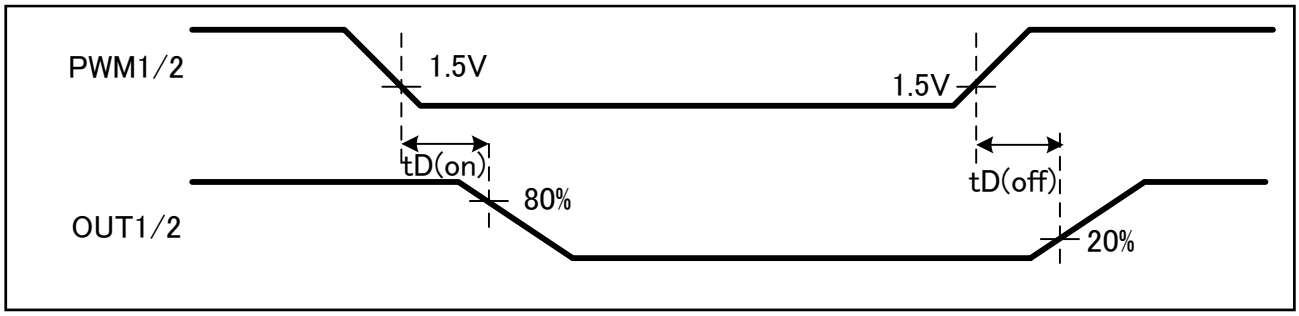


Figure 10.9-2 Driver output delay

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

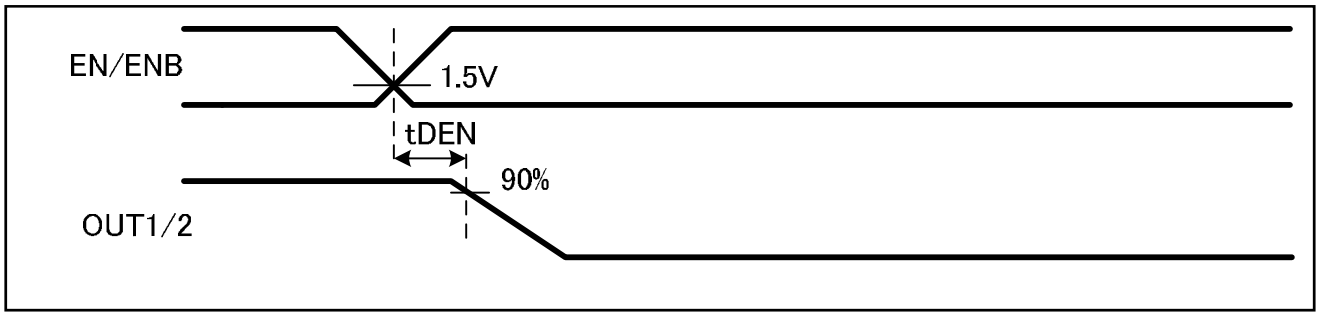


Figure 10.9-3 Driver output Enable delay

Note: Some of timing charts in this document may be omitted or simplified for explanatory purposes.

11. Test circuit

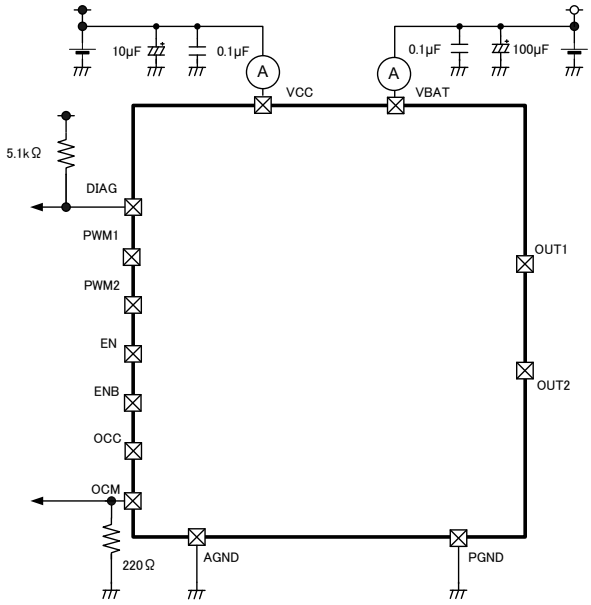


Figure 11.1 Test circuit diagram of current consumption

Note: Components in the test circuits are only used to obtain and confirm the device characteristics. These components and circuits do not warrant preventing the application from malfunction from malfunction or failure.

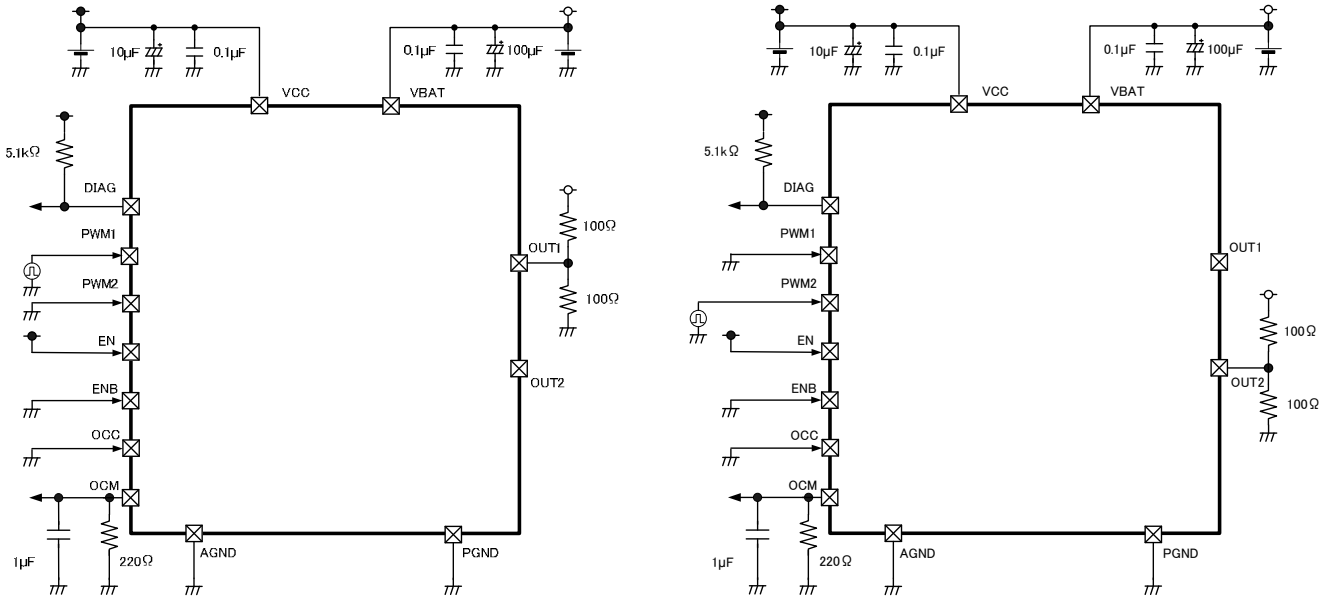
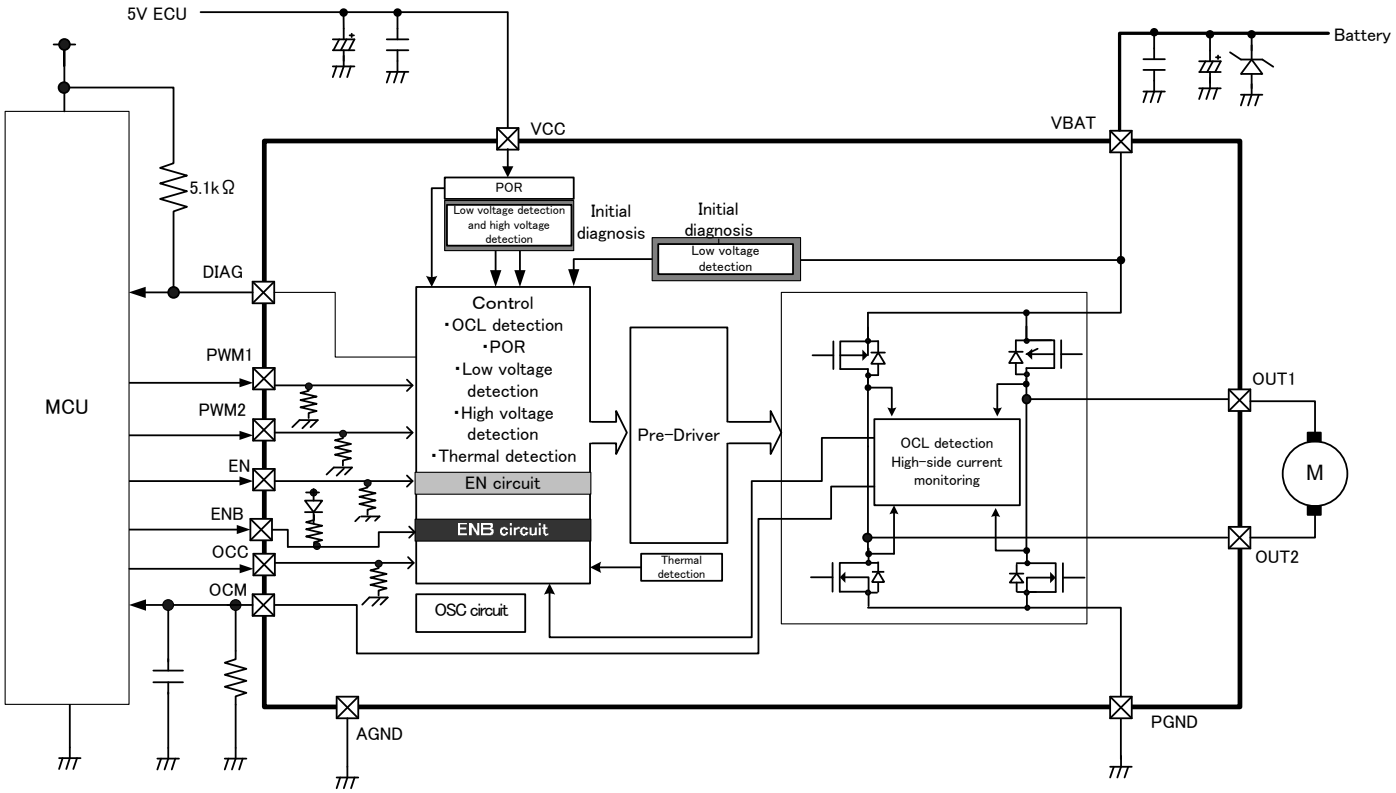


Figure 11.2 tDEN test circuit

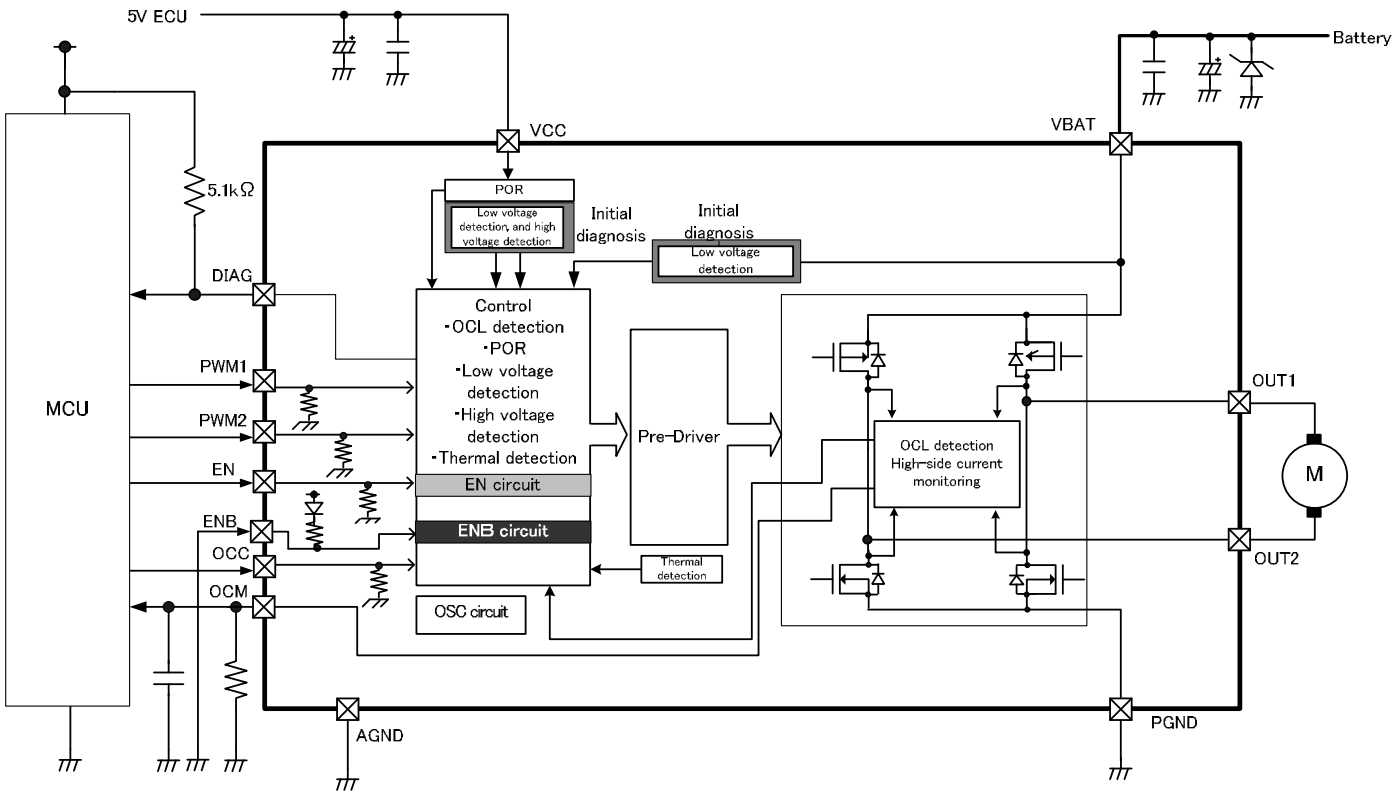
Note: Components in the test circuits are only used to obtain and confirm the device characteristics. These components and circuits do not warrant preventing the application from malfunction from malfunction or failure.

12. Examples of application circuit



*Application circuit using both EN pin and ENB pin

Table 12.1 Example of application circuit 1



* This figure shows an example of application circuit controlled by only EN pin. EN pin is fixed to H and this circuit can be controlled by ENB.

Table 12.2 Example of application circuit 2

Note 1: Some of the functional blocks, circuits in the block diagram may be omitted or simplified for explanatory purposes.
Note 2: Do not insert devices in the wrong orientation or incorrectly. Otherwise, it may cause device breakdown, damage and/or deterioration.
Note 3: The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage. Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.
Note 4: Careful attention should be paid to the layout of the output line, VBAT, VCC and GND line since IC may be destroyed due to short-circuit between outputs, to the power supply, or to the ground.
Note 5: For the board design, it is necessary to consider the solid pattern of AGND and PGND.

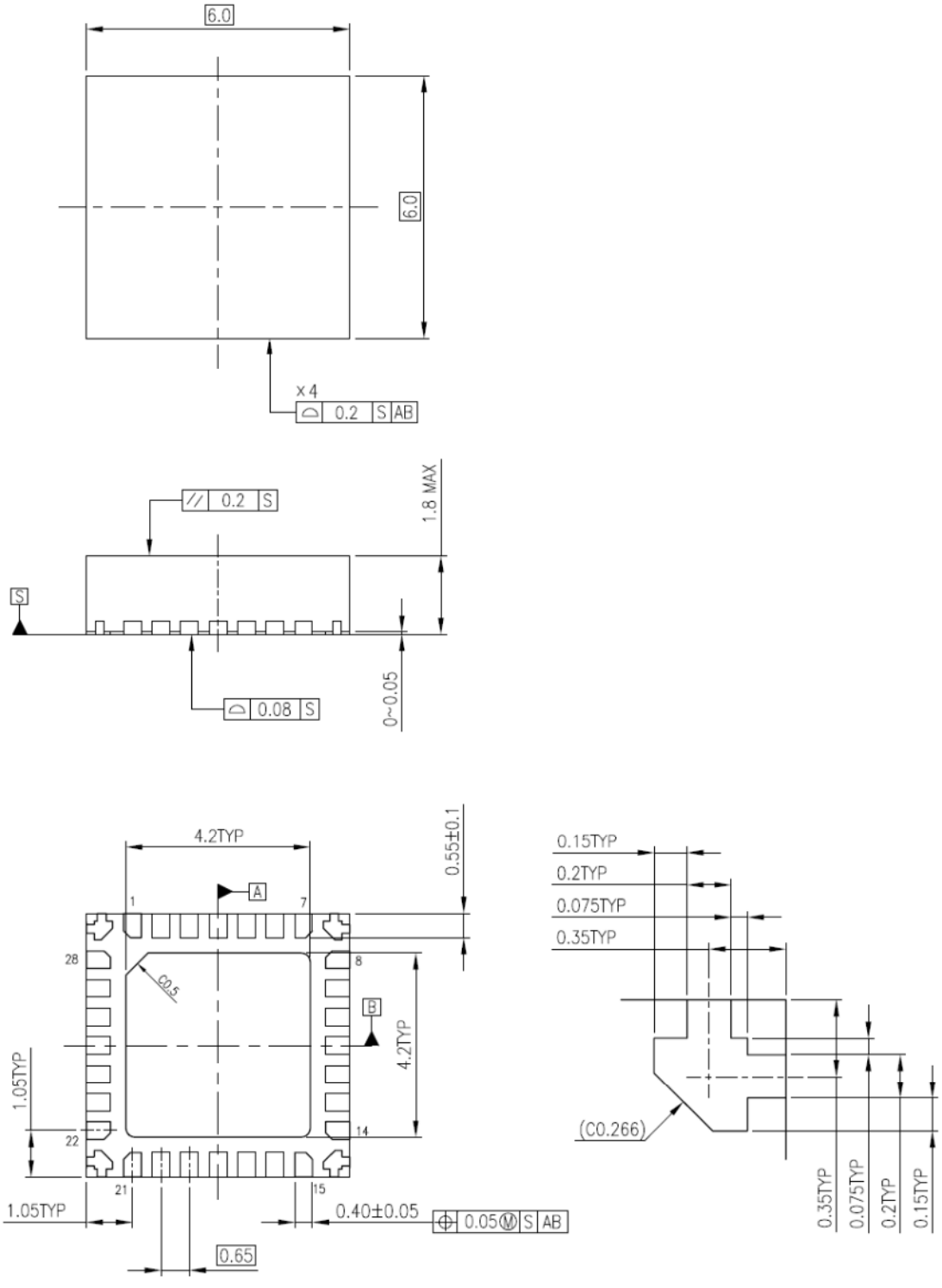
Back-EMF
While a motor is rotating, there is a timing at which power is fed back to the power supply. At that timing, the motor current is fed back to the power supply owing to the effect of the motor back-EMF. If the power supply does not have enough sink capability, the power supply and output pins of the device might rise above the rated voltages. The magnitude of the motor back-EMF varies with usage conditions and motor characteristics. It must be fully verified that there is no risk that this product or other components will be damaged or fail owing to the motor back-EMF.

13. Package

13.1. Package dimensions

Package dimensions

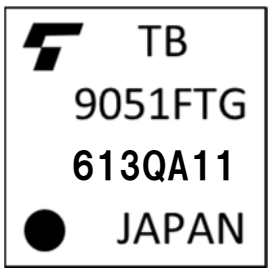
P-QFN28-0606-0.65-001 "Unit:mm"



Weight: 0.22g (Typ.)

Table 13.1 Package dimensions

13.2. Mark Design



1. Toshiba logo mark
2. Product name (Part number: TB9051FTG)
3. Lot code (e.g.613QA11)
4. Country/Region of origin (JAPAN)

* Lot code description
Example. : 6 (1) 13 (2) Q (3) A11 (4)

(1) Last number of calendar year (Example shows “6” of 2016)
(2) Week code (Example shows 13th week)
(3) Product sight code (Q)
(4) Toshiba management code (3 digits at maximum)

14. IC Usage Considerations

14.1. Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over-current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as Fast-blow fuse capacity, fusing time and insertion circuit location, are required.

14.2. Points of Remember on Handling of ICs

(1) Over-current Protection Circuit
Over-current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over-current protection circuits operate against the over-current, clear the over-current status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over-current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over-current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

Notes on Handling of ICs

(1) Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

(2) Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

(3) Timing Charts

Timing charts may be simplified for explanatory purposes.

(4) Absolute Maximum

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment.

(5) Do not insert devices in the wrong orientation or incorrectly.

Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

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