

Migrating from MX30LF2G(4G)28AB to MX30LF2G(4G)18AC

1. Introduction

This application note is a migration guide for migrating Macronix MX30LF2G(4G)28AB to MX30LF2G(4G)18AC

2Gb(4Gb) SLC NAND Flash. The document does not provide detailed information on the individual devices, but highlights the major similarities and differences between them. The comparison covers the general features, performance, command codes and other differences.

The information in this document is based on datasheets listed in Section 8. Newer versions of the datasheets may override the contents of this document.

2. General Features

Both flash device families have similar features and functions as shown in **Table 2-1**. Feature differences are highlighted in **Bold Italic** type in the table.

Part Name	MX30LF2G(4G)28AB	MX30LF2G(4G)18AC
Voltage	2.7V-3.6V	2.7V-3.6V
Bus Width	x8	x8
Operating Temperature	-40°C to 85°C	-40°C to 85°C
Interface	ONFI 1.0 Compliant	ONFI 1.0 Compliant
Page Size	(2K+112)B	(2K+ 64)B
Block Size	(128K+7K)B	(128К+ 4К)В
ECC Requirement	8bit/540B	4bit/528B
OTP	30 Pages	30 Pages
Unique ID	ONFI Standard	ONFI Standard
Block Protection	N/A	Yes
Guaranteed Good Blocks at shipping	Block#0	Block#0
Data Retention	10 Years	10 Years
Endurance	100K Cycles	100K Cycles
Package	48TSOP (12x20mm) 63-VFBGA (9x11mm)	48TSOP (12x20mm) 63-VFBGA (9x11mm)

Table 2-1. Key Features Comparison



3. Electrical Performance

Both flash device families have similar performance as shown in **Table 3-1**. Performance differences are highlighted in *Bold Italic* type in the table.

Part Name		MX30LF2G(4G)28AB		MX30LF2G(4G)18AC			
Performance		Min.	Тур.	Max.	Min.	Тур.	Max.
	Random (tR)	-	-	25us	-	-	25us
Access Time	Cache Read Busy time	-	2us	25us	-	3.5us	25us
	Sequential	20ns	-	-	20ns	-	-
	Page Program	-	300us	600us	-	300us	600us
Program Time	Cache Program Busy time	-	3us	600us	-	5us	600us
Erase Time	Block	-	1ms	3.5ms	-	1ms	3.5ms
	Standby (TTL)	-	-	1mA	-	-	1mA
	Standby (CMOS)	-	10uA	50uA	-	10uA	50uA
	Active Read	-	20mA	30mA	-	20mA	30mA
	Active Program	-	20mA	30mA	-	20mA	30mA
Current Consumption	Active Erase	-	15mA	30mA	-	15mA	30mA
	Power-up Current (Including POR Current)	-	-	30mA	-	-	50mA
	Input Leakage	-	-	+/- 10uA	-	-	+/- 10uA
	Output Leakage	-	-	+/- 10uA	-	-	+/- 10uA
Partial-Page Programs	NOP	-	-	4 cycles	-	-	4 cycles

Table 3-1. Key Performance Comparison



4. Command Set

Command sets are the same with the addition of the "Block Protection Status Read" command which is highlighted in *Bold Italic type* in Table 4-1.

Part Name	MX30LF2G(4G)28AB		MX30LF2G(4G)18AC		
Command Description	1st cmd Cycle	2nd cmd Cycle	1st cmd Cycle	2nd cmd Cycle	
Read	00h	30h	00h	30h	
Random Data Input	85h	-	85h	-	
Random Read Data Output	05h	E0h	05h	E0h	
Cache Read Random	00h	31h	00h	31h	
Cache Read Sequential	31h	-	31h	-	
Cache Read End	3Fh	-	3Fh	-	
Read ID	90h	-	90h	-	
Parameter Page Read (ONFI)	ECh	-	ECh	-	
Read Unique ID (ONFI)	EDh	-	EDh	-	
Get Features (ONFI)	EEh	-	EEh	-	
Set Features (ONFI)	EFh	-	EFh	-	
Reset	FFh	-	FFh	-	
Page Program	80h	10h	80h	10h	
Cache Program	80h	15h	80h	15h	
Block Erase	60h	D0h	60h	D0h	
Status Read	70h	-	70h	-	
Status Enhanced Read (ONFI)	78h	-	78h	-	
Block Protection Status Read	-	-	7Ah	-	
Two-plane Program (ONFI)	80h-11h-80h-10h		80h-11h-80h-10h		
Two-plane Cache Program (ONFI)	80h-11h-80h-15h		80h-11h-80h-15h		
Two-plane Block Erase (ONFI)	60h-D1h-60h-D0h		60h-D1h-60h-D0h		
OTP Area Access	Set Feature followed by normal read/program command		Set Feature followed by normal read/program command		

Table 4-1. Command Set



5. Status Register Comparison

Status Register bit functions are the same (**Table 5-1**). Please refer to the Macronix datasheet for additional details.

Part Name	MX30LF2G(4G)28AB	MX30LF2G(4G)18AC	
SR[0]	Program/Erase Pass or Fail	Program/Erase Pass or Fail	
SR[1]	Cache Program Pass or Fail	Cache Program Pass or Fail	
SR[2]	Not Used	Not Used	
SR[3]	Not Used	Not Used	
SR[4]	Not Used	Not Used	
SD[5]	Ready/Busy for Internal Controller	Ready/Busy for Internal Controller	
SR[5]	Program/Erase/Read Operation	Program/Erase/Read Operation	
SR[6]	Ready/Busy	Ready/Busy	
SR[7]	Write Protect	Write Protect	

Table 5-1. Status Register Comparison

6. Package Pin Definition

The MX30LF2G(4G)28AB can be replaced by the MX30LF2G(4G)18AC without pin conflicts. Because the only difference is the PT (Protection) pin #38 of the MX30LF2G(4G)18AC. 48-TSOP (or ball G5 of the 63-VFBGA) (which has an internal weak pull-down) the user does not need to do anything if the protection feature is not used.

Package physical dimensions are the same. For detailed information, please refer to the individual datasheets.

Table 6-1. Package Pin Definition

Part Name	MX30LF2G(4G)28AB	MX30LF2G(4G)18AC
48-TSOP pin 38 63-VFBGA ball G5	DNU	PT (Protection)



7. Device Identification

The ID codes of the MX30LF2G(4G)28AB and MX30LF2G(4G)18AC are identical except for the last byte which is used to indicate the ECC requirement.

Please note that although the two devices share the same code of "1" for the Spare Area Size (4th Byte, Bit 2), the MX30LFxG28AB's Spare Area Size is 28 Bytes per 512 bytes, whereas the MX30LFxG18AC's Spare Area size is 16 bytes per 512 bytes. Firmware that uses a non-ONFI detection method may need to be modified to recognize the smaller spare area of the MX30LFxG18AC device.

Part Name		MX30LFxG28AB	MX30LFxG18AC	
ID Code	2Gb	C2h/DAh/90h/95h/07h	C2h/DAh/90h/95h/06h	
4Gb		C2h/DCh/90h/95h/57h	C2h/DCh/90h/95h/5 6h	
1st Byte		Manufacturer ID	Manufacturer ID	
	2nd Byte	Device ID	Device ID	
		Number of Die per CE	Number of Die per CE	
		Cell Structure	Cell Structure	
		Number of Concurrently Programmed	Number of Concurrently Programmed	
	3rd Byte	Pages	Pages	
		Interleaved Programming between	Interleaved Programming between	
		multiple devices	multiple devices	
		Cache program	Cache program	
ID Definition		Page Size	Page Size	
		Spare Area Size (28-byte per 512-	Spare Area Size (16-byte per 512-	
		byte), bit2=1	byte), bit2=1	
	4th Byte	Sequential Read Cycle Time	Sequential Read Cycle Time	
		(bit7, bit3=1,0)	(bit7, bit3= 1,0)	
		Block Size (Excluding spare area)	Block Size (Excluding spare area)	
		Organization	Organization	
		ECC level requirement, 8-bit ECC	ECC level requirement, 4-bit ECC	
		required (bit1:0=11b)	required (bit1:0=10b)	
	5th Byte	Plane number	Plane number	
		Plane Size (Excluding spare area)	Plane Size (Excluding spare area)	
		Reserved	Reserved	

Table 7-1. Device Identification

8. Reference

Table 8-1 shows the datasheet versions used for comparison in this application note. For the most current, detailed specification, please contact Macronix Sales and distributors.

Table 8-1. Datasheet Versions

Datasheet	Location	Date Issued	Revision
MX30LFxG28AB	Website	Jun. 2014	Rev. 1.1
MX30LFxG18AC	Website	Oct. 2014	Rev. 1.0



9. Summary

The Macronix MX30LFxG28AB and MX30LFxG18AC NAND flash share the same basic Read, Program, and Erase commands and have compatible pin-outs. The newly defined "PT" function on pin-38 of the MX30LFxG18AC can be left floating if the function is not needed or used. Migrating to the MX30LFxG18AC may require firmware modifications to accommodate differences in spare area sizes and ECC requirements

10. Part Number Cross-Reference

Table 10-1. Part Number Cross Reference

Bus Width	Voltage	Density	Package	Part Number	Part Number
		2G	48-TSOP	MX30LF2G28AB-TI	MX30LF2G18AC-TI
	x8 3V		63-VFBGA	MX30LF2G28AB-XKI	MX30LF2G18AC-XKI
xo			48-TSOP	MX30LF4G28AB-TI	MX30LF4G18AC-TI
		4G	63-VFBGA	MX30LF4G28AB-XKI	MX30LF4G18AC-XKI

11. Revision History

Table 11-1. Revision History

Revision No.	Description	Page	Date
REV. 1	Initial Release of Advanced Information Version	ALL	Jun. 20, 2014
REV. 2	Correct the issuing date	6	Jul. 17, 2014
	1. Revised some timing spec to align with production datasheet	2	
REV. 3	2. Defined ID byte#4 of MX30LFxG18AC to align with production datasheet	5	Nov. 25, 2014
	3. Revised the datasheet version of MX30LFxG18AC as Rev 1.0. Also removed title of "Advanced Information"	5	



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