8V19N850

Applicable to part number, 8V19N850DNLGI

Description

This document describes the following topics about the 8V19N850 evaluation board:

- Basic hardware and GUI set-up
- Board power-up instructions
- Instructions to get active output signals using a provided configuration file.
- Hardware modifications require for different conditions

Features

The EVB has SMA connectors to relevant I/O of the device:

- Two differential clock inputs
- Four differential digital outputs
- Five differential RF-PLL outputs
- Five SYSREF outputs (JESD204B/C)
- On-board EEPROM stores startup-configuration data
- Four GPIO controls
- Selectable output buffer voltage
- XO_DPLL and OSCI terminals can use laboratory signal generator or OCXO/TCXO/XO components and board
- Laboratory power supply connectors
- Serial port for configuration and register read out

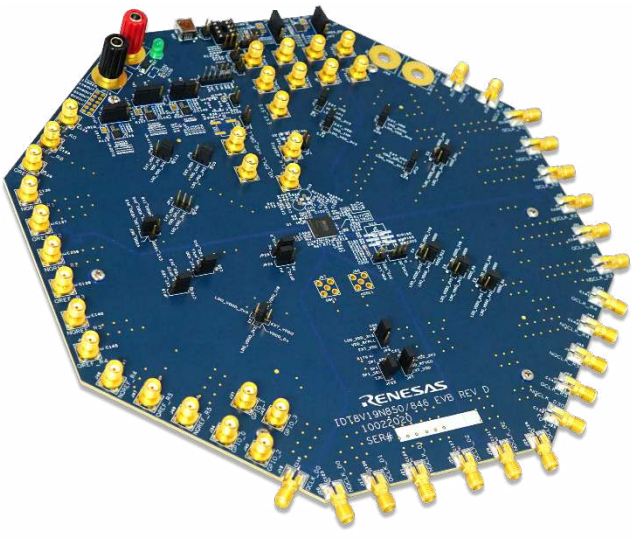
Board Contents

- 8V19N850 evaluation board
- EVB manual
- Configuration software (TCP file for Timing Commander)
- Configuration example file for four built-in device settings
- Board schematic and BOM

Computer Requirements

- Timing Commander Software installed
- 8V19N850 GUI
- USB 2.0 or USB 3.0 Interface
- Windows XP SP3 or later
- Processor: Minimum 1GHz
- Memory: Minimum 512MB; recommended 1GB
- Available disk space:
  - Minimum 600MB (1.5GB 64-bit)
  - Recommended 1GB (2GB 64-bit)
- Network access during installation if the .NET framework is not currently installed on the system

Evaluation Board



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Figures

1. Functional Description

The evaluation kit can be used to evaluate the 8V19N850, a fully integrated radio synchronizer and JESD204B/C clock jitter attenuator. The kit can be used to evaluate major parameters including phase noise, spurious attenuation, clock frequency, output skew, phase alignment, device timing, and the signal waveform. The device on the board accepts any input frequency from 1Hz to 1GHz. Locked to a selected input, the device PLLs generate clock and SYSREF signals for converter reference frequency and data frame synchronization.

The 8V19N850 supports two independent frequency domains: one generates transport network clocks, such as Ethernet frequencies at four outputs and the other one generates radio base station clocks at 12 outputs (ADC/DAC reference clocks and SYSREF signals). Each frequency domain uses a DPLL for frequency translation, clock filtering, and jitter attenuation. The DPLLs provide a programmable bandwidth and a DCO function for real-time frequency/phase adjustment.

1.1 Operational Characteristics

The board is equipped with on-board LDOs that require a 4V supply. The input power voltage should not exceed 5V. The board is designed to operate over the industrial temperature range from -40 to 85°C, ambient temperature.

It is recommended that the person operating the board use proper grounding to avoid ESD damage to the EVB.

1.2 Hardware Setup and Configuration

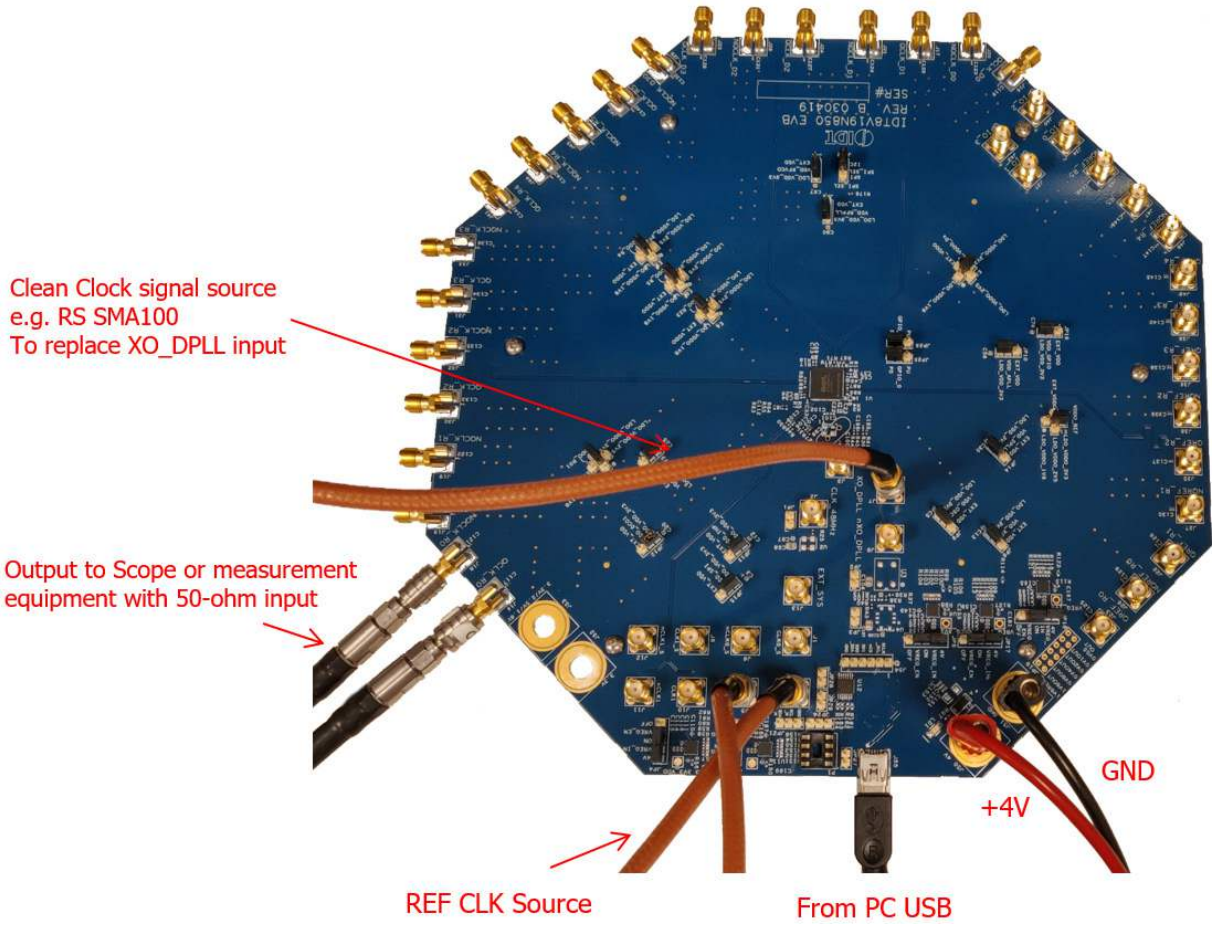


Figure 1. 8V19N850 EVB Hardware Connections

Connect the board as shown in Figure 2. See more details below:

- Power connection:
  - Set the power supply voltage to 4V and the current limit to 2.5A
  - +4V (J50) = +4V
  - GND (J51) = GND
- Expected current draw
  - Rakon TCXO not populated: ~ 1.5A
  - Rakon TCXO populated. Initial current draw will be ~2A and then it will drop down to ~1.7A (Rakon TCXO draws about 250mA after it stabilizes.)
  - After programming the device, depending on the configuration, ~1.1A to 1.7A during normal operation.
- USB/I2C Connection
  - Connect the USB port (J55) to PC through USB Cable
- For proper functionality out of the box, the jumpers on board should be placed to allow the correct voltages at each LDO and domain. The jumpers should be arranged as seen in Table 1.

Table 1. Default Jumper Configuration

Label/Function	Jumper	Default Orientation
XO Enable	JP1	Not populated
OCXO_EN	JP2	Not populated
TCXO_EN	JP3	Not populated
U5 Enable	JP4	4V-to-VREG & VREG_EN-to-ON
U6 Enable	JP5	4V-to-VREG & VREG_EN-to-ON
VDD_RFPLL	JP6	LDO_VDD_3V3
VDDK_RFVCO	JP7	LDO_VDD_3V3
VDD_XO	JP8	LDO_VDD_3V3
VDD_OSC	JP9	LDO_VDD_3V3
VDD_APLL	JP10	LDO_VDD_3V3
VDD_IMP	JP11	LDO_VDD_3V3
VDD_DCO1	JP12	LDO_VDD_3V3
VDD_DPLL1	JP13	LDO_VDD_3V3
VDD_DPLL	JP14	LDO_VDD_3V3
VDD_SPI	JP15	LDO_VDD_3V3
VDD_GPIO	JP16	LDO_VDD_3V3

Label/Function	Jumper	Default Orientation
U7 Enable	JP17	4V-to-VREG & VREG_EN-to-ON
U8 Enable	JP18	4V-to-VREG & VREG_EN-to-ON
U8 LDO Voltage Selection	JP19	Not populated
U11 Enabled	JP20	4V-to-VREG & VREG_EN-to-ON
EEPROM External Connection	JP21	Not populated
SPI_SEL	JP22	I2C
LVL_SHIFT_EN	JP24	Not populated
GPIO_0	JP25	PD
GPIO_1	JP26	PU
EEPROM Power	JP27	Not populated
Connect chip SDA to EEPROM	JP28	Not populated
Connect chip SCLK to EEPROM	JP29	Not populated
VDD_LCF	JP30	Not populated
VCSO_OE	JP31	Not populated
VDDD_REF	E1	LDO_VDDD_3V3
VDDD_Dx	E2	LDO_VDDD_3V3
VDDO_R01	E3	LDO_VDDD_3V3
VDDO_R23	E4	LDO_VDDD_3V3
VDDO_R4	E5	LDO_VDDD_3V3
VDDO_R5	E6	LDO_VDDD_3V3

1.3 GUI Setup and Configuration

1.3.1. Prepare the Software

1. Prior to execution of the GUI, the Timing Commander software must be downloaded and installed.

   If Timing Commander is already installed on the computer, skip this step.
2. Download the 8V19N850D_vx.tcp file from the 8V19N850 webpage.
3. Download and unzip the 8V19N850D_Example_Configuration_files.zip found on the 8V19N850 webpage. These configurations match the four default configuration settings from the internal read-only storage spaces that is specified by the GPIO pins 0, 1.
4. If Timing Commander is not yet installed, please download and install the software from the Timing Commander webpage.

Figure 2. Timing Commander Download

5. Double click on the TimingCommanderSetup.exe file.
6. Follow the on-screen instructions.

1.3.2. Bring Up the GUI

1. After successfully installing the Timing Commander software, activate the software from the Windows <start> menu at the bottom left-corner of the screen.
2. Start > IDT > Timing Commander.

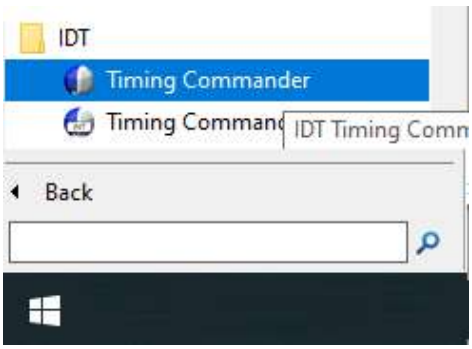


Figure 3. Start Timing Commander

3. Click <Open Setting File>.

Figure 4. Open Settings File

4. Use the file browser button to locate the example tcs file.

Figure 5. Open Browser to Search for .tcs File

5. Pick one of the example .tcs files from the folder and click “Open”.

Figure 6. Browse for .tcs File

6. Use the file browser button to locate the 8V19N850D_V.x.tcp Timing Commander Personality (.tcp) file.

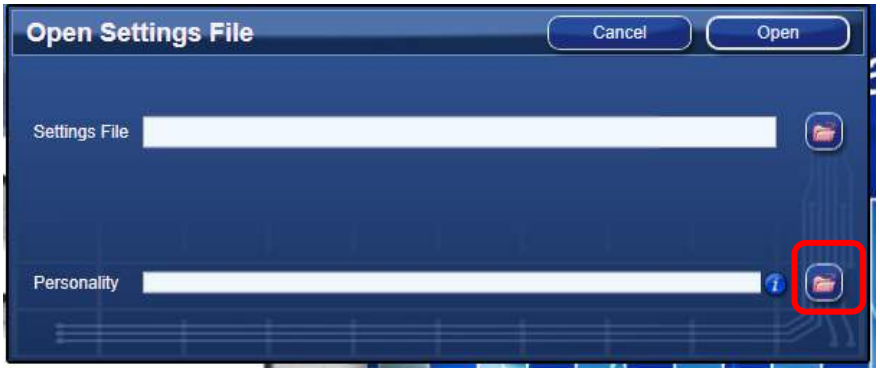


Figure 7. Browse for .tcp File

7. Select the .tcp file and click “Open”.

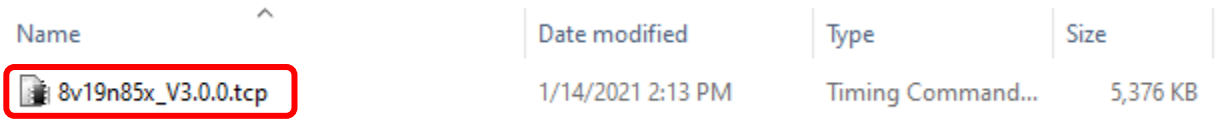


Figure 8. TCP File

8. Once the .tcp and .tcs files have been selected, clock the “Open” button.

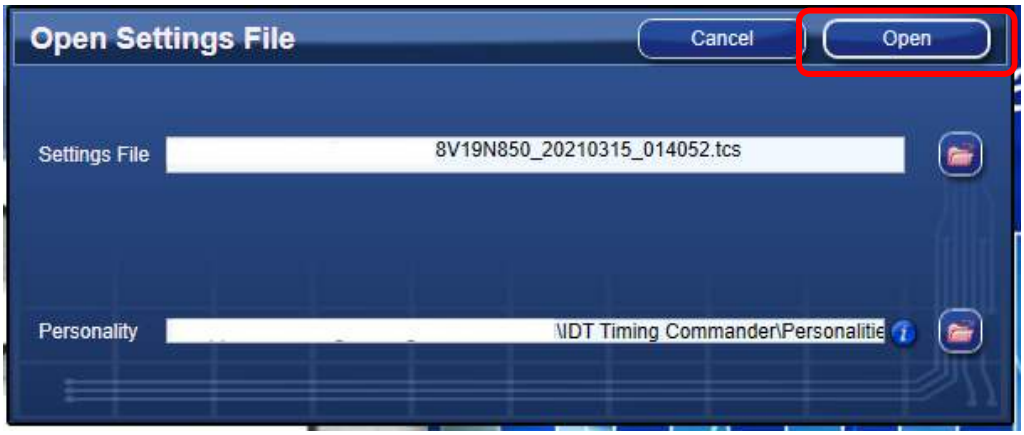


Figure 9. Complete the TCP and TCS File Load

9. The GUI will load the configuration file and the screen will look like the following screen.

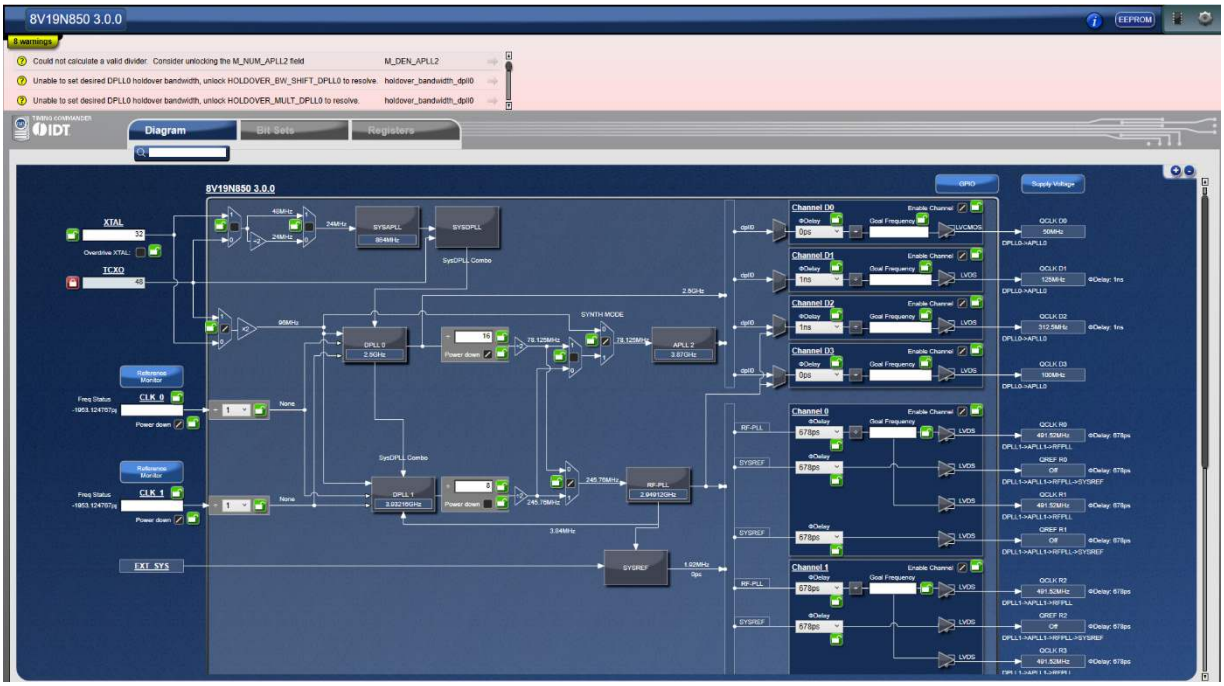


Figure 10. Example Setup View

1.3.3. Configure the Evaluation Board

1. To establish communication between the EVB and the GUI, click the top right-corner chip logo.

Figure 11. Connect to the Board

2. Program the board by pressing the “WriteAll” button. Expect the outputs to activate.

Figure 12. Write All Button

3. After the GUI successfully connects to the device, there will be an Initialization dialog that appears in the diagram.

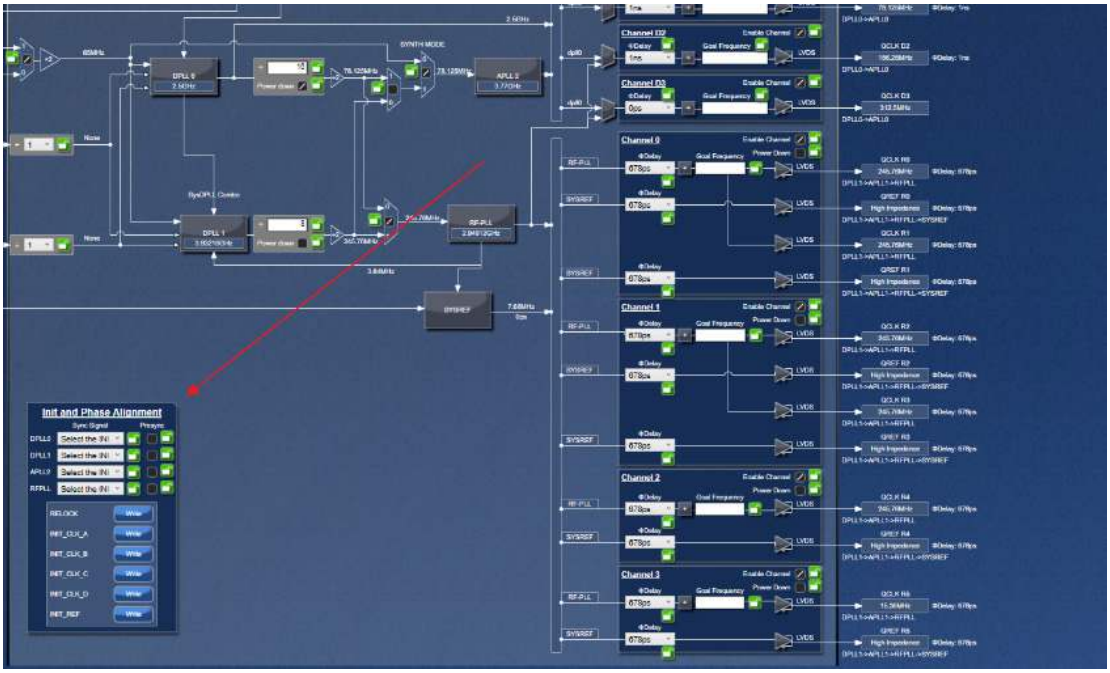


Figure 13. Initialization Dialog

4. Click the “Relock Write” button to see the 8V19N850 PLL lock and align the outputs.

Figure 14. Relock Button

1.4 Hardware Modification Options

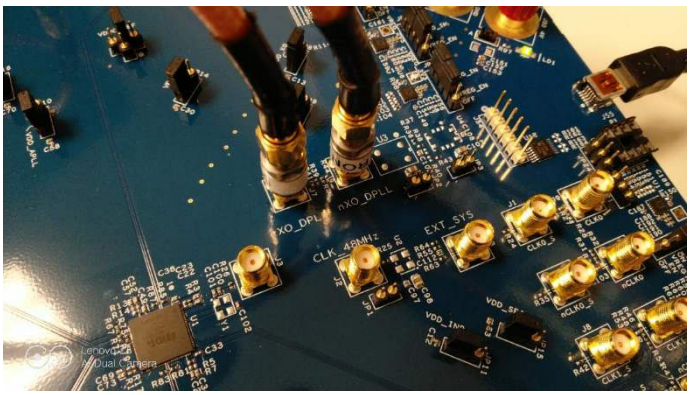
There are three options for providing an input signal to the device XO_DPLL (crystal oscillator input for System Digital PLL) pin:

- An external signal (J7/J9 SMA connectors) typically from a signal generator; see Section 1.4.1). This option is configured by default.
- An on-board OCXO (U3: OCXO, mounted on the board); see Section 1.4.2
- An on-board TCXO (U4: TG7050, footprint for TCXO), see Section 1.4.3.

The following sections describe how to configure the board for each option.

1.4.1. Overdrive the OCXO (TCXO) with an External Signal Source

1. Power off the on-board TCXO by removing the JP2 jumper.
2. Apply a single-ended signal to J7 or a differential signal to J7/J9 from an external signal source (e.g., Lab Low noise Signal Generator, RS SMA100A). See an example cable connection in the following image. The signal must meet these requirements:
   - ~1.6Vpp to ~3Vpp for single-ended input
   - ~800mVpp to ~1.5Vpp for differential
   - Option 1 circuit (default Assembly)



3. Use the default EVB XO schematic configuration, as shown in the following figure.

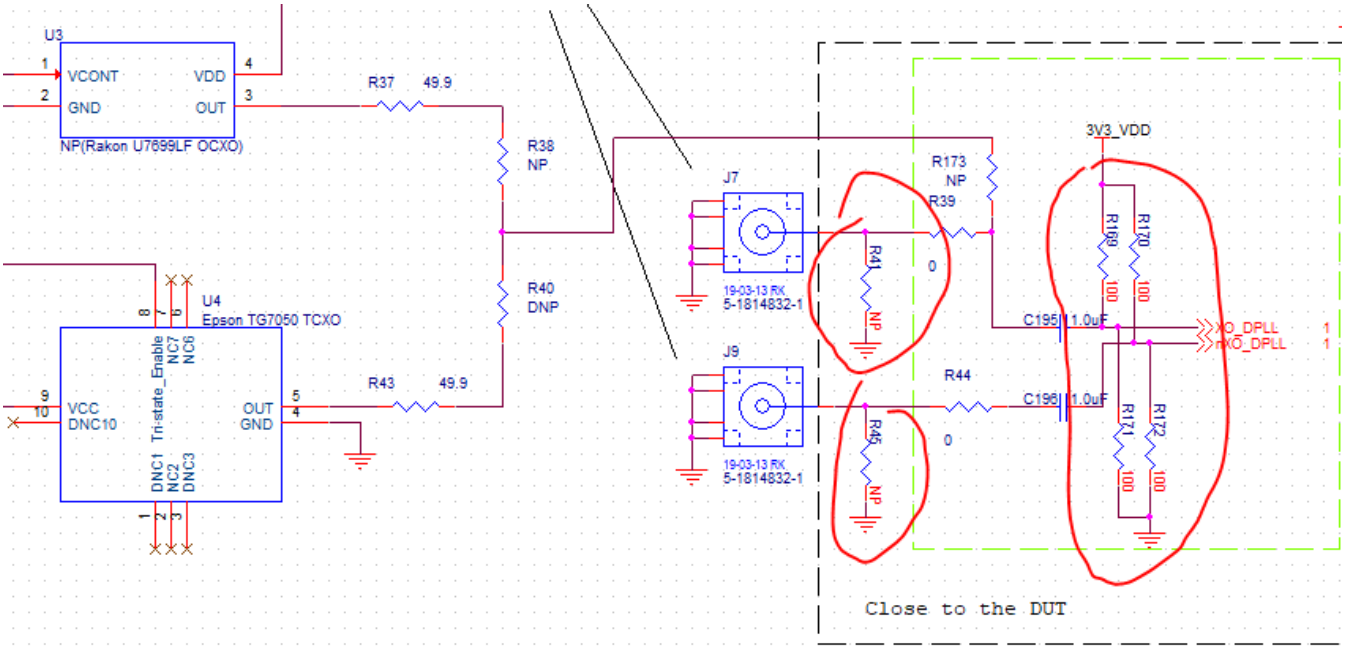


Figure 15. Default XO Input Schematic

1.4.2. Use the Onboard OCXO

1. Install 0Ohm on: R38, R173, and R39.
2. Remove R41.
3. Place a 50 or 100Ohm resistor on R37.
4. Add a 50Ohm termination to J7.

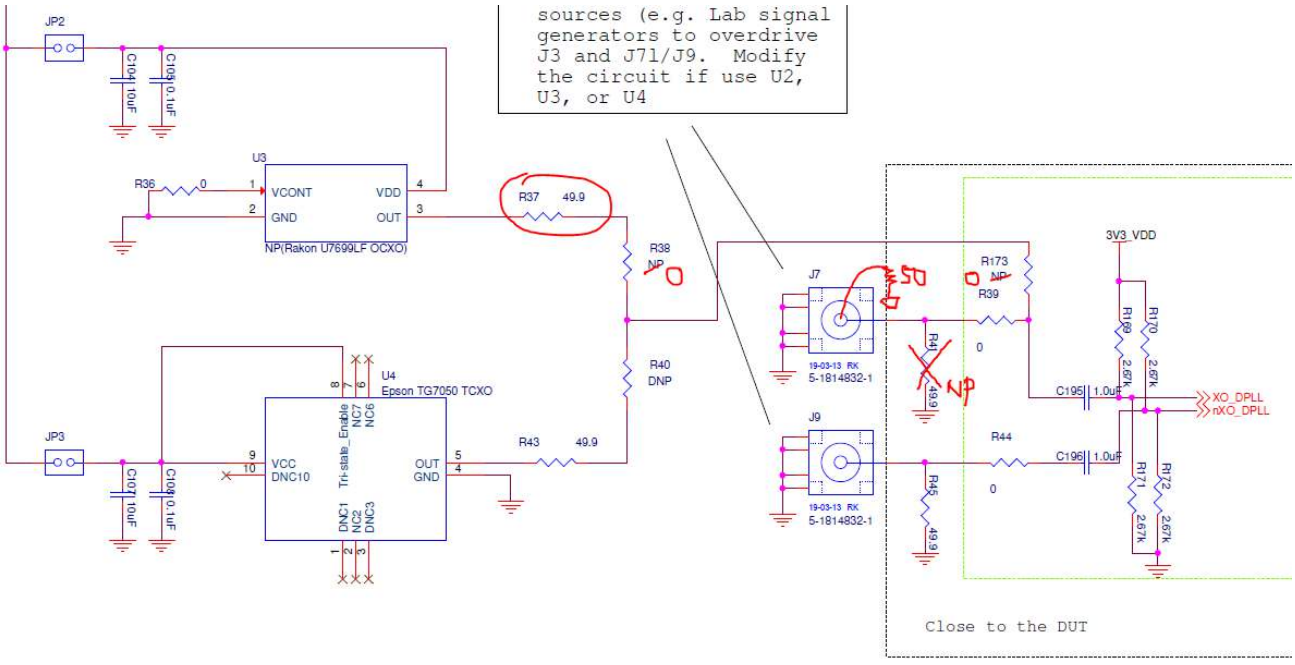


Figure 16. Use On-board OCXO to Drive the XO Input

1.4.3. Use the Onboard TCXO

1. Install a TCXO on U4.
2. Install 0 ohm on: R40, R173, R39
3. Remove R41
4. Place a 50 or 100ohm resistor on R43
5. Add a 50 Ohm termination to J7

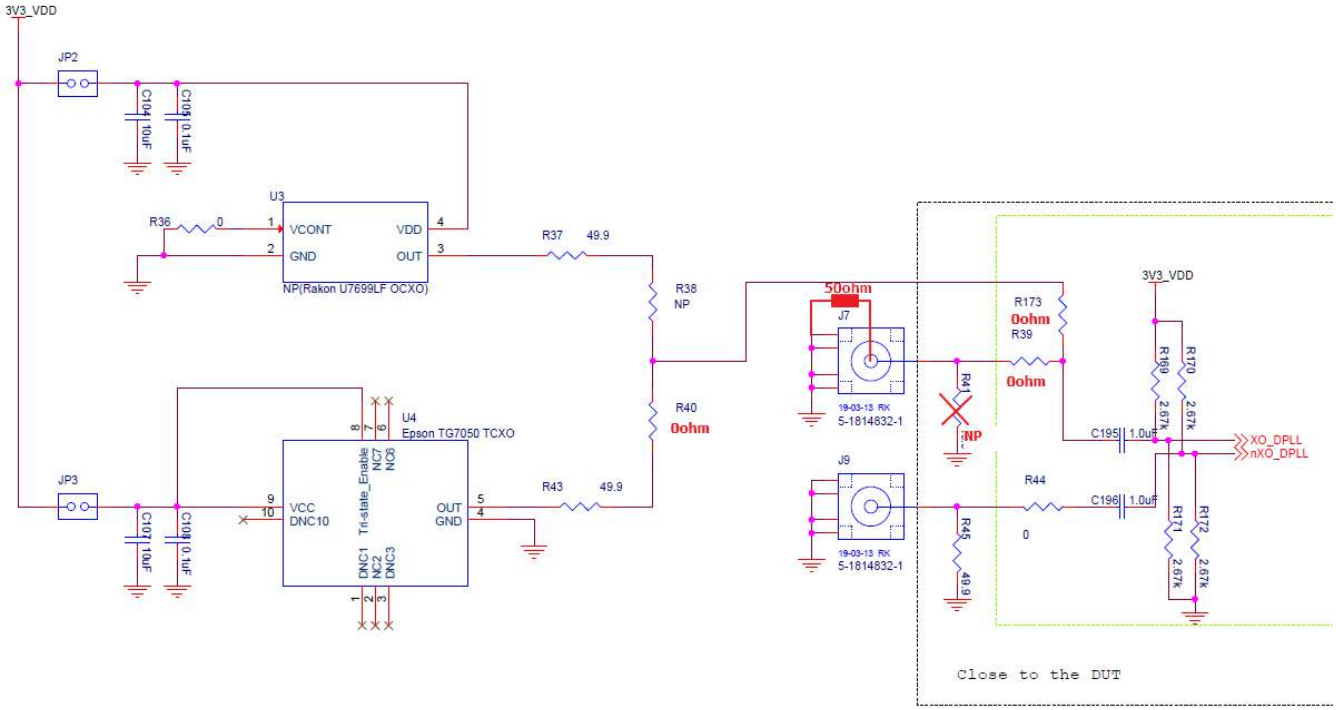


Figure 17. Use On-board TCXO to Drive the XO Input

2. Board Design

2.1 Evaluation Board Images

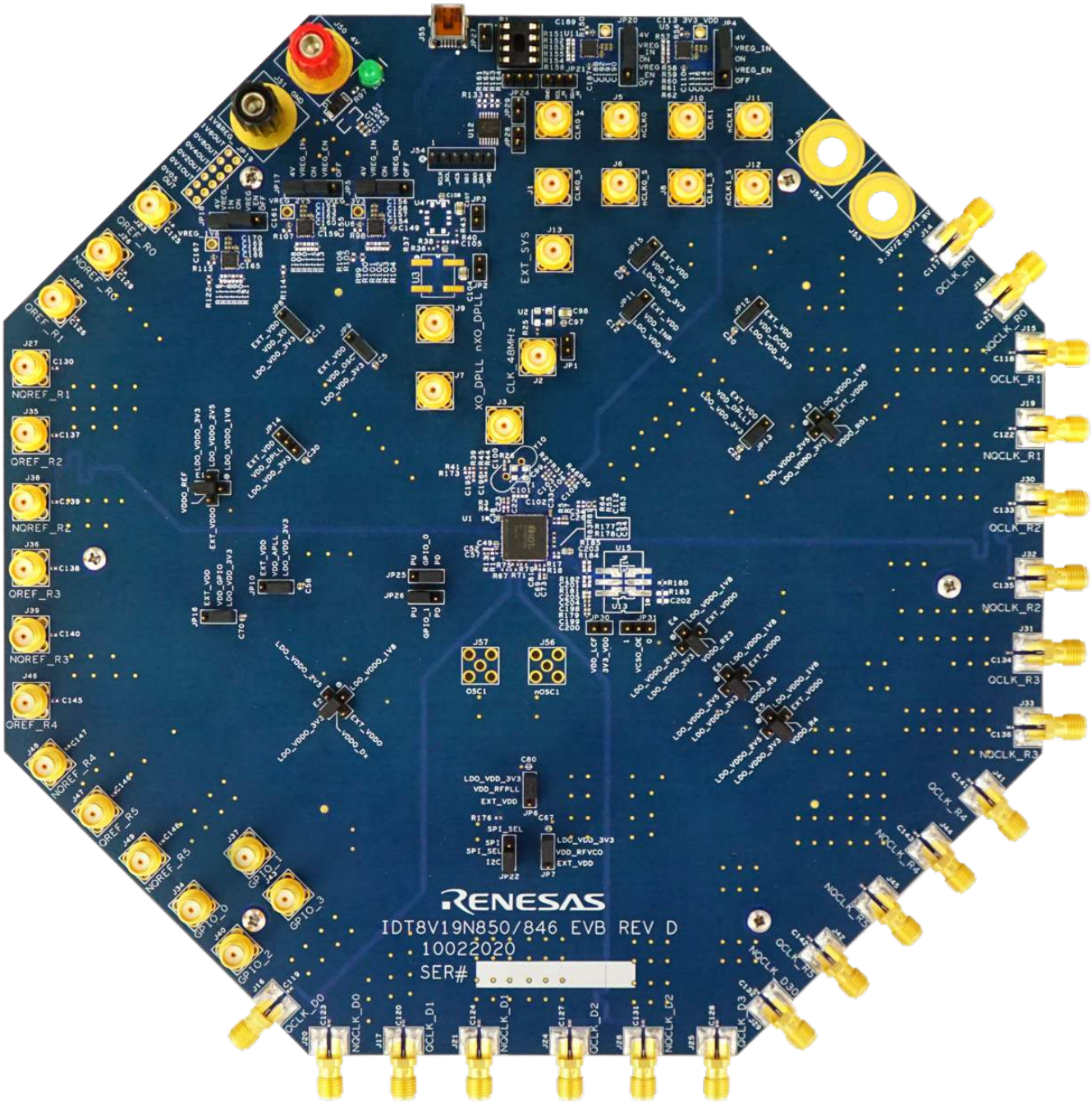


Figure 18. 8V19N850 EVB – Top View

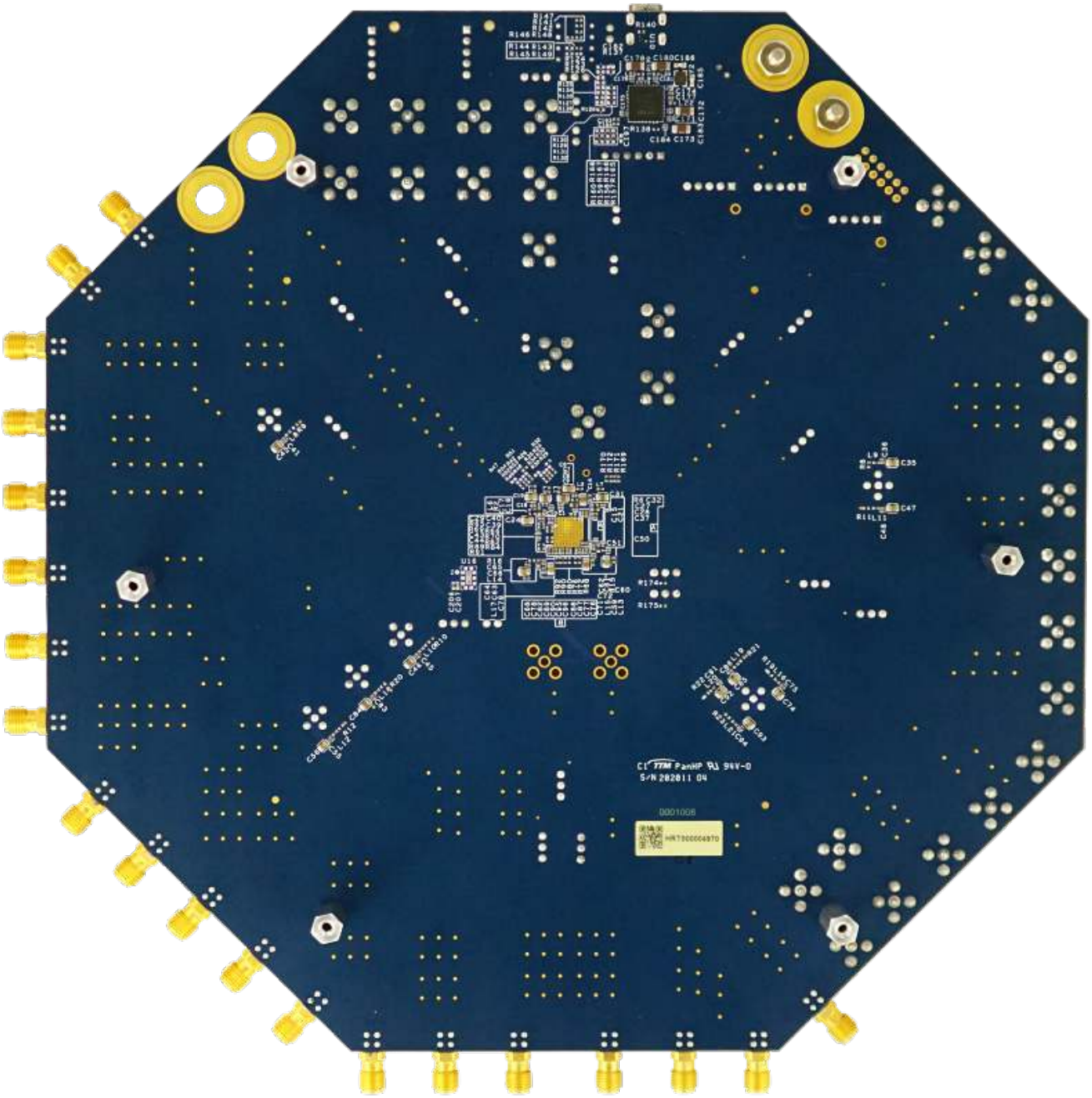


Figure 19. 8V19N850 EVB – Bottom View

2.2 Layout Guidelines

For information, see the *8V19N850 Hardware Design Guide*.

2.3 Schematic Diagrams

For the schematic diagrams, see the end of this document.

2.4 Bill of Materials

Item	Qty	Reference	Part	Manufacturer Part Number
1	78	C1,C3,C5,C7,C9,C10,C12,C13,C15,C16,C18,C20,C23,C25,C28,C29,C30,C32,C34,C36,C37,C40,C41,C44,C45,C48,C49,C54,C55,C57,C58,C60,C62,C63,C65,C67,C70,C72,C73,C75,C76,C78,C80,C82,C83,C86,C87,C90,C91,C94,C95,C97,C105,C108,C153,C172,C174,C175,C176,C177,C179,C181,C183,C184,C110,C113,C149,C155,C159,C161,C165,C167,C187,C189, C100, C199,C204,C206	0.1uF	C0402C104K4RACTU or 0402YC104JAT2A
2	24	C2,C6,C11,C14,C19,C24,C31,C35,C42,C46,C47,C56,C59,C66,C71,C74,C79,C84,C85,C92,C93,C98,C104,C107	10uF	08056C106KAT2A
3	30	C4,C99,C103,C106,C109,C117,C118,C119,C120,C121,C122,C123,C124,C127,C128,C131,C132,C133,C134,C135,C136,C141,C142,C143,C144,C193,C194, C195, C196, C200	1.0uF	EMK105BJ105KV-F
4	6	C8,C17,C27,C61,C64, C198	22uF	CL05A226MQ6ZUN8 or 04026D226MAT2A
5	4	C26,C52,C69, C182	33pF	GJM1555C1H330FB01D
6	12	C38,C39,C43,C50,C53,C77,C81,C88,C89,C96, C205, C207	100pF	C0402C101J3GACTU
7	2	C185,C186	12pF	06036C120KAT4A
8	4	C171,C173,C178,C180	10uF	1206YC106KAT2A
9	25	C111,C114,C115,C116,C152,C154,C156,C157, C158,C160,C162,C163,C164,C166,C168,C169, C170,C188,C190,C191,C192, C21, C33, C68, C51	10uF	GRM155R60G106ME44D
10	1	C151	0.01uF	GRM155R61A103KA01D
11	1	D1	Diode General Purpose 400V 1A	CGRA4004-G
12	11	E1,E2,E3,E4,E5,E6,JP4,JP5,JP17,JP18,JP20	0.100 SPACING 5-PIN HEADER	TSW-105-07-F-S
13	7	JP1,JP2,JP3, JP27, JP30, JP28, JP29	0.100 SPACING HEADER 2x1	TSW-102-07-F-S
15	17	JP6, JP7, JP8,JP9,JP10,JP11,JP12,JP13,JP14,JP15,JP16,JP21,JP22,JP24, JP25, JP26, JP31	0.100 SPACING HEADER 3x1	TSW-103-07-F-S
16	29	J1,J2,J3,J4,J5,J6,J7,J8,J9,J10,J11,J12,J13,J22, J23,J26,J27,J34,J35,J36,J37,J38,J39,J40,J43,J46,J47,J48,J49	SMA VERTICAL	142-0701-201

Item	Qty	Reference	Part	Manufacturer Part Number
17	20	J14,J15,J16,J17,J18,J19,J20,J21,J24,J25,J28,J29,J30,J31,J32,J33,J41,J42,J44,J45	SMA_END_LAUNCH_PCB_cinch	142-0761-881
18	1	J50	4V - BANANA (RED)	111-0702-001
19	1	J51	GND - BANANA (BLACK)	111-0703-001
20	1	J54	HEADER 1x6	22-28-4062
21	1	J55	USB PORT 548190589	548190589
22	1	LD1	LED_1.6V_Green	WP7113GD
23	24	L1,L2,L3,L4,L5,L6,L7,L8,L9,L10,L11,L12,L13,L14,L15,L16,L17,L18,L19,L20,L21,L22,L23,L24	220	BLM15HB221SN1D
24	1	P1	A08-LC-TT	A08-LC-TT
25	15	R1,R2,R6,R8,R9,R10,R11,R12,R15,R16,R19,R20,R21,R22,R23	1	ERJ-2GEJ1R0X
26	1	R17	200	ERA-2AED201X
27	47	R32,R36,R51,R140,R39,R58,R61,R62,R100,R103,R104,R105,R106,R109,R113,R114,R118,R120,R122,R131,R133,R153,R155,R157,R159,R160, R124, R137, C125, C126, C129, C130, C137, C138, C139, C145, C146, C147, C148, R44, C112, C140, C201, C203, R177,R179,R150	0	ERJ-2GE0R00X
28	1	R25	33.2	ERJ-2RKF33R2X
29	10	R26,R27,R31,R37,R41,R43,R45,R46,R50,R63	49.9	ERJ-2RKF49R9X
30	12	R29,R30,R33,R34,R48,R49,R52,R53, R169, R170, R171, R172	2.67k	ERJ-2RKF2671X
31	10	R56,R98,R107,R115,R128,R144,R145, R125, R127, R166	10K	ERJ-2GEJ103X
32	20	R65,R66,R67,R68,R69,R70,R71,R72,R75,R76, R79,R80,R81,R82,R83,R84,R89,R90,R91,R92	180	ERA-2AEB181X
33	8	R146,R147,R148, R176, R174, R175, R143, R180	1K	ERJ-2RKF1001X
34	3	R129,R130,R132	1.5K	ERJ-2RKF1501X
35	4	R138,R139,R141,R142	12k	ERJ-2RKF1202X
36	5	U5,U6,U7,U8,U11	TPS7A8300RGRT	TPS7A8300RGRT
37	1	U9	FT232HQ-REEL	FT232HQ-REEL
38	1	U10	TPD4S012DRYR	TPD4S012DRYR
39	1	U12	LSF0204PWR_TSSOP14	LSF0204PWR_TSSOP14
40	1	Y2	ABM8G-12.000MHZ-18-D2Y-T	ABM8G-12.000MHZ-18-D2Y-T
41	2	R4,R97	510	ERA-2AED511X
42	1	R5	2k	ERA-2AED202X

Item	Qty	Reference	Part	Manufacturer Part Number
43	1	R14	300	ERA-2AED301X
44	1	C22	470p	GRM155R72A471KA01D
45	1	U1	8V19N850	8V19N850DNLGI

3. Ordering Information

Part Number	Description
8V19N850-EVK	8V19N850 Evaluation Board

4. Revision History

Revision	Date	Description
1.0	Mar 25, 2021	Initial release.