



# STY140NS10

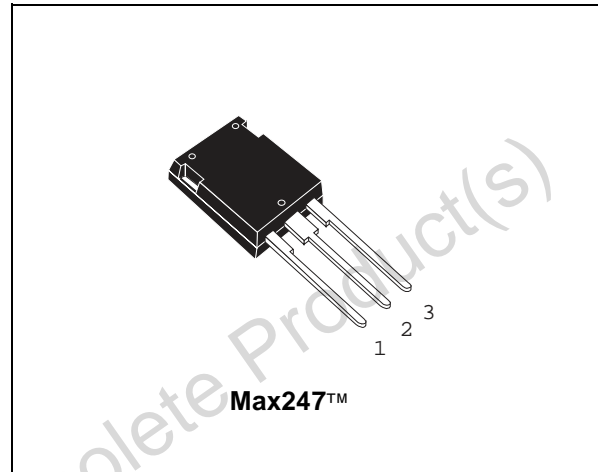
## N-CHANNEL 100V - 0.009 Ω - 140A MAX247™ MESH OVERLAY™ POWER MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STY140NS10	100V	<0.011Ω	140A

- TYPICAL R<sub>DS(on)</sub> = 0.009Ω
- STANDARD THRESHOLD DRIVE
- 100% AVALANCHE TESTED

### DESCRIPTION

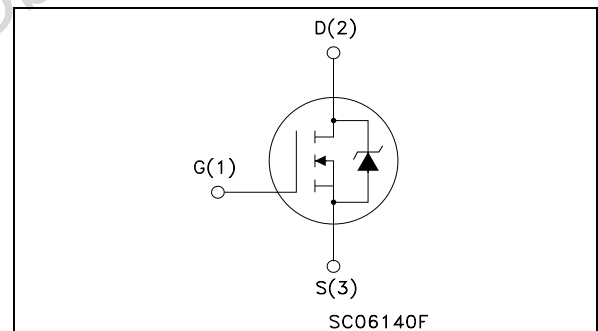
Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest R<sub>DS(on)</sub> per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.



### APPLICATIONS

- HIGH CURRENT, HIGH SWITCHING SPEED
- SWITCH MODE POWER SUPPLY (SMPS)

### INTERNAL SCHEMATIC DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	100	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	100	V
V <sub>GS</sub>	Gate- source Voltage	± 20	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	140	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	99	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	560	A
P <sub>tot</sub>	Total Dissipation at T <sub>C</sub> = 25°C	450	W
	Derating Factor	3	W/°C
E <sub>AS</sub> (1)	Single Pulse Avalanche Energy	2900	mJ
dv/dt (2)	Peak Diode Recovery voltage slope	5	V/ns
T <sub>stg</sub>	Storage Temperature	-55 to 175	°C
T <sub>j</sub>	Operating Junction Temperature	-55 to 175	°C

(●) Pulse width limited by safe operating area.

(1) Starting T<sub>j</sub> = 25 °C, I<sub>D</sub> = 70A, V<sub>DD</sub> = 50V

(2) I<sub>SD</sub> ≤ 140A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ V(BR)<sub>DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>.

**STY140NS10****THERMAL DATA**

Rthj-case	Thermal Resistance Junction-case	Max	0.33	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	30	°C/W
T <sub>j</sub>	Maximum Lead Temperature For Soldering Purpose	Typ	300	°C

**ELECTRICAL CHARACTERISTICS** (T<sub>case</sub> = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	100			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating T <sub>C</sub> = 125°C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> I <sub>D</sub> = 250 μA	2		4	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V I <sub>D</sub> = 70 A		0.009	0.011	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (*)	Forward Transconductance	V <sub>DS</sub> = 20 V I <sub>D</sub> = 70 A		50		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		12600		pF
C <sub>oss</sub>	Output Capacitance			2100		pF
C <sub>riss</sub>	Reverse Transfer Capacitance			690		pF

**ELECTRICAL CHARACTERISTICS** (continued)

**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 50\text{ V}$ $I_D = 70\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 1)		40 150		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD}=50\text{V}$ $I_D=140\text{A}$ $V_{GS}=10\text{V}$ (see test circuit, Figure 2)		450 70 170	600	nC nC nC

**SWITCHING OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ $t_f$	Turn-off Delay Time Fall Time	$V_{DD} = 50\text{ V}$ $I_D = 70\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 1)		465 270		ns ns

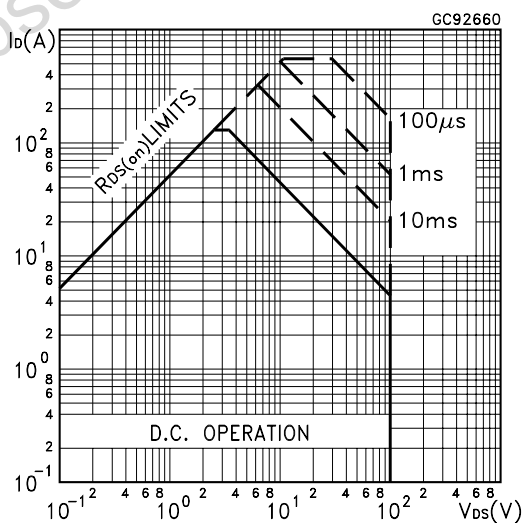
**SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM} (\bullet)$	Source-drain Current Source-drain Current (pulsed)				140 560	A A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 140\text{ A}$ $V_{GS} = 0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 140\text{ A}$ $di/dt = 100\text{A}/\mu\text{s}$ $V_r = 20\text{ V}$ $T_j = 150^\circ\text{C}$ (Inductive Load, Figure 3)			275 2 15	ns $\mu\text{C}$ A

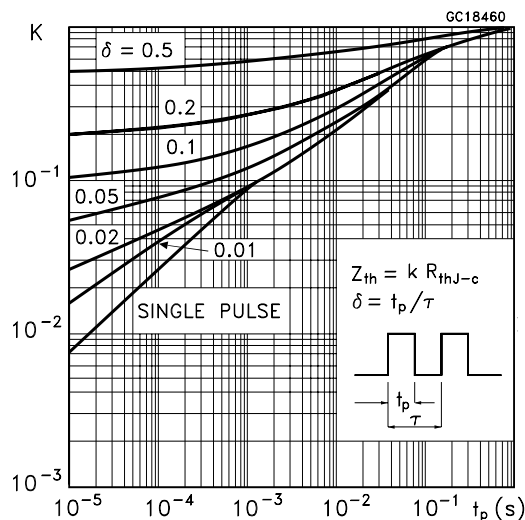
(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

( $\bullet$ ) Pulse width limited by safe operating area.

Safe Operating Area

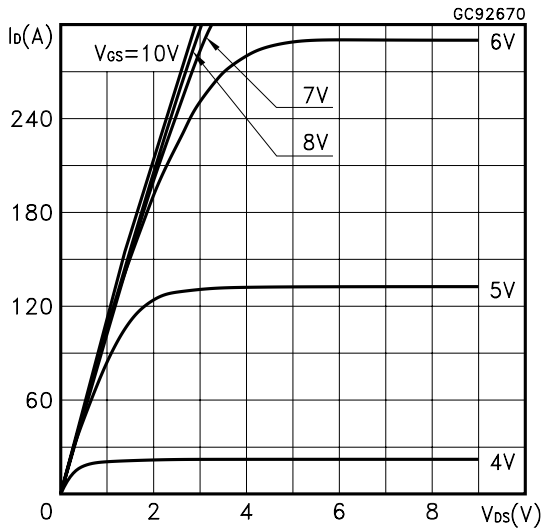


Thermal Impedance

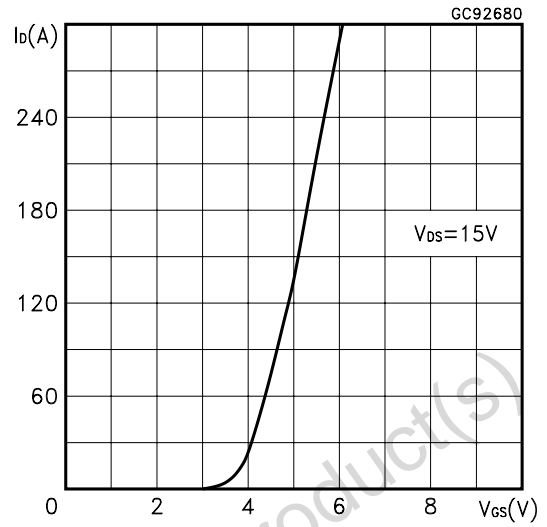


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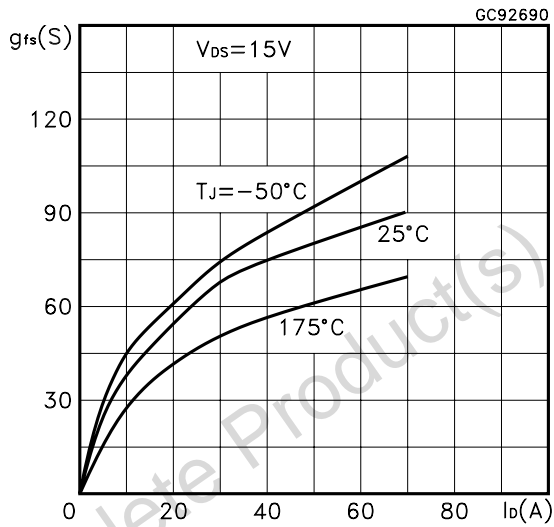
Output Characteristics



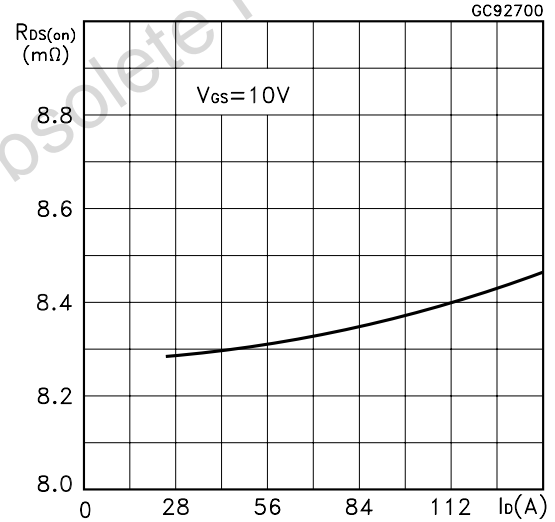
Transfer Characteristics



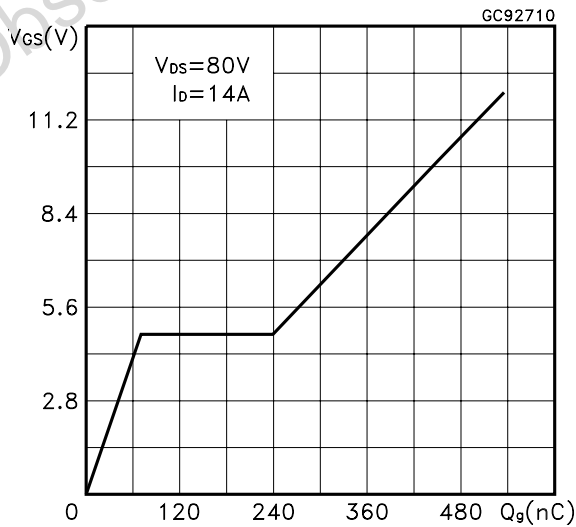
Transconductance



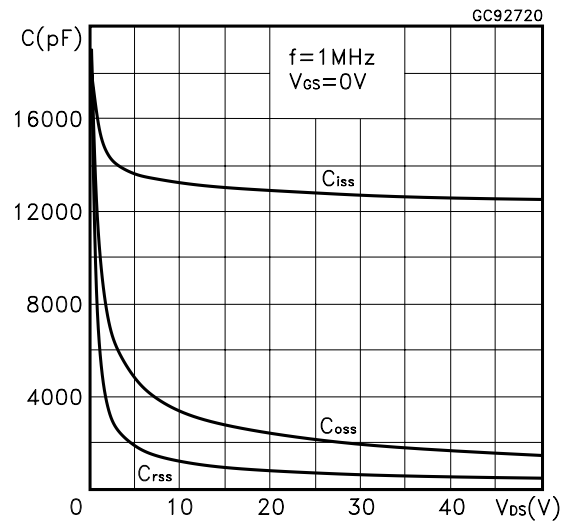
Static Drain-source On Resistance



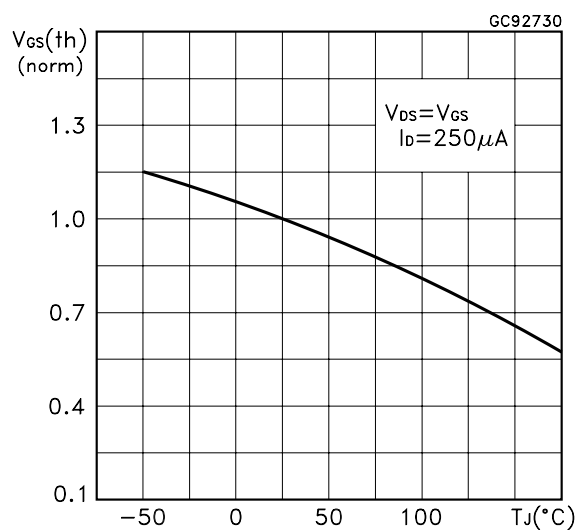
Gate Charge vs Gate-source Voltage



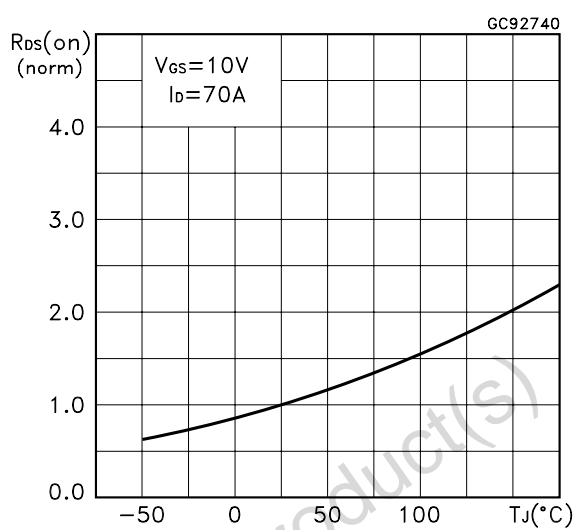
Capacitance Variations



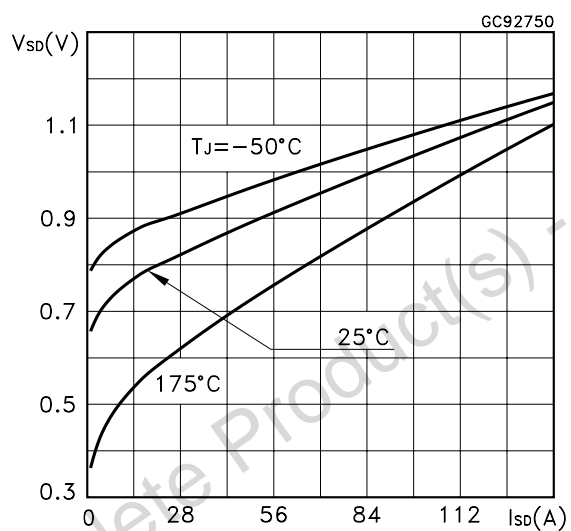
Normalized Gate Threshold Voltage vs Temperature



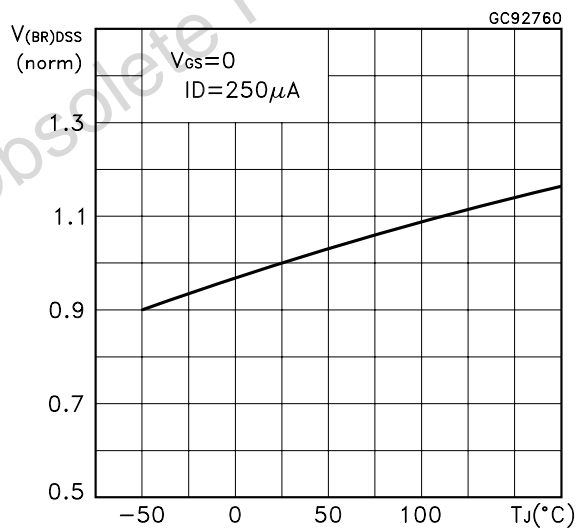
Normalized on Resistance vs Temperature



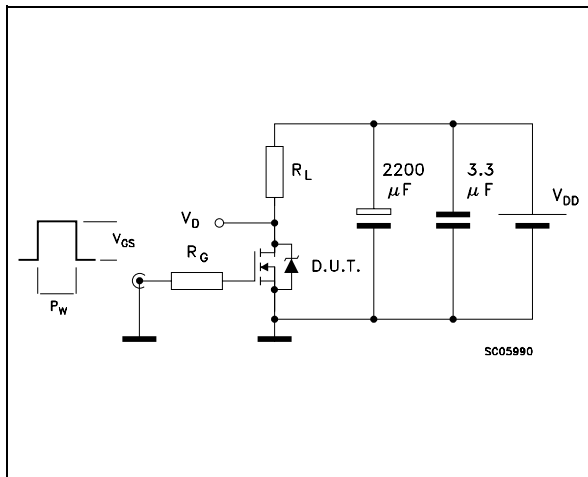
Source-drain Diode Forward Characteristics



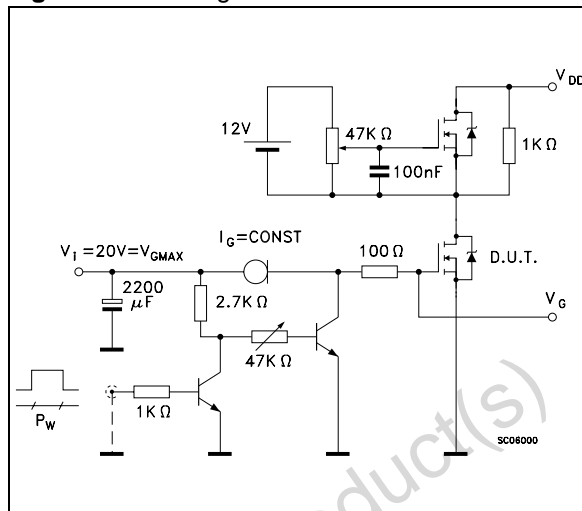
Normalized Breakdown Voltage vs Temperature



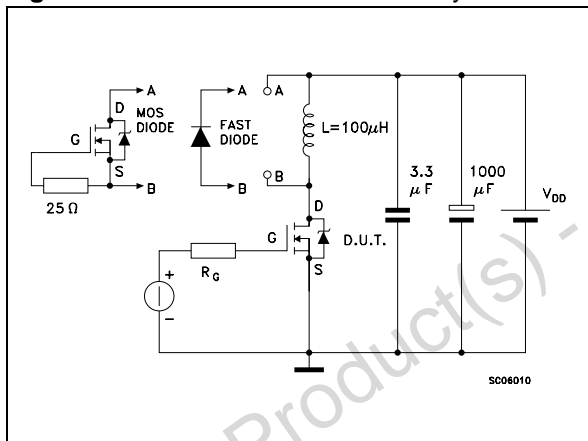
**Fig. 1: Switching Times Test Circuits For Resistive Load**



**Fig. 2: Gate Charge test Circuit**

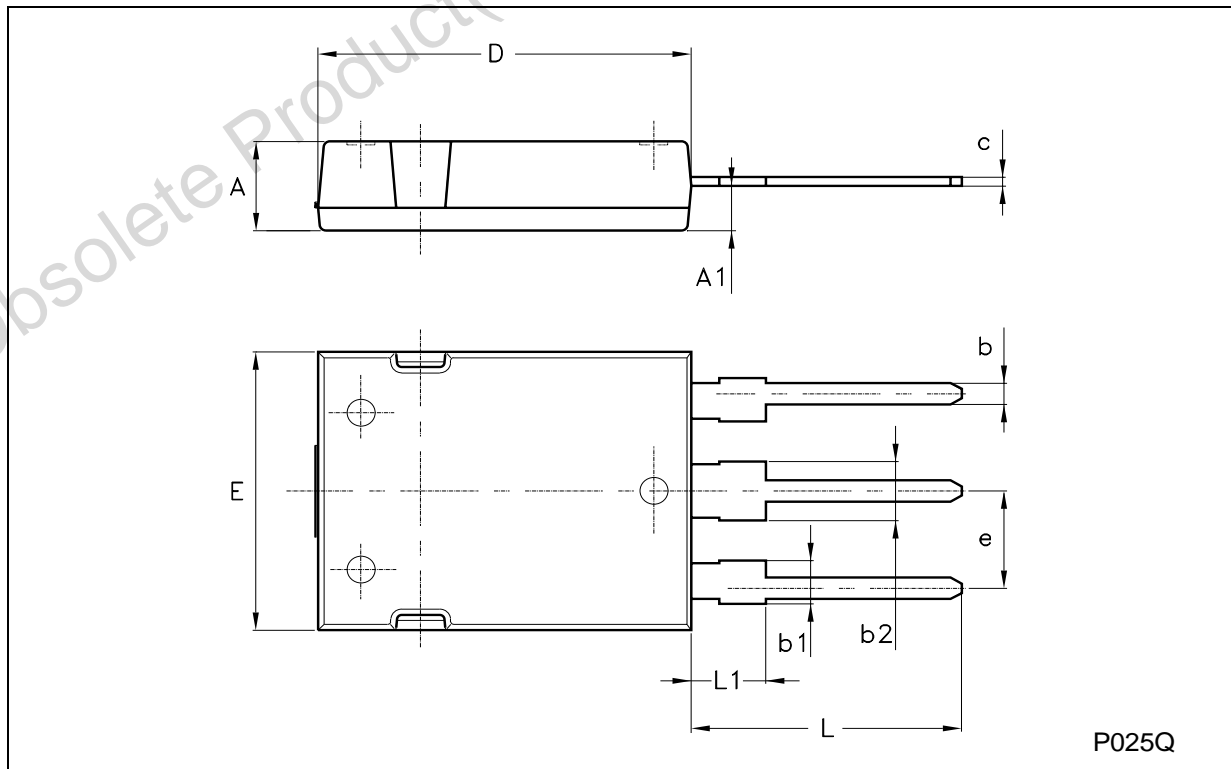


**Fig. 3: Test Circuit For Diode Recovery Behaviour**



**Max247 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.70		5.30			
A1	2.20		2.60			
b	1.00		1.40			
b1	2.00		2.40			
b2	3.00		3.40			
c	0.40		0.80			
D	19.70		20.30			
e	5.35		5.55			
E	15.30		15.90			
L	14.20		15.20			
L1	3.70		4.30			



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