Fast Sample and Hold

Features

- Maximum Acquisition Time (10V Step to 0.1%) ... 4μs
  (10V Step to 0.01%) 6μs
- Low Droop Rate (C_H = 1000pF) ..... 5μV/ms (Typ.)
- Gain Bandwidth Product ..... 2.5MHz (Typ.)
- Low Effective Aperture Delay Time ..... 30ns (Typ.)
- TTL Compatible Control Input
- ±12V to ±15V Operation

Applications

- 12-Bit Data Acquisition
- Digital to Analog Deglitcher
- Auto Zero Systems
- Peak Detector
- Gated Operational Amplifier

Description

The HA-2420/2425 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and MOSFET input unity gain amplifier.

With an external holding capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

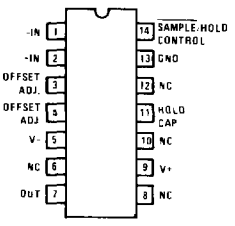
Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc. For more information, please see Application Note 517.

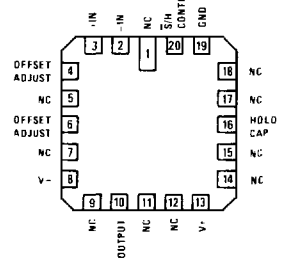
The HA-2420/25 is offered in a 14 pin Ceramic or Plastic DIP and a 20 pad Ceramic LCC or 20 pad PLCC. The MIL-STD-883 data sheet for this device is available on request.

Pinouts

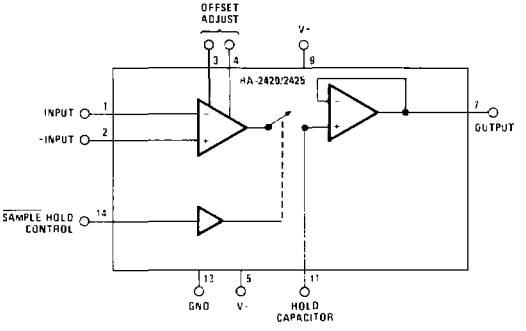
14 PIN CERAMIC/PLASTIC DIP
TOP VIEW



20 PAD LCC/PLCC
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage ..... ±24V
Digital Input Voltage (Sample and Hold Pin) ..... +8V, -15V
Output Current ..... Short Circuit Protected
Junction Temperature ..... +175°C

Operating Temperature Range

HA-2420-2 ..... $-55°C \leq T_A \leq +125°C$
HA-2425-5/-7 ..... $0°C \leq T_A \leq +75°C$
Storage Temperature Range ..... $-65°C \leq T_A \leq +150°C$

Electrical Specifications

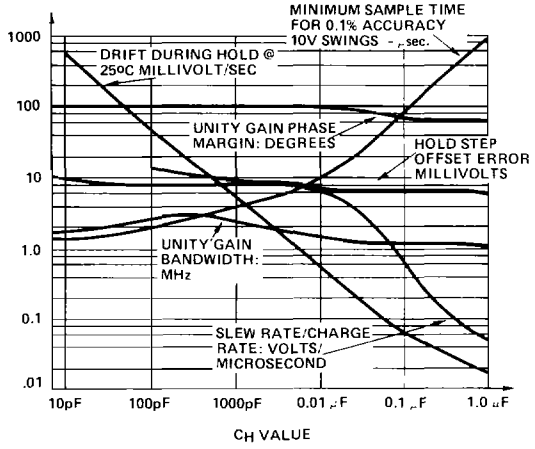
Test Conditions (Unless Otherwise Specified) $V_{SUPPLY} = \pm 15.0V$; $C_H = 1000pF$; *Digital Input:* $V_{IL} = +0.8V$ *(Sample)*, $V_{IH} = +2.0V$ *(Hold)*, Unity Gain Configuration (Output tied to -Input)

PARAMETER	TEMP	HA-2420-2 MIN	HA-2420-2 TYP	HA-2420-2 MAX	HA-2425-5/-7 MIN	HA-2425-5/-7 TYP	HA-2425-5/-7 MAX	UNITS
INPUT CHARACTERISTICS								
Input Voltage Range	Full	±10	-	-	±10	-	-	V
Offset Voltage	+25°C	-	2	4	-	3	6	mV
	Full	-	3	6	-	4	8	mV
Bias Current	+25°C	-	40	200	-	40	200	nA
	Full	-	-	400	-	-	400	nA
Offset Current	+25°C	-	10	50	-	10	50	nA
	Full	-	-	100	-	-	100	nA
Input Resistance	+25°C	5	10	-	5	10	-	MΩ
Common Mode Range	Full	±10	-	-	±10	-	-	V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 1, 4)	Full	25K	50K	-	25K	50K	-	V/V
Common Mode Rejection (Note 2)	Full	-80	-90	-	-74	-90	-	dB
Hold Mode Feedthrough Attenuation (Note 3)	Full	-	-76	-	-	-76	-	dB
Gain Bandwidth Product (Note 3)	+25°C	-	2.5	-	-	2.5	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10	-	-	±10	-	-	V
Output Current	+25°C	±15	-	-	±15	-	-	mA
Full Power Bandwidth (Notes 3, 4)	+25°C	-	100	-	-	100	-	kHz
Output Resistance (D.C.)	+25°C	-	0.15	-	-	0.15	-	Ω
TRANSIENT RESPONSE								
Rise Time (Notes 3, 5)	+25°C	-	75	100	-	75	100	ns
Overshoot (Notes 3, 5)	+25°C	-	25	40	-	25	40	%
Slew Rate (Notes 3, 6)	+25°C	3.5	5	-	3.5	5	-	V/μs
DIGITAL INPUT CHARACTERISTICS								
Digital Input Current ($V_{IN} = 0V$)	Full	-	-	-0.8	-	-	-0.8	mA
Digital Input Current ($V_{IN} = +5.0V$)	*Full*	-	-	*20*	-	-	*20*	μA
Digital Input Voltage (Low)	Full	-	-	0.8	-	-	0.8	V
Digital Input Voltage (High)	Full	2.0	-	-	2.0	-	-	V
SAMPLE AND HOLD CHARACTERISTICS								
Acquisition Time to 0.1% 10V Step (Note 3)	+25°C	-	2.3	4	-	2.3	4	μs
Acquisition Time to 0.01% 10V Step (Note 3)	+25°C	-	3.2	6	-	3.2	6	μs
Aperture Time (Note 9)	+25°C	-	30	-	-	30	-	ns
Effective Aperture Delay Time	+25°C	-	30	-	-	30	-	ns
Aperture Uncertainty	+25°C	-	5	-	-	5	-	ns
Drift Current (Notes 3, 7)	+25°C	-	5	-	-	5	-	pA
HA1-2420, HA4-2420	Full	-	1.8	10	-	-	-	nA
HA1-2425	Full	-	-	-	-	0.1	1.0	nA
HA3-2425, HA4P2425	Full	-	-	-	-	7.5	10.0	nA
Hold Step Error (Note 7)	+25°C	-	10	20	-	10	20	mV
POWER SUPPLY CHARACTERISTICS								
Supply Current (+)	+25°C	-	3.5	5.5	-	3.5	5.5	mA
Supply Current (-)	+25°C	-	2.5	3.5	-	2.5	3.5	mA
Power Supply Rejection	Full	-80	-90	-	-74	-90	-	dB

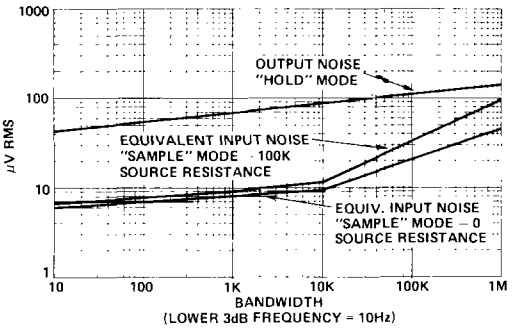
NOTES:
1. $R_L = 2k\Omega$.
2. $V_{CM} = \pm 10VDC$.
3. $A_V = \pm 1$, $R_L = 2k\Omega$, $C_L = 50pF$.
4. $V_{OUT} = 20V$ peak-to-peak.
5. $V_{OUT} = 200mV$ peak-to-peak.
6. $V_{OUT} = 10.0V$ peak-to-peak.
7. $V_{IN} = 0V$.
8. $f_{IN} \leq 100kHz$.
9. Derived from computer simulation only; not tested.

Performance Curves $V_{SUPPLY} = \pm 15VDC$, $T_A = +25^oC$, $C_H = 1000pF$ Unless Otherwise Specified

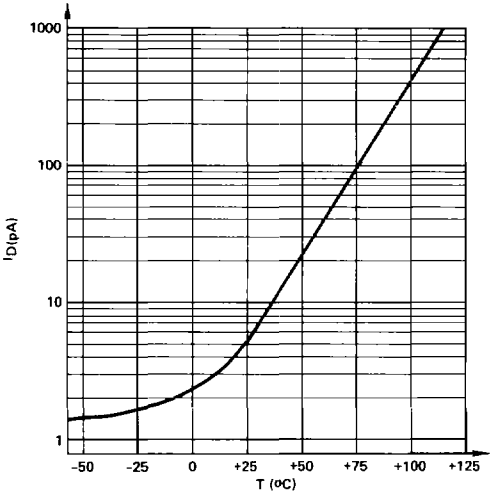
TYPICAL SAMPLE AND HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITOR



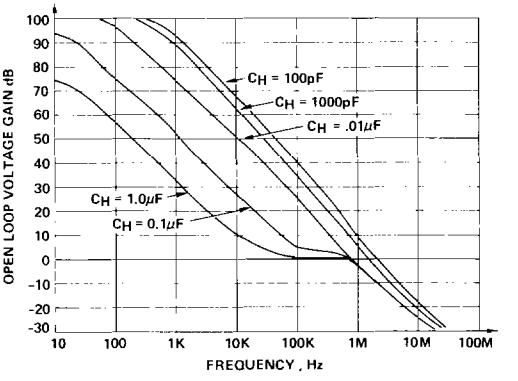
BROADBAND NOISE CHARACTERISTICS



DRIFT CURRENT vs. TEMPERATURE

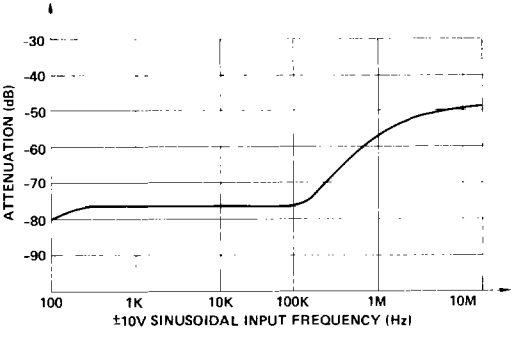


OPEN LOOP FREQUENCY RESPONSE

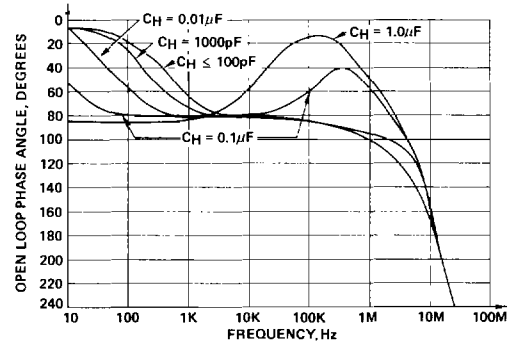


HOLD MODE FEED THROUGH ATTENUATION

$C_H = 1000pF$



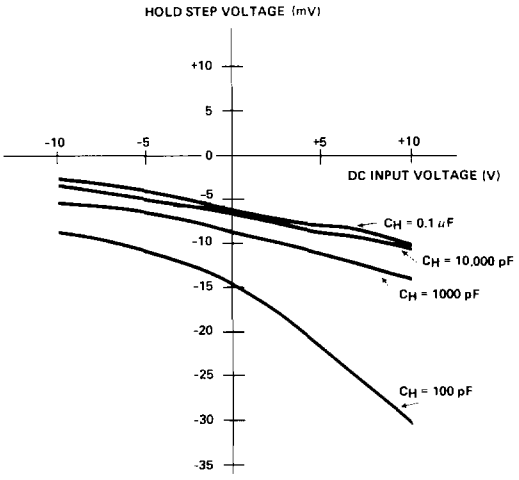
OPEN LOOP PHASE RESPONSE



7 SAMPLE & HOLD AMPLIFIERS

Offset and Gain Adjustment

HOLD STEP vs. INPUT VOLTAGE



OFFSET ADJUSTMENT

The offset voltage of the HA-2420/2425 may be adjusted using a 100kΩ trim pot, as shown in Figure 6. The recommended adjustment procedure is:

1. Apply zero volts to the sample-and-hold input, and a square wave to the $\overline{S}$/H control.
2. Adjust the trim pot for zero volts output in the hold mode.

GAIN ADJUSTMENT

The linear variation in pedestal voltage with sample-and-hold input voltage causes a -0.06% gain error (C_H = 1000pF). In some applications (D/A deglitcher, A/D converter) the gain error can be adjusted elsewhere in the system, while in other applications it must be adjusted at the sample-and-hold. The two circuits shown below demonstrate how to adjust gain error at the sample-and-hold.

The recommended procedure for adjusting gain error is:

1. Perform offset adjustment.
2. Apply the nominal input voltage that should produce a +10V output.
3. Adjust the trim pot for +10V output in the hold mode.
4. Apply the nominal input voltage that should produce a -10V output.
5. Measure the output hold voltage ($V_{-10\ NOMINAL}$). Adjust the trim pot for an output hold voltage of

$$\frac{(V_{-10\ NOMINAL}) + (-10V)}{2}$$

INVERTING CONFIGURATION

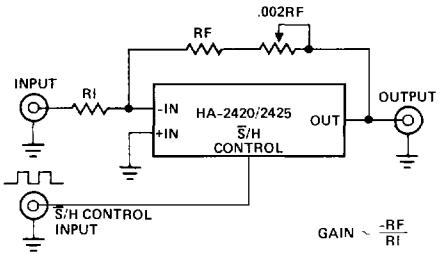


FIGURE 2.

NONINVERTING CONFIGURATION

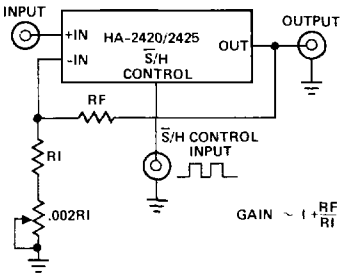


FIGURE 3.

Test Circuits

HOLD STEP ERROR AND DRIFT CURRENT

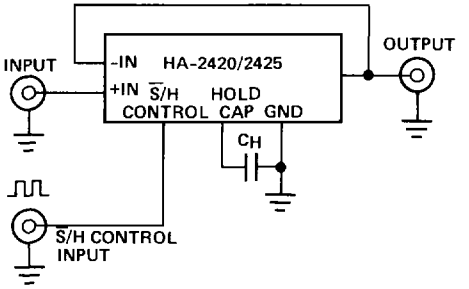


FIGURE 4.

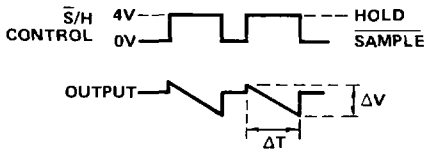
HOLD STEP ERROR TEST

1. With a D.C. input voltage, observe the following waveforms:

2. Set rise/fall times of S/H Control to approximately 20ns.

DRIFT CURRENT TEST

1. With a D.C. input voltage, observe the following waveforms:



2. Measure the slope of the output during hold, $\Delta V/\Delta t$, and compute drift current from: $I_D = C_H \Delta V/\Delta t$.

HOLD MODE FEEDTHROUGH ATTENUATION

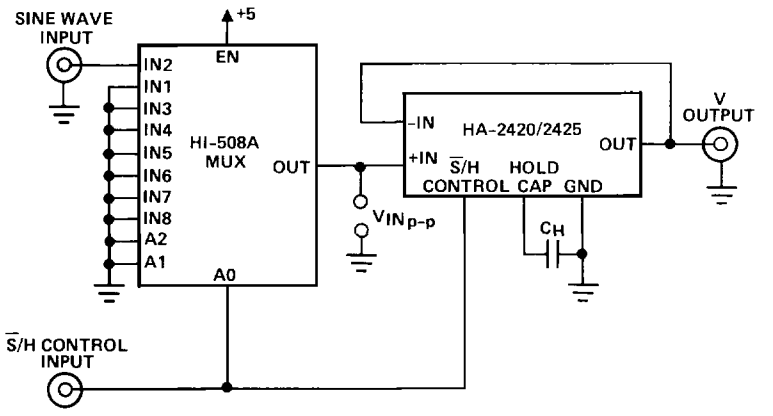


FIGURE 5.

NOTE: Compute hold mode feedthrough attenuation from the formula:

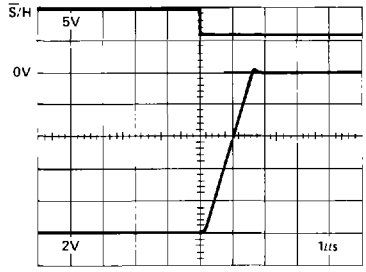
$$\text{Feedthrough Attenuation} = 20 \text{ Log } \frac{V_{OUT\ HOLD}}{V_{IN\ HOLD}}$$

Where V_{OUT} HOLD = Peak-to-Peak value of output sinewave during the hold mode.

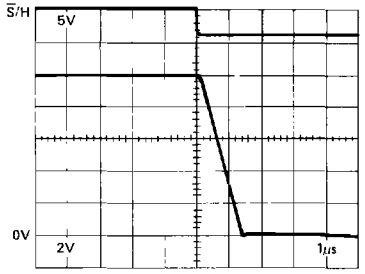
7 SAMPLE & HOLD AMPLIFIERS

Acquisition Times (C_H = 1000pF)

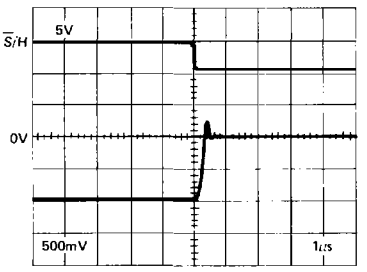
-10 TO 0V



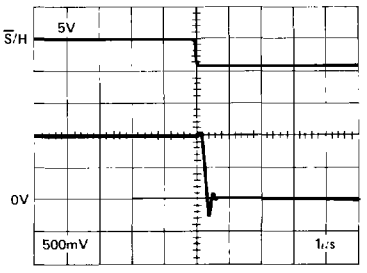
+10V TO 0V



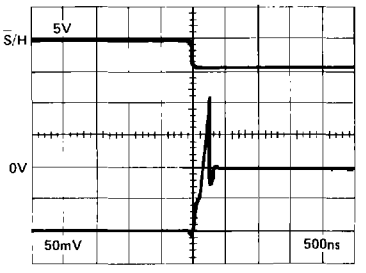
-1V TO 0V



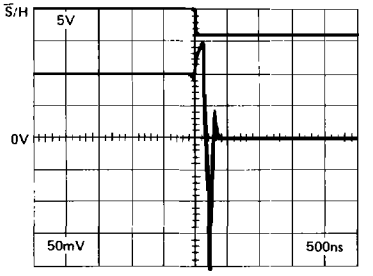
+1V TO 0V



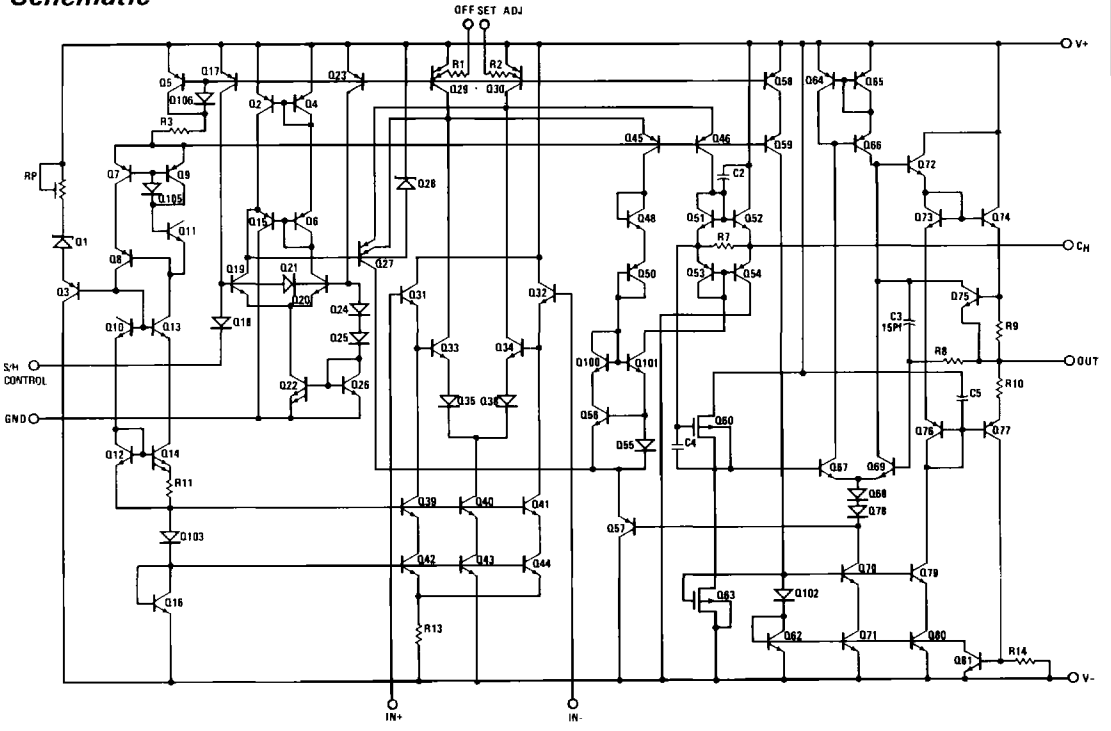
-100mV TO 0V



+100mV TO 0V



Schematic



Applications

BASIC SAMPLE-AND-HOLD
TOP VIEW

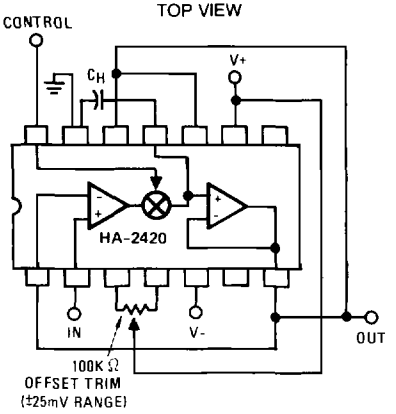


FIGURE 6.

GUARD RING LAYOUT
BOTTOM VIEW

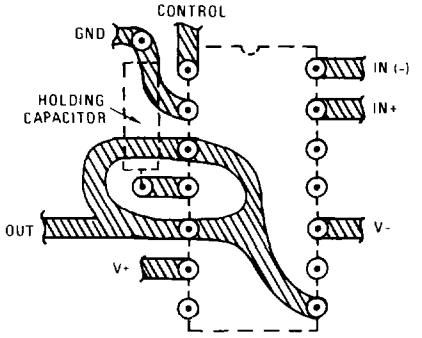


FIGURE 7.

NOTES:

1. Figure 6 shows a typical unity gain circuit, with Offset Zeroing. All of the other normal op amp feedback configurations may be used with the HA-2420/2425. The input amplifier may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.
2. The method used to reduce leakage paths on the P.C. board and the device package is shown in Figure 7. This guard ring is recommended to minimize the drift during hold mode.
3. The holding capacitor should have extremely high insulation resistance and low dielectric absorption. Polystyrene (below +85°C), Teflon, or Parlene types are recommended.

   For more applications, consult Harris Application Note 517, or factory applications group.

Glossary of Terms:

ACQUISITION TIME:

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

APERTURE TIME:

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

EFFECTIVE APERTURE DELAY TIME (EADT):

The difference between propagation time from the analog input to the S/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the $\overline{S}/H$ amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

APERTURE UNCERTAINTY:

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

DRIFT CURRENT:

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D\ (pA) = C_H\ (pF) \times \frac{\Delta V}{\Delta T}\ (Volts/sec)$$

Die Characteristics

Transistor Count 78
Die Dimensions ..... 97 x 61 x 19 mils
Substrate Potential ..... $-V_{SUPPLY}$
Process ..... Bipolar DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	94	39
Ceramic LCC	88	28

7 SAMPLE & HOLD AMPLIFIERS