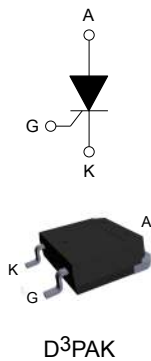


80 A 800 V high temperature thyristor (SCR) in D³PAK package



Features

- High junction temperature: $T_j = 150\text{ °C}$
- Blocking voltage: $V_{DRM} = V_{RRM} = 800\text{ V}$
- Nominal current: $I_{T(RMS)} = 80\text{ A}$
- Gate triggering current: $I_{GT\text{ max.}} = 50\text{ mA}$
- High noise immunity: $dV/dt > 1\text{ kV}/\mu\text{s}$
- Surface mounted device D³PAK for compact designs
- Increase of thermal margin due to extended T_j up to 150 °C
- Low I_D and I_R in blocking state
- [Ecopack2](#) (includes halogen free & RoHS compliance)

Applications

- AC-DC rectifier controlled bridge
- Motorbike voltage regulator
- Variable speed motor drive
- Battery charging system
- AC solid state relay
- By-pass switch of UPS
- Industrial welding systems
- Motor soft starter

Description

Available in power surface mount package (D³PAK), the TM8050H-8D3 device is an 800V SCR thyristor suitable for applications where high power switching ($I_{T(RMS)} = 80\text{ A}$) and low power dissipation ($V_{TM} = 1.55\text{ V}$ at 160 A) are key features. These features make it ideal for motorbike voltage regulator, by-pass AC switch, controlled rectifier bridge, solid state relay, battery charger, welding equipment and motor driver applications.

Product status link	
TM8050H-8D3	
Product summary	
$I_{T(RMS)}$	80 A
V_{DRM}/V_{RRM}	800 V
I_{GT}	50 mA
T_j	150 °C

1 Characteristics

Table 1. Absolute maximum ratings (limiting values), $T_j = 25\text{ °C}$ unless otherwise stated

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current (180 ° conduction angle)		$T_c = 130\text{ °C}$	80	A
$I_{T(AV)}$	Average on-state current (180 ° conduction angle)			50	A
I_{TSM}	Non repetitive surge peak on-state current, $V_R = 0\text{ V}$	$t_p = 8.3\text{ ms}$	$T_j\text{ initial} = 25\text{ °C}$	731	A
		$t_p = 10\text{ ms}$		670	
I^2t	I^2t value for fusing		$T_j = 25\text{ °C}$	2245	A^2s
V_{RRM}/V_{DRM}	Maximum repetitive symmetric blocking voltage			800	V
di/dt	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$, $t_r \leq 100\text{ ns}$	$F = 50\text{ Hz}$	$T_j = 25\text{ °C}$	200	$A/\mu s$
I_{GM}	Peak gate current	$t_p = 20\text{ }\mu s$	$T_j = 150\text{ °C}$	8	A
$P_{G(AV)}$	Average gate power dissipation		$T_j = 150\text{ °C}$	1	W
V_{RGM}	Maximum peak reverse gate voltage			5	V
T_{stg}	Storage junction temperature range			-40 to +150	$^{\circ}C$
T_j	Operating junction temperature range			-40 to +150	$^{\circ}C$
T_L	Maximum lead temperature soldering during 10 s			245	$^{\circ}C$

Table 2. Electrical characteristics ($T_j = 25\text{ °C}$ unless otherwise specified)

Symbol	Test conditions		Value	Unit	
I_{GT}	$V_D = 12\text{ V}$, $R_L = 33\text{ }\Omega$		Min.	2.5	mA
			Max.	50	
V_{GT}	$V_D = 12\text{ V}$, $R_L = 33\text{ }\Omega$		Max.	1.5	V
V_{GD}	$V_D = V_{DRM}$, $R_L = 3.3\text{ k}\Omega$	$T_j = 125\text{ °C}$	Min.	0.2	V
$I_H^{(1)}$	$I_T = 500\text{ mA}$, gate open		Max.	100	mA
I_L	$I_G = 1.2 \times I_{GT}$		Max.	125	mA
t_{gt}	$I_T = 80\text{ A}$, $V_D = V_{DRM}$, $I_G = 200\text{ mA}$, $di_G/dt = 0.2\text{ A}/\mu s$		Typ.	3	μs
dV/dt	$V_D = 67\% V_{DRM}$, gate open	$T_j = 150\text{ °C}$	Min.	1000	$V/\mu s$
t_q	$I_T = 33\text{ A}$, $di_T/dt = 10\text{ A}/\mu s$, $V_R = 75\text{ V}$, $V_D = 400\text{ V}$, $dV_D/dt = 20\text{ V}/\mu s$, $t_p = 100\text{ }\mu s$	$T_j = 150\text{ °C}$	Max.	150	μs

1. For both polarities of A2 referenced to A1

Table 3. Static characteristics

Symbol	Test conditions			Value	Unit
$V_{TM}^{(1)}$	$I_{TM} = 160\text{ A}$, $t_p = 380\ \mu\text{s}$	$T_j = 25\ ^\circ\text{C}$	Max.	1.55	V
$V_{t0}^{(1)}$	On state threshold voltage	$T_j = 150\ ^\circ\text{C}$	Max.	0.85	
$R_D^{(1)}$	On state dynamic resistance	$T_j = 150\ ^\circ\text{C}$	Max.	5.5	m Ω
I_{DRM} , I_{RRM}	$V_D = V_{DRM} = V_R = V_{RRM} = 800\text{ V}$	$T_j = 25\ ^\circ\text{C}$	Max.	20	μA
		$T_j = 150\ ^\circ\text{C}$	Max.	2.5	mA

1. For both polarities of A2 referenced to A1

Table 4. Thermal parameters

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Junction to case (DC, max.)	0.25	$^\circ\text{C/W}$
$R_{th(j-a)}$	Junction to ambient (DC, typ., $S_{CU} = 2.1\text{ cm}^2$)	40	$^\circ\text{C/W}$

1.1 Characteristics curves

Figure 1. Maximum average power dissipation versus average on-state current

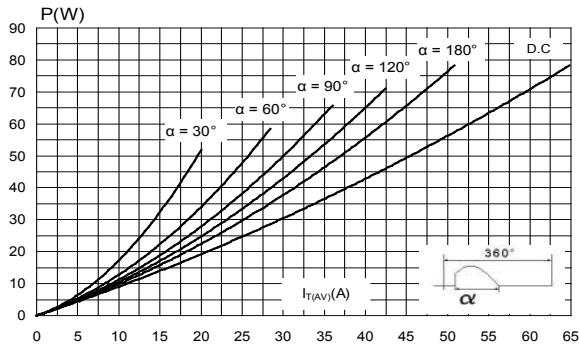


Figure 2. Average and DC on-state current versus case temperature

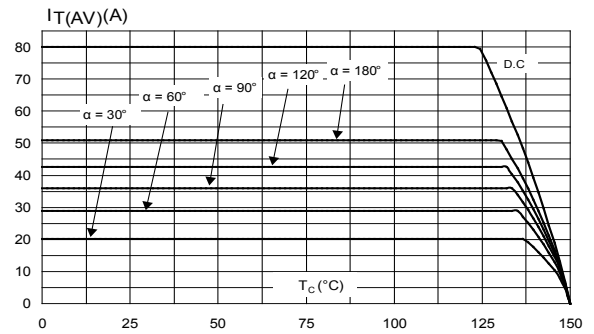


Figure 3. On-state characteristics (maximum values)

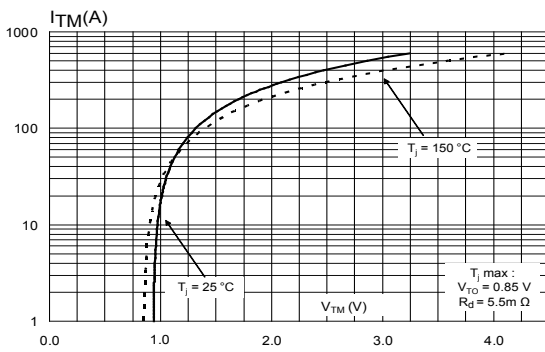


Figure 4. Average and DC on-state current versus ambient temperature

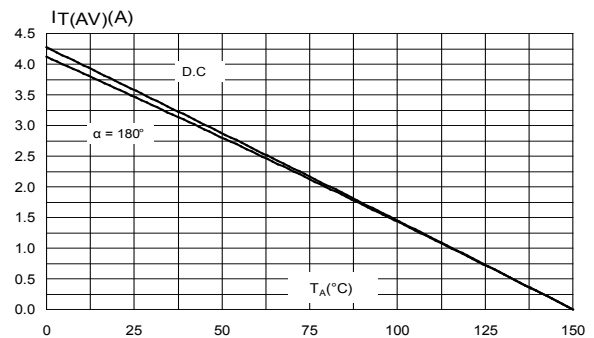


Figure 5. Relative variation of thermal impedance versus pulse duration

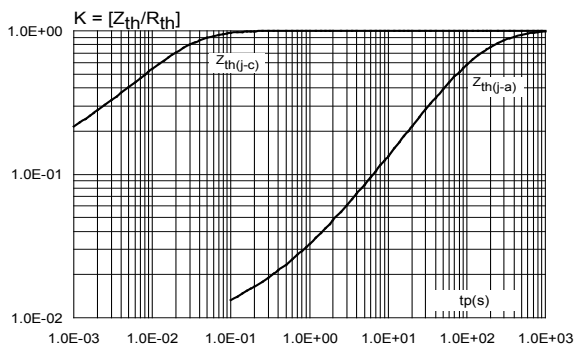


Figure 6. Thermal resistance junction to ambient versus copper surface under tab (D³PAK printed circuit board FR4, copper thickness: 35 μm)

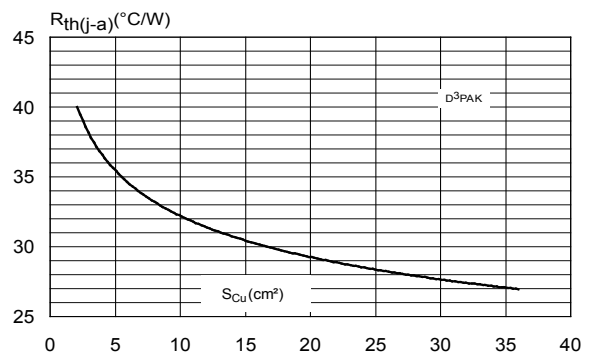


Figure 7. Surge peak on-state current versus number of cycles

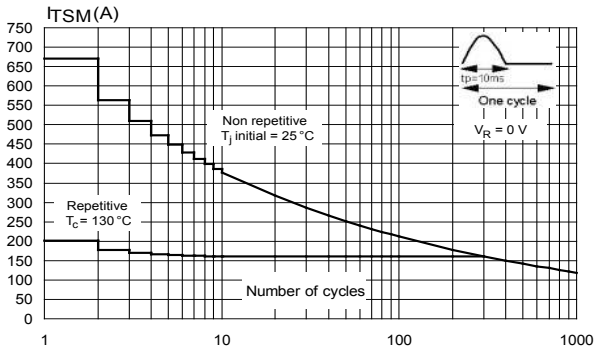


Figure 8. Non repetitive surge peak on-state current for a half cycle sine pulse versus pulse width ($t_p < 10$ ms)

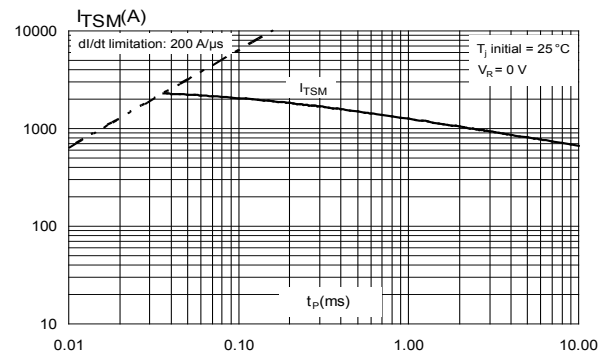


Figure 9. Relative variation of holding current and latching current versus junction temperature (typical values)

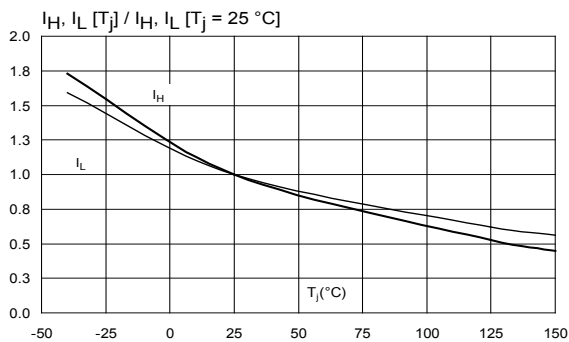


Figure 10. Relative variation of gate trigger current and gate voltage versus junction temperature

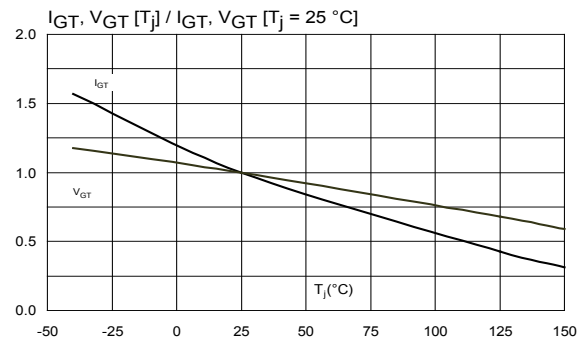


Figure 11. Relative variation of leakage current versus junction temperature for different values of blocking voltage

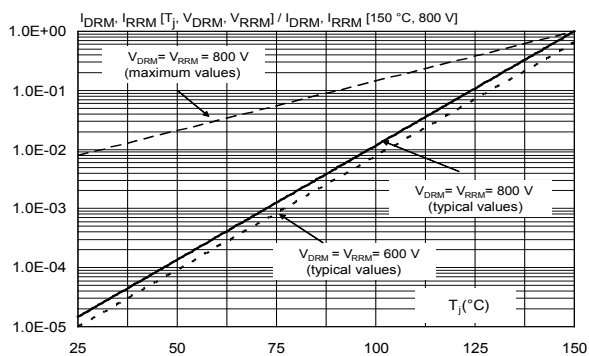
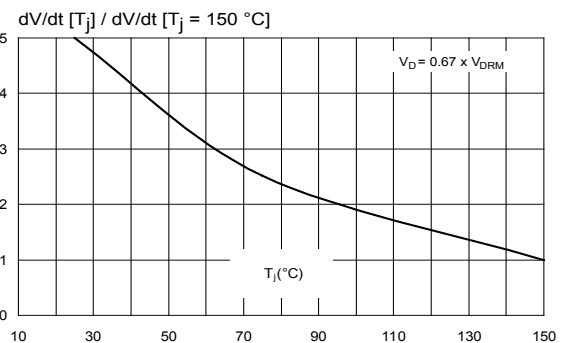


Figure 12. Relative variation of static dV/dt immunity versus junction temperature (typical values)



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 D³PAK package information

- Epoxy meets UL 94,V0
- Lead-free package leads, halogen-free molding resin
- Pre-conditioning moisture sensitivity MSL 1

Figure 13. D³PAK package dimension definitions

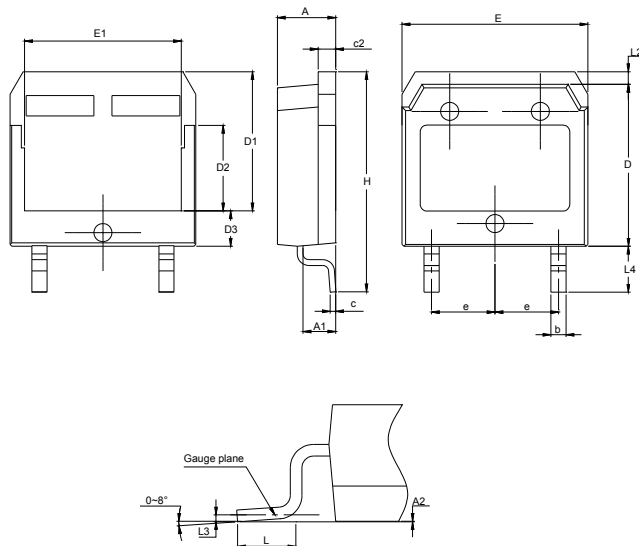
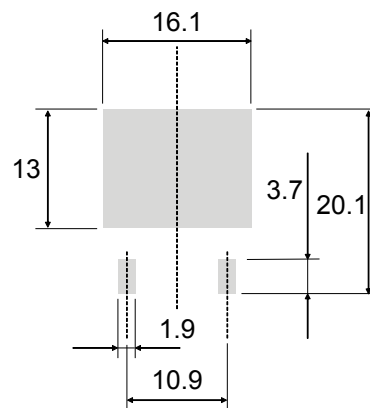


Table 5. D³PAK package mechanical data

Ref.	Dimensions					
	Millimeters			Inches (dimension in inches are given for reference only)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.90		5.10	0.1929		0.2008
A1	2.70		2.90	0.1063		0.1142
A2	0.02		0.25	0.0008		0.0098
b	1.15		1.45	0.0453		0.0571
c	0.40		0.65	0.0157		0.0256
c2	1.45		1.61	0.0571		0.0634
D	13.80		14.00	0.5433		0.5512
D1	11.80		12.10	0.4646		0.4764
D2	7.50		7.80	0.2953		0.3071
D3	2.90		3.20	0.1142		0.1260
E	15.85		16.05	0.6240		0.6319
E1	13.30		13.60	0.5236		0.5354
e		5.45			0.2146	
H	18.70		19.10	0.7362		0.7520
L	1.70		2.00	0.0669		0.0789
L2	1.00		1.15	0.0394		0.0453
L3		0.25			0.0098	
L4	3.80		4.10	0.1496		0.1614

Figure 14. Minimum footprint (dimensions in mm)



Revision history

Table 7. Document revision history

Date	Revision	Changes
11-Feb-2016	1	Initial release.
01-Apr-2016	2	Updated Table 3: "Electrical characteristics ($T_j = 25\text{ °C}$ unless otherwise specified)".
02-May-2016	3	Updated Thermal parameters.
30-Jul-2019	4	Updated Table 1 , Figure 8 and Figure 9 . Minor text change.

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