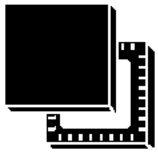
ST25R3910

Mid-range HF reader with 0.7 W supporting AAT

Datasheet - production data



QFN32

Features

- Close loop adjustment of ASK modulation for accurate control of modulation depth in case of ISO-14443B protocol
- Low power (3.5 µA) NFC target mode
- AM/PM demodulator
- Accurate RF envelope measurement (8-bit A/D converter)
- High output power at 3.3 V power supply:
  - Up to 700 mW in case regulator is externally shorted
  - Up to 500 mW in case of differential output when antenna trimming is used
  - Up to 125 mW in case of single ended output when antenna trimming is used
- Squelch for gain reduction, to compensate for noise generated by tag processing
- Automatic Antenna tuning (AAT)
- Transparent mode
- Amplitude and phase measurement
- Supporting 13.56 MHz and 27.12 MHz quartz oscillator with fast start-up
- Supply voltage range from 2.4 to 3.6 V
- Wide temperature range: -40 ºC to 85 ºC
- Package: 32-pin QFN (5x5mm)

Description

The ST25R3910 is a high performance 13.56 MHz RFID reader, with two differential, low impedance (1.5 Ohm) antenna drivers.

These drivers are unmatched, allowing the ST25R3910 to deliver up to eight times the output power of a standard HF reader IC using the same power supply voltage, and reducing in half the power consumption at the same output power.

The ST25R3910 can operate already at 2.4 V, with a low power operating mode of 5 mA, making it perfectly suited for portable or battery-powered applications.

For applications where high power is required the ST25R3910 can deliver up to 700 mW, thus avoiding the need for complex external booster circuitry.

The component count and complexity of the design is further reduced through automatic modulation depth adjustment.

The analog front end (AFE) is complemented by a highly integrated data framing engine for both ISO-14443 A and B. This includes data rates up to 848 kbit/s, with all framing and synchronization tasks on board. This enables to build a complete HF RFID reader using only a low end MCU.

The ST25R3910 supports reader to tag and Peer to Peer communication using the NFCIP-1 active communication mode with a 106 kbps data rate. Other standard and custom protocols, such as ISO-15693 or FeliCa™ can be implemented via transparent mode. The ST25R3910 features a SPI, which enables bi-directional communication with the external microcontroller.

The ST25R3910 also features the Automatic Antenna Tuning (AAT) technology, enabling the reader to re tune itself to deliver maximum output at 13.56 MHz, when the surroundings detune the antenna.

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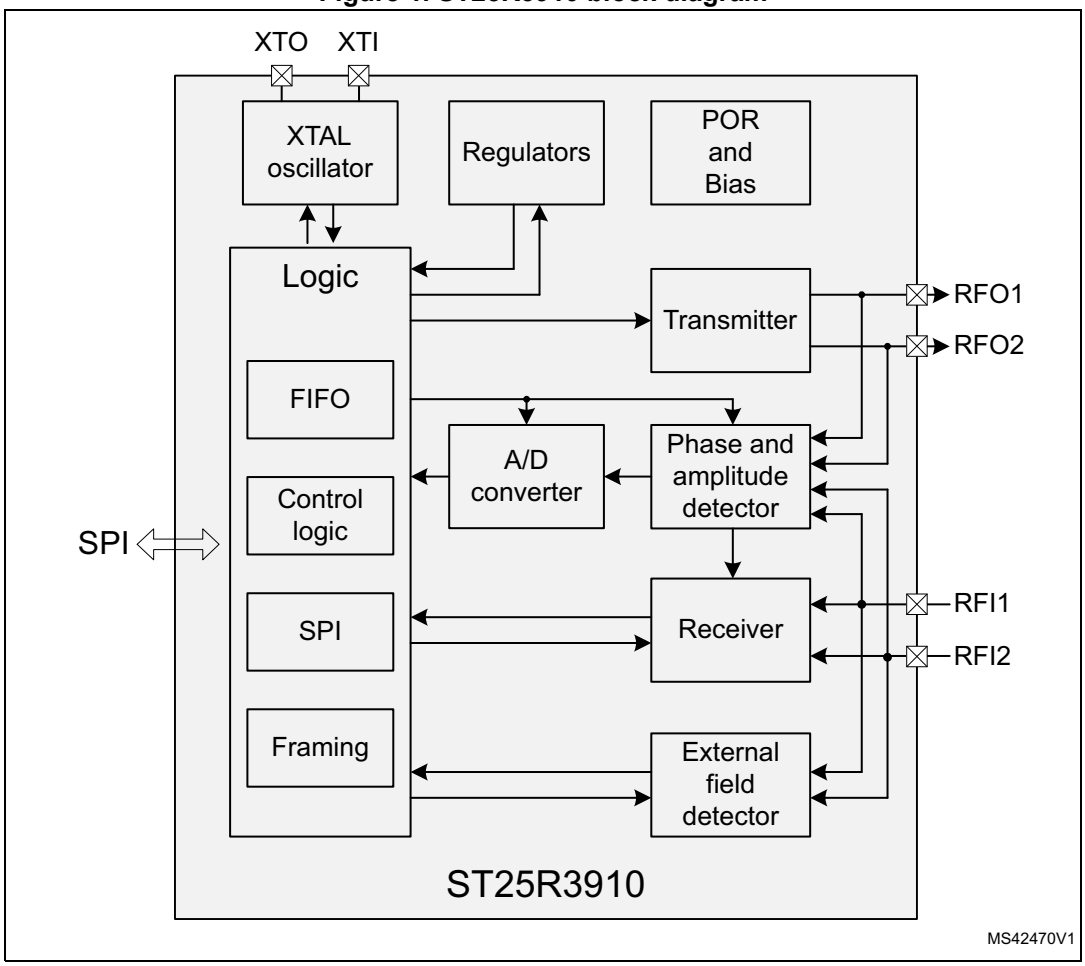
1 Functional overview

The ST25R3910 is suitable for applications where the reader antenna is directly driven (no 50 Ω cable). Several unique features make it especially suitable for low power and battery powered applications.

1.1 Block diagram

The block diagram is shown in *Figure 1*.

Figure 1. ST25R3910 block diagram



1.1.1 Transmitter

The transmitter incorporates drivers that drive external antenna through pins RFO1 and RFO2. Single sided and differential driving is possible. The transmitter block additionally contains a sub-block that modulates transmitted signal (OOK or configurable AM modulation).

The ST25R3910 transmitter is intended to directly drive antennas (without 50 Ω cable, usually antenna is on the same PCB). Operation with 50 Ω cable is also possible, but in that case some of the advanced features are not available.

1.1.2 Receiver

The receiver detects tag modulation superimposed on the 13.56 MHz carrier signal. The receiver contains two receive chains (one for AM and another for PM demodulation) composed of a peak detector followed by two gain and filtering stages and a final digitizer stage. The filter characteristics are adjusted to optimize performance for each mode and bit rate (sub-carrier frequencies from 212 kHz to 848 kHz are supported). The receiver chain inputs are the RFI1 and RFI2 pins. The receiver chain incorporates several features that enable reliable operation in challenging phase and noise conditions.

1.1.3 Phase and amplitude detector

The phase detector is observing the phase difference between the transmitter output signals (RFO1 and RFO2) and the receiver input signals (RFI1 and RFI2). The amplitude detector is observing the amplitude of the receiver input signals (RFI1 and RFI2) via self-mixing. The amplitude of the receiver input signals (RFI1 and RFI2) is directly proportional to the amplitude of the antenna LC tank signal.

The phase detector and the amplitude detector can be used for the following purposes:

- PM demodulation, by observing RFI1 and RFI2 phase variation
- Average phase difference between RFOx pins and RFIx pins is used to check and optimize antenna tuning and inductive wakeup via the MCU
- Amplitude of signal present on RFI1 and RFI2 pins is used to check and optimize antenna tuning

1.1.4 A/D converter

The ST25R3910 contains a built in Analog to Digital (A/D) converter. Its input can be multiplexed from different sources and is used in several applications (measurement of RF amplitude and phase, calibration of modulation depth…). The result of the A/D conversion is stored in a register and can be read via SPI.

1.1.5 External field detector

The External field detector is a low power block switched on in NFCIP target mode to detect the presence of the initiator field, and also used during the NFCIP Collision Avoidance procedure.

1.1.6 Quartz crystal oscillator

The quartz crystal oscillator can operate with 13.56 MHz and 27.12 MHz crystals. At start-up the transconductance of the oscillator is increased to achieve a fast start-up. The start-up time varies with crystal type, temperature and other parameters, hence the oscillator amplitude is observed and an interrupt is sent when stable oscillator operation is reached.

The oscillator block also provides a clock signal to the external microcontroller (MCU_CLK), according to the settings in the control register.

1.1.7 Power supply regulators

Integrated power supply regulators ensure a high power supply rejection ratio for the complete reader system. If the reader system PSRR has to be improved, the command Adjust Regulators is sent. As a result of this command, the power supply level of V_{DD} is measured in maximum load conditions and the regulated voltage reference is set 250 mV below this measured level to assure a stable regulated supply. The resulting regulated voltage is stored in a register. It is also possible to define regulated voltage by writing a configuration register. To decouple any noise sources from different parts of the IC there are three regulators integrated with separated external blocking capacitors (the regulated voltage of all of them is the same). One regulator is for the analog blocks,the other is for the antenna drivers. Logic and digital I/O pads are supplied directly from V_{DD} (negative supply pin for logic and digital I/O is separated to avoid coupling of logic induced noise in the substrate).

This block additionally generates a reference voltage for the analog processing (AGD - analog ground). This voltage also has an associated external buffer capacitor.

1.1.8 POR and Bias

This block provides the bias current and the reference voltages to all other blocks. It also incorporates a Power on Reset (POR) circuit that provides a reset at power-up and at low supply voltage levels.

1.1.9 ISO-14443 and NFCIP-1 framing

This block performs framing for receive and transmit according to the selected ISO mode and bit rate settings.

In reception it takes the demodulated sub-carrier signal from the receiver. It recognizes the SOF, EOF and data bits, performs parity and CRC check, organizes the received data in bytes and places them in the FIFO.

During transmit, it operates inversely, it takes bytes from the FIFO, generates parity and CRC bits, adds SOF and EOF and performs final encoding before passing the modulation signal to the transmitter.

In Transparent mode, the framing and FIFO are bypassed, the digitized sub-carrier signal (the receiver output), is directly sent to the SDATAO pin, and the signal applied to the SDATAI pin is directly used to modulate the transmitter.

1.1.10 FIFO

The ST25R3910 contains a 32-byte FIFO. Depending on the mode, it contains either data that has been received or data to be transmitted.

1.1.11 Control logic

The control logic contains I/O registers that define operation of device.

1.1.12 SPI

A 4-wire Serial Peripheral Interface (SPI) is used for communication between the external microcontroller and the ST25R3910.

1.2 Application information

The minimum configurations required to operate the ST25R3910 are shown in *Figure 2* and *Figure 3*.

Figure 2. Minimum configuration with single sided antenna driving (including EMC filter)

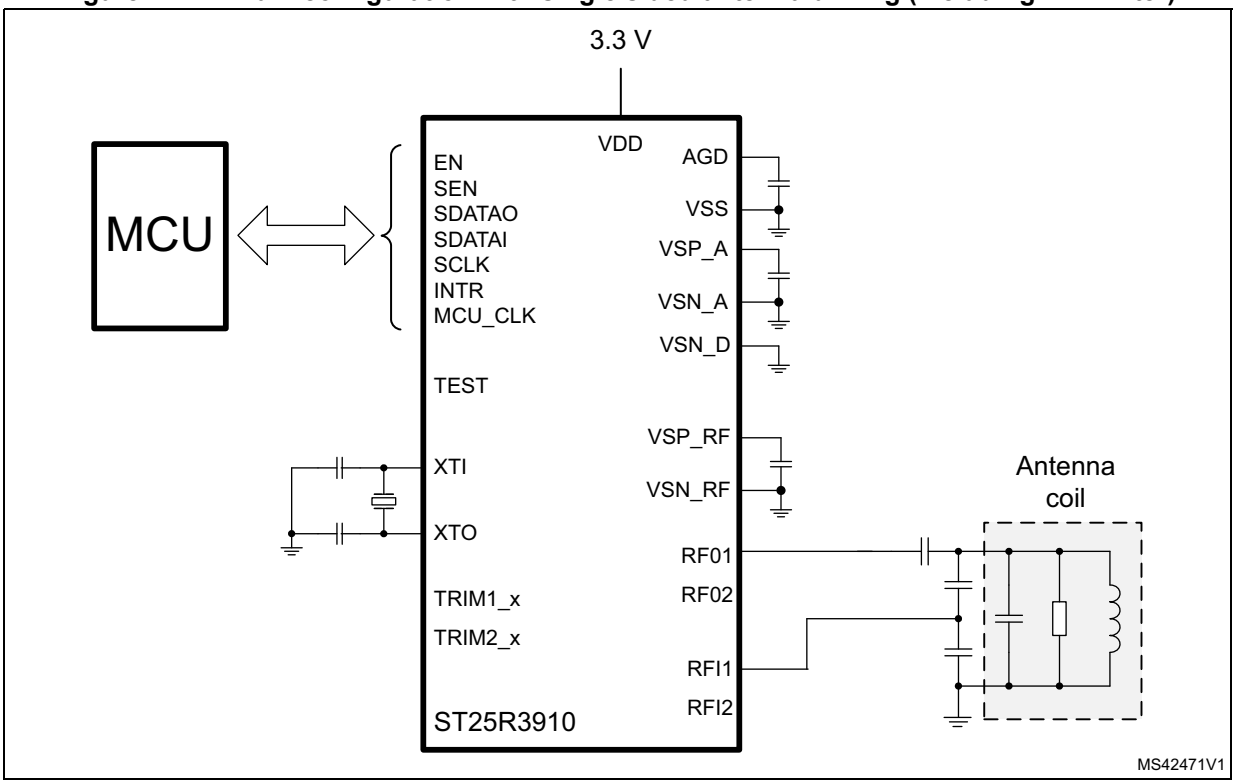
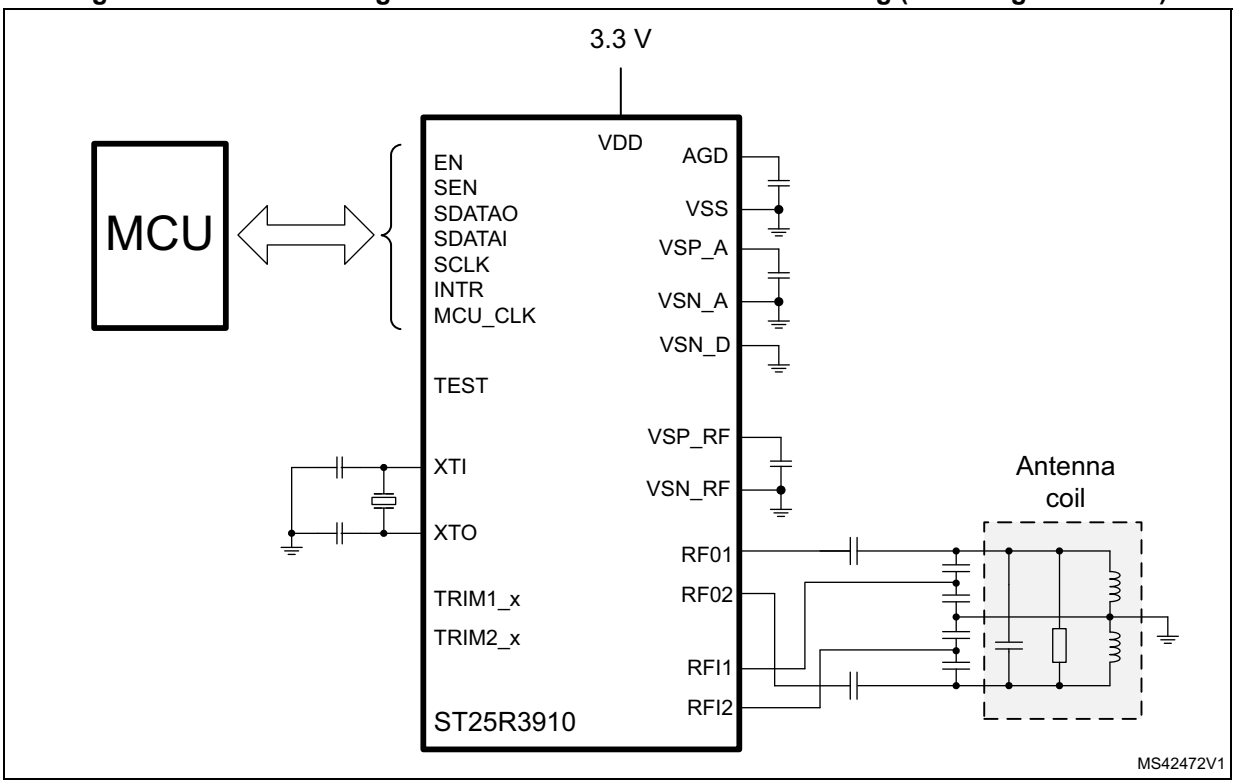


Figure 3. Minimum configuration with differential antenna driving (including EMC filter)



1.2.1 Operating modes

The ST25R3910 operating mode is defined by the contents of the *Operation Control Register*.

At power-up all bits of the *Operation Control Register* are set to 0, the ST25R3910 is in Power-down mode. In this mode AFE static power consumption is minimized, only the POR and part of the bias are active, while the regulators are transparent and are not operating. The SPI is still functional in this mode so all settings of ISO mode definition and configuration registers can be done.

Control bit en (bit 7 of the *Operation Control Register*) is controlling the quartz crystal oscillator and regulators. When this bit is set, the device enters in Ready mode. In this mode the quartz crystal oscillator and regulators are enabled. An interrupt is sent to inform the microcontroller when the oscillator frequency is stable.

Enable of receiver and transmitter are separated so it is possible to operate one without switching on the other (control bits rx_en and tx_en). In some cases this may be useful, if the reader field has to be maintained and there is no tag response expected, the receiver can be switched-off to save current. Another example is the NFCIP-1 active communication receive mode in which the RF field is generated by the initiator and only the receiver operates.

The receiver also has a Low power mode in which its power consumption (and then its sensitivity) is reduced. This mode is entered in by setting control bit rx_lp.

The last control bit of the *Operation Control Register* is nfc_t bit. Setting of this bit is only allowed in case the NFC mode is set in the ISO mode definition register. Setting this bit to one, while all other bits are set to 0, puts the ST25R3910 into Initial NFC Target mode. In

this low power mode, only the Target Activation Detector, which will detect a presence of external RF field, is active. Once the presence of external RF field is detected, an interrupt is sent to the microcontroller, which will in turn switch on the oscillator and the receiver.

1.2.2 Transmitter

The transmitter contains two identical push-pull driver blocks connected to the pins RFO1 and RFO2. Each driver is composed of eight segments having binary weighted output resistance. The MSB segment typical ON resistance is 3 Ω, when all segments are turned on; the output resistance is typically 1.5 Ω. All segments are turned on to define the normal transmission (non-modulated) level. It is also possible to switch off certain segments when driving the non-modulated level to reduce the amplitude of the signal on the antenna and/or to reduce the antenna Q factor without making any hardware changes.

AM modulation and operation of the driver segments is controlled by writing AM modulation depth and antenna driver registers. *Antenna Driver Non-Modulated Level Definition Register* defines which segments will be used to define normal, non-modulated level. *Modulation Depth Definition Register* and *Antenna Driver AM Modulated Level Definition Register* are used to define how the AM modulated level is set-up. It can be set-up automatically by definition of modulation depth and the direct command Calibrate Modulation Depth or by a direct definition of segments which are turned off during AM modulation.

1.2.3 Receiver

The receiver performs demodulation of the tag sub-carrier modulation that is superimposed on the 13.56 MHz carrier frequency. It performs AM and/or PM demodulation, amplification, band-pass filtering and digitalization of sub-carrier signals (848, 424 and 212 kHz subcarrier frequencies are supported). Additionally it performs RSSI measurement, automatic gain control (AGC) and Squelch.

The receiver is switched on when *Operation Control Register* bit rx_en is set. The operation of the receiver is additionally controlled by the signal rx_on, set high when modulated signal is expected on the receiver input. This is automatically done after every Transmit command. Signal rx_on can be also forced high by sending direct command Unmask Receive Data. Signal rx_on is used to control features like RSSI and AGC.

AM demodulation is performed using a peak follower. Both the positive and negative peaks are tracked to suppress common mode signal. In case external demodulation is carried out the peak follower stage can be bypassed by setting bit envi in *Configuration Register 2*. In case of PM demodulation signal coming from the phase detector is replacing the output of peak follower.

Next stage in signal processing is the buffer amplifier followed by second order low pass filter with adjustable corner frequency. Final stage is a first order high pass filter with adjustable corner frequency. The digital signal representing tag subcarrier modulation is produced by a window comparator.

Filter setting is done automatically when ISO mode and data rate are chosen by writing *ISO Mode Definition Register*. Setting is displayed in the *Receiver Configuration Register* and can be changed by rewriting this register. In Transparent mode the *ISO Mode Definition Register* is not used and Filter selection has to be done by writing *Receiver Configuration Register*. By setting the *Operation Control Register* bit rx_lp receiver operates in Low power mode. In this mode, power consumption is lower but receiver sensitivity is reduced (see *Section 3: Electrical characteristics on page 58*).

Gain reduction, AGC and Squelch

The total gain of receiver chain is 160. In certain conditions it is desirable to reduce this gain. There are several features implemented in the Receiver to reduce this gain.

Automatic Gain Reduction (AGC)

The automatic gain control feature is useful in case the tag is close to the reader. In such conditions the receiver chain is in saturation and demodulation can be influenced by system noise and saturation of last gain stage. When AGC is switched on receiver gain is reduced so that the input to digitizer stage is not saturated. The AGC system comprises a window comparator with a window three times larger than the one of the digitalization window comparator. When the AGC function is enabled the gain is reduced until there are no transitions on its output. Such procedure ensures that the input to digitalization window comparator is less than three times larger than its window.

AGC operation is controlled by the *Receiver Configuration Register* bits agc_en and agc_m. Agc_en bit enables AGC operation, agc_m defines AGC operating mode. The AGC action is started 20 µs after the rising edge of signal rx_on. In case agc_m bit is 0 it will operate during a complete receive period, in case it is 1 it will operate on the first 8 subcarrier pulses. The AGC is reducing gain by 21 dB in 7 steps of 3 dB. When signal rx_on is low AGC is in reset.

Squelch

This feature is designed for operation of the receiver in noisy conditions. The noise can come from tags (caused by the processing of reader commands), or it can come from a noisy environment. This noise may be misinterpreted as start of tag response, resulting in decoding errors.

During execution of the Squelch procedure the output of the digitizing comparator is observed. In case there are more than two transitions on this output in a 50 µs time period, the receiver gain is reduced by 3 dB, and the output is observed during the next 50 µs. This procedure is repeated until the number of transitions in 50 µs is lower or equal to two, or until the maximum gain reduction is reached. This gain reduction can be cleared sending the direct command Clear Squelch.

During execution of the direct command Squelch the digital output of receiver (output of window comparator mentioned above) is observed. In case there are more than two transitions on this output in 50 µs time period, the gain is reduced by 3 dB and output is observed during next 50 µs. This procedure is repeated until the number of transitions in 50 µs is lower or equal to two, or until the maximum gain reduction (21 dB) is reached. This setting is cleared with direct command Clear Squelch.

Setting gain reduction

By setting bits rg2 to rg0 in *Receiver Configuration Register* receiver gain can also be reduced in seven steps of 3 dB.

Actual gain reduction is combination of all three gain reduction features mentioned above (AGC, Squelch and setting gain reduction in *Receiver Configuration Register*). Actual gain reduction state can also be observed by reading the *Receiver State Display Register* bits gr_2 to gr_0.

RSSI

The receiver also performs the RSSI (Received Signal Strength Indicator) measurement of the modulated signal that is superimposed on the 13.56 MHz carrier. The RSSI measurement is started after the rising edge of rx_on. It stays active as long as signal rx_on is high, it is frozen while rx_on is low. The RSSI is a peak hold system, and the value can only increase from the initial zero value. Every time the AGC reduces the gain the RSSI measurement is reset and starts from zero. Result of RSSI measurements is a 4-bit value that can be observed by reading the *Receiver State Display Register*. The LSB step is 2.15 dB.

Since the RSSI measurement is of peak hold type the RSSI measurement result does not follow any variations in the signal strength (the highest value will be kept). In order to follow RSSI variations it is possible to reset the RSSI bits and restart the measurement by sending the direct command Clear RSSI.

1.2.4 A/D converter

The ST25R3910 contains an 8-bit successive approximation A/D converter. Inputs to the A/D converter can be multiplexed from different sources to be used in several direct commands and adjustment procedures. The result of the last A/D conversion is stored in the *A/D Output Register*.

The A/D converter has two operating modes, absolute and relative.

- In absolute mode the low reference is 0 V and the high reference is 2 V. This means that A/D converter input range is from 0 to 2 V, 00h code means input is 0 V or lower, FFh means that input is 2 V - 1 LSB or higher (LSB is 7.8125 mV).
- In relative mode low reference is 1/6 of V_{SP_A} and high reference is 5/6 of V_{SP_A}, so the input range is from 1/6 to 5/6 V_{SP_A}.

Relative mode is only used in phase measurement (phase detector output is proportional to power supply). In all other cases absolute mode is used.

The A/D converter input can also be accessed externally. When the direct command AD Convert is sent, an A/D conversion of voltage present on pin AD_IN is performed in absolute mode, result is stored in *A/D Output Register*. AD_IN pin should be left non-connected in case A/D conversion is not needed in application.

1.2.5 Phase and amplitude detector

Phase detector

The phase detector is observing phase difference between the transmitter output signals (RFO1 and RFO2) and the receiver input signals RFI1 and RFI2, which are proportional to the signal on the antenna LC tank. These signals are first elaborated by digitizing comparators, then digitized signals are processed by a phase detector. Filter characteristics of the phase antenna are adapted to one of the two possible operation modes. For antenna tuning check, a strong low power filter is used to get average phase difference, for PM demodulation a low pass filter having 1 MHz corner frequency is used to pass the subcarrier frequency.

The phase detector output is inversely proportional to the phase difference between the two inputs. The 90° phase shift (ideal antenna LC tank tuning) results in $V_{SP}/2$ output voltage.

If the antenna LC tank is detuned, phase shift changes, resulting in a different phase detector output voltage. In case of command Check Antenna Resonance phase detector output is applied to A/ D converter in relative mode. Output of phase detector is also observed by comparator with reference signal $V_{SP}/2$. Output of this comparator is used in execution of direct command Calibrate Antenna.

The phase detector has low pass characteristics in case of PM demodulation. This is to enable phase demodulation of the 848 kHz subcarrier signal. The output is then fed to the Receiver.

Amplitude detector

Signals from pins RFI1 and RFI2 are used as inputs to the self-mixing stage. The output of this stage is a DC voltage proportional to amplitude of signal on pins RFI1 and RFI2. This signal is fed to the A/D converter when amplitude of signal on RFI inputs has to be measured (direct commands Measure RF and Calibrate Modulation Depth).

1.2.6 External field detector

The External Field Detector is used in NFC mode to detect the presence of an RF field. It is composed of two sub-blocks, Target Activation Detector and a RF Collision Avoidance Detector. Input to both blocks is the signal from the RFI1 pad. The thresholds of the two blocks can be independently set by writing the *NFCIP Field Detection Threshold Register*. The outputs of both detectors are fed to a logic OR gate, whose output is fed to the Control logic. A low to high transition of this logic or gate output triggers an interrupt (Interrupt due to NFC event).

Target Activation Detector

This block is turned on in NFC target mode to detect the presence of an interrogator field. It is enabled by setting the *Operation Control Register* bit nfc_t. It is a low power block with an adjustable threshold in the range from 145mVpp and 590mVpp. This block generates an interrupt when an external field is detected and also when it disappears. With such implementation it can also be used to detect the moment when the external field disappears. This is useful to detect the moment when external NFC device (it can either an interrogator or a target) has stopped emitting an RF field since a response can only be sent afterwards. Actual state of the Target Activation Detector can be checked by reading the bit rfp in the *Receiver State Display Register*. When this bit is set to logic one, there is a signal higher than the threshold present on the input of Target Activation Detector.

RF Collision Avoidance Detector

This block is activated during the RF Collision Avoidance sequence which is executed before every request or response in NFC active communication (Initial or Response RF Collision Avoidance). In case during the RF Collision Avoidance sequence the presence of an external field is detected, request/response is not sent, an interrupt is generated to inform the external controller about collision. During RF Collision Avoidance, the Target Activation Detector is disabled in order to have the correct threshold when detection is made. The threshold of the RF Collision Avoidance Detector can be adjusted in the range from 50 to 1080 mVpp.

1.2.7 Quartz crystal oscillator

The quartz crystal oscillator can operate with 13.56 and 27.12 MHz crystals. The oscillator is based on an inverter stage supplied by controlled current source. A feedback loop is controlling the bias current in order to regulate amplitude on XTI pin to 1 V_{pp}. This feedback ensures reliable operation even in case of low quality crystals, with R_s up to 50 Ω. To enable a fast reader start-up an interrupt is sent when the oscillator amplitude exceeds 750 mV_{pp}. The oscillator block always provides 13.56 MHz clock signal to the rest of the IC. In case of 27.12 MHz crystal clock signal is internally divided by two. Divider is controlled by *Configuration Register 2* bit osc. Division by two ensures that the 13.56 MHz signal has a duty cycle of 50%, which is better for the Transmitter performance (no PW distortion). Use of 27.12 MHz crystal is therefore recommended.

In case of 13.56 MHz crystal, the bias current of stage which is digitizing oscillator signal is increased to minimize the PW distortion. The oscillator output is also used to drive a clock signal output pin, which can be used by the external microcontroller (MCU_CLK). By setting *Configuration Register 2* the frequency can be chosen between 13.56, 6.78 and 3.39 MHz. Any microcontroller processing generates noise, which may be captured by the ST25R3910 receiver. Using MCU_CLK as the microcontroller clock source generates noise synchronous with the reader carrier frequency that is filtered out by the receiver, while using some other incoherent clock source produces noise which may generate some sideband signals captured by Receiver. It is then recommended to use MCU_CLK as microcontroller clock source.

1.2.8 Power supply, Regulators

The ST25R3910 includes two regulators that can be adjusted automatically to improve the reader PSRR. VDD is an external power supply pin, used to supply the logic and digital pins. One regulator is used to supply analog blocks (V_{SP_A}), another is reserved for the transmitter (V_{SP_RF}) in order to decouple transmitter current spikes from the rest of the IC. All negative power supply pins are externally connected to the same negative supply, the reason for separation is the need to decouple noise induced by voltage drops on the internal power supply lines. These pins are VSS (die substrate potential), VSN_D (negative supply of logic and digital pads), VSN_A (negative supply of analog blocks) and VSN_RF (negative supply of transmitter).

An additional regulator block provides AGD voltage (1.5 V), which is used as reference potential for analog processing (analog ground). Blocking capacitors have to be connected externally to regulator outputs and AGD pins. For pins VSP_A and VSP_RF recommended blocking capacitors are 2.2 µF in parallel with 10 nF, for pin AGD 1 µF in parallel with 10 nF is suggested.

The regulated voltage ranges from 2.4 to 3.4 V, with 100 mV step. Both regulators are set to the same voltage. V_{SP_A} regulator maximum capability is 20 mA while maximum capability of V_{SP_RF} regulator is 300 mA. V_{SP_RF} regulator also has a built-in protection limiting current to 300 mA in normal operation and to 500 mA in case of a short. The regulators are operating when either the *Operation Control Register* bit en is set or pin EN is high.

In Power-down mode the regulators are not operating, V_{SP_A} and V_{SP_RF} are connected to V_{DD} through 1 kΩ resistors, to ensure smooth power-up of the system and a smooth transitions from Stand-by mode to other operating modes. In case regulators were regulating or were transparent at power-up a large current would be pulled from V_{DD} supply to charge blocking capacitors of regulated outputs, a problematic situation for battery powered systems.

At power-up the regulated voltage is set to its maximum, i.e. 3.4 V.

The regulator voltage can then be set automatically or “manually”. The automatic procedure is started by sending the direct command Adjust Regulators. In this procedure regulated voltage is set 250 mV below V_{DD}. This procedure ensures that reader operates with maximum possible power while still achieving a good PSRR.

Regulator operation can be controlled and observed by writing and reading two Regulator registers. *Regulator Display Register* is a read only register that displays actual regulated voltage when regulator is operating. In Power-down mode its content is forced to 00.

By writing *Regulated Voltage Definition Register* the user chooses between automatic and “manual” adjustment of regulated voltage. Automatic mode is chosen when bit reg_s is 0 (default and also recommended state). When bit reg_s is asserted to 1 regulated voltage is defined by bits rege_3 to rege_0 of the same register.

1.2.9 Communication with an external microcontroller

The ST25R3910 is a slave devices and the external microcontroller initiates all communication. Communication is performed by a 4-wire Serial Peripheral Interface (SPI). The ST25R3910 sends an interrupt request (pin INTR) to the microcontroller, which can use clock signal available on pin MCU_CLK when the oscillator is running. The microcontroller can also drive pin EN. Putting this pin high has the same function as setting the *Operation Control Register* bit en (entry in Ready mode).

Serial Peripheral Interface (SPI)

While signal SEN is low the SPI interface is in reset, while it is high the SPI is enabled. It is recommended to keep SEN low whenever the SPI is not in use. SDATAI is sampled at the falling edge of SCLK. All communication is done in blocks of 8 bits (bytes). First two bits of first byte transmitted after low to high transition of SEN define SPI operation mode.

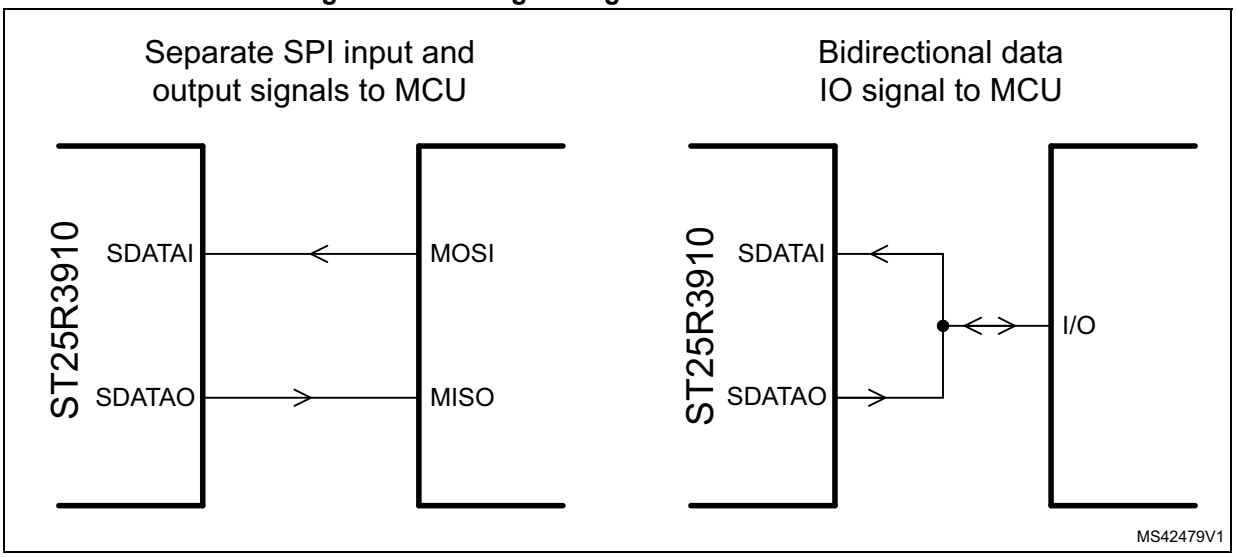
Table 1. Serial data interface (4-wire interface) signal lines

Name	Signal	Signal level	Description
SEN	Digital input	CMOS	SPI Enable (active low)
SDATAI	Digital input		Serial data input
SDATAO	Digital output with tristate		Serial data output
SCLK	Digital input		Clock for serial communication

MSB bit is always transmitted first (valid for address and data).

Read and Write modes support address auto-incrementing. This means that if some additional data bytes are sent/read after the address and first data byte, they are written to/read from addresses incremented by ‘1’. *Figure 4* defines possible modes.

Figure 4. Exchange of signals with microcontroller



When signal SEN is low, the SPI interface is in reset and SDATAO is in tristate; when it is high, SPI interface is enabled. It is recommended to keep signal SEN low whenever the SPI interface is not in use. SDATAI is sampled at the falling edge of SCLK. All communication is done in blocks of 8 bits (bytes). The first two bits of the first byte transmitted after low to high transition of SEN define the SPI operation mode. *Table 2* defines the possible modes.

Table 2. SPI operation patterns

Mode	Mode pattern (communication bits)								Mode related data							
	Mode		Register address						Register data							
	M1	M0	C5	C4	C3	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Write	0	0	A5	A4	A3	A2	A1	A0	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
Read	0	1	A5	A4	A3	A2	A1	A0	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
FIFO load	1	0	0	0	0	0	0	0	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
FIFO read	1	0	1	1	1	1	1	1	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
Command	1	1	C5	C4	C3	C2	C1	C0	-	-	-	-	-	-	-	-

Writing data to addressable registers (Write mode)

Figure 5 and *Figure 6* show cases of writing a single byte and writing multiple bytes with auto-incrementing address. SDATAI is sampled at the falling edge of SCLK. A SEN low pulse indicates the end of the Write command after register has been written. Auto incrementing address is supported, this means that if after the address and first data byte some additional data bytes are sent, they are written to addresses incremented by 1. If the command is terminated by putting SEN low before a packet of 8 bits composing one byte is sent, writing of this register is not performed. In case the register on the defined address does not exist or it is a read only register, no write is performed.

Figure 5. SPI communication: writing a single byte

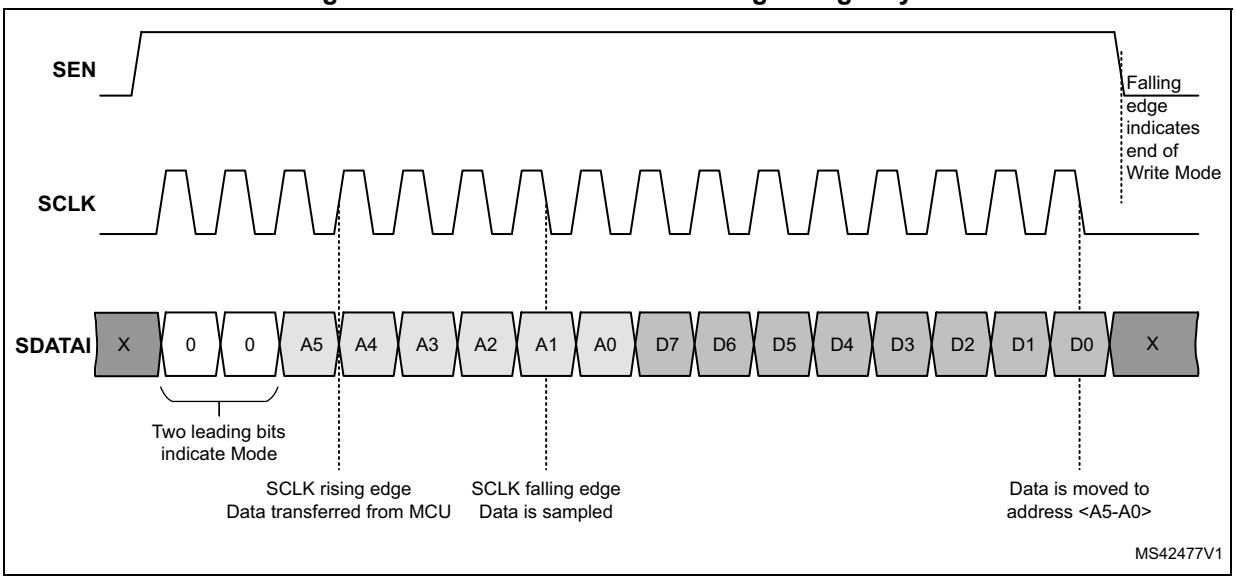
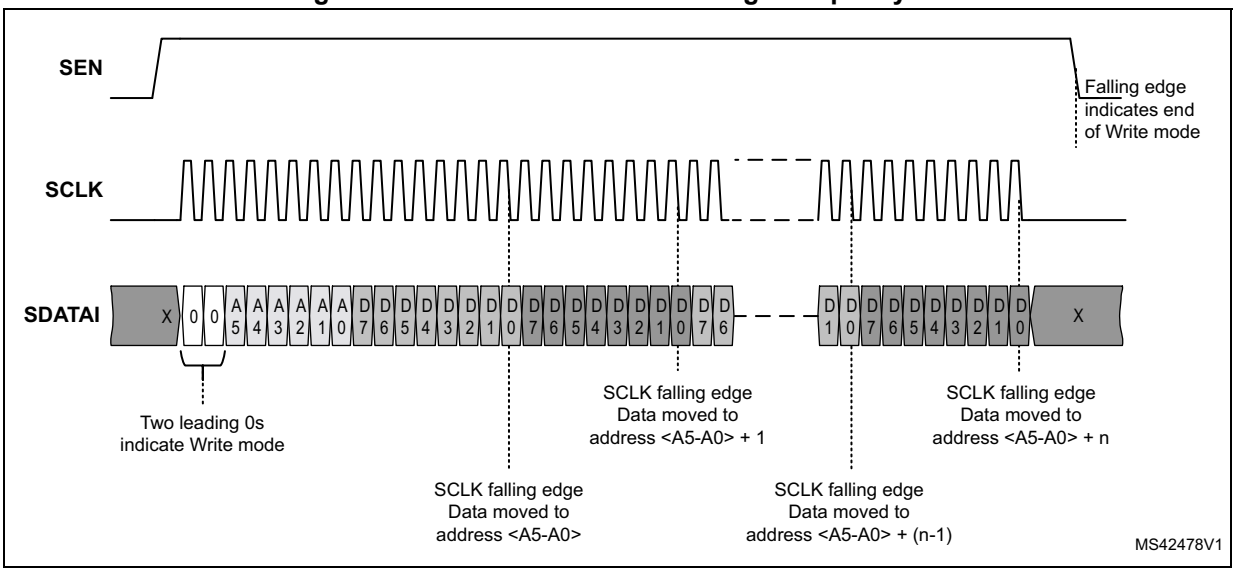


Figure 6. SPI communication: writing multiple bytes



Reading data from addressable registers (Read mode)

The command control byte for a read command consists of a command code and an address. After the command code, the address of register to be read has to be provided from the MSB to the LSB. Then one or more data bytes can be transferred from the SPI slave to the master, always from the MSB to the LSB. As in case of write, the read command supports auto-incrementing address. To transfer bytes from consecutive addresses, SPI master has to keep the SEN signal high and the SCLK has to be active as long as data need to be read from the slave.

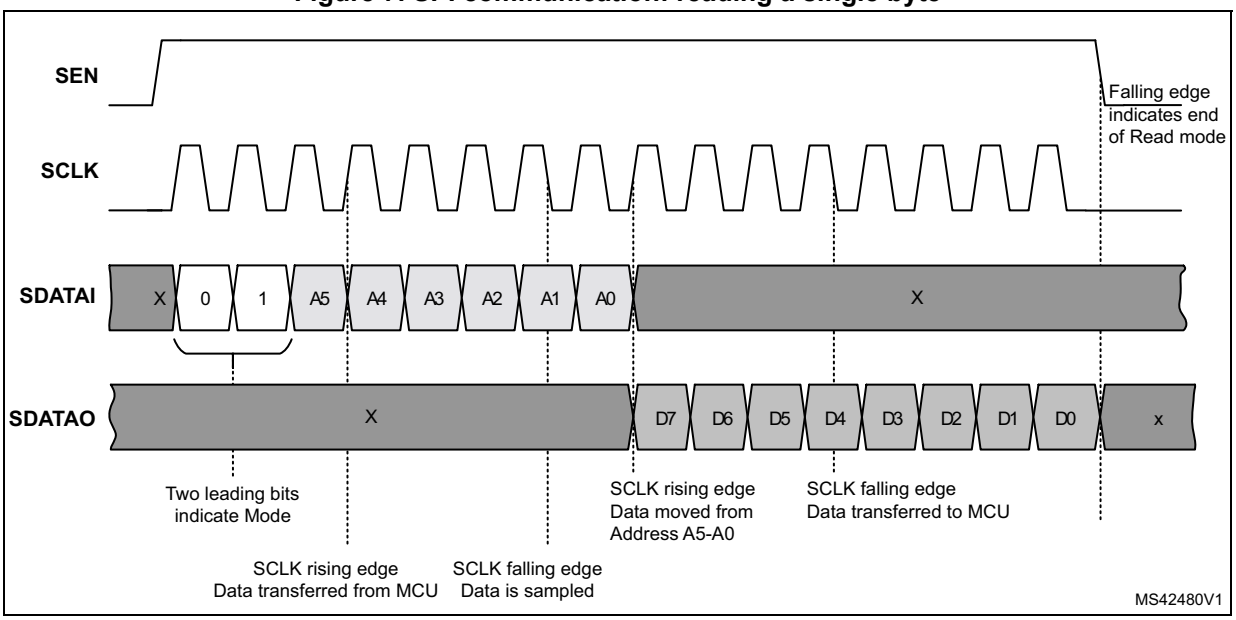
SDATAI is sampled at the falling edge of SCLK, data to be read from the ST25R3910 internal register is driven to SDATAO pin on rising edge of SCLK and is sampled by the MCU at the falling edge of SCLK.

A SEN low pulse has to be sent after register data has been transferred in order to indicate the end of the Read command and to prepare the Interface to the next command control byte.

In case the register on defined address does not exist all 0 data is sent to SDATAO.

Figure 7 is an example for reading of single byte.

Figure 7. SPI communication: reading a single byte

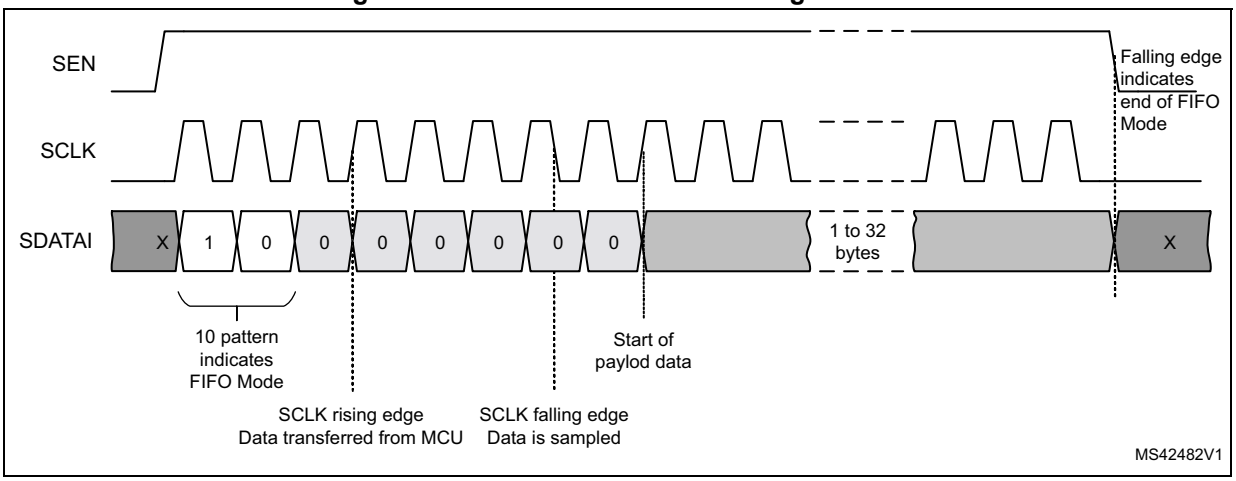


Loading transmitting data into FIFO

Loading the transmitting data into the FIFO is similar to writing data into an addressable registers. Difference is that in case of loading more bytes all bytes go to the FIFO. SPI operation mode bits 10 indicate FIFO operations. In case of loading transmitting data into FIFO all bits <C5 – C0> are set to 0. Then a bit-stream, the data to be sent (1 to 32 bytes), can be transferred. In case the command is terminated by putting SEN low before a packet of 8 bits (one byte) is sent, writing of that particular byte in FIFO is not performed.

Figure 8 shows how to load the Transmitting Data into the FIFO.

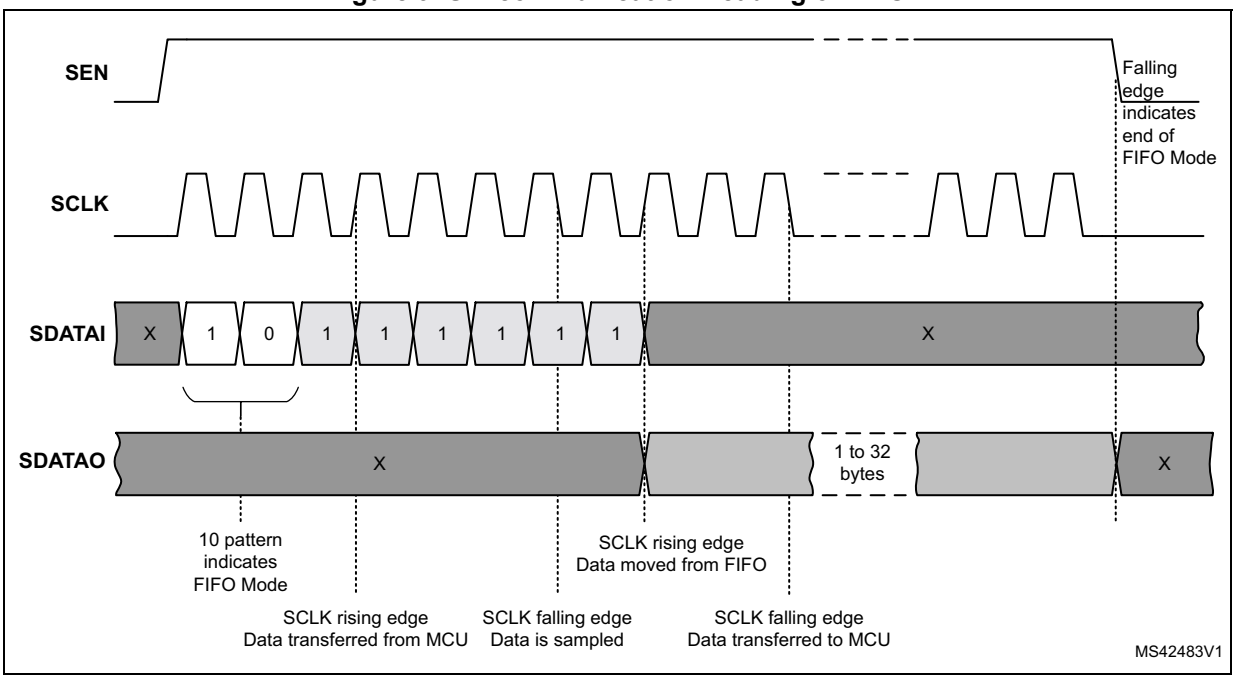
Figure 8. SPI communication: loading of FIFO



Reading received data from FIFO

Reading received data from the FIFO is similar to reading data from an addressable registers. Difference is that in case of reading more bytes they all come from the FIFO. SPI operation mode bits 10 indicate FIFO operations. In case of reading the received data from the FIFO all bits <C5 – C0> are set to 1. On the following SCLK rising edges the data from FIFO appears as in case of read data from addressable registers. If the command is terminated by putting SEN low before a packet of 8 bits (one byte) is read, that particular byte is considered unread and will be the first one read in next FIFO read operation.

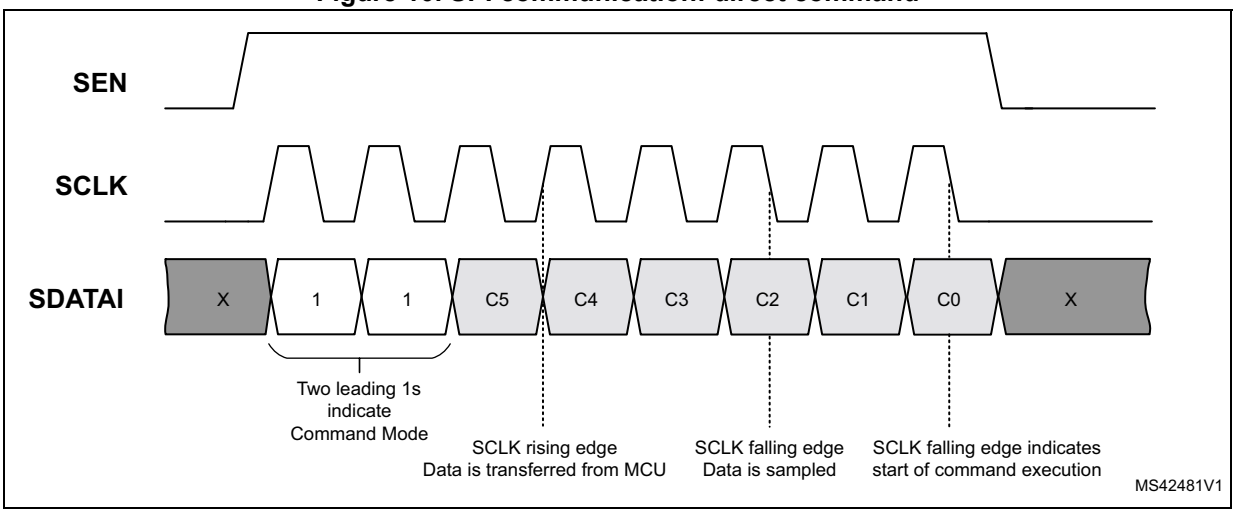
Figure 9. SPI communication: reading of FIFO



Direct Command Mode

Direct Command Mode has no arguments, so a single byte is sent. SPI operation mode bits 11 indicate Direct Command Mode. The following six bits define command code, sent MSB to LSB. The command is executed on falling edge of last clock (see *Figure 10*).

Figure 10. SPI communication: direct command



Interrupt interface

When an interrupt condition is met the source of interrupt bit is set in the *Interrupt Register* and the INTR pin transitions to high.

Table 3. INTR output

Name	Signal	Signal level	Description
INTR	Digital output	CMOS	Interrupt output pin

The microcontroller then reads the *Interrupt Register* to distinguish between different interrupt sources. After the *Interrupt Register* is read its content is reset to 0 and INTR pin signal transitions to low.

Note: There may be more than one interrupt bit set in case the microcontroller does not immediately read the Interrupt Register after the INTR signal has been set and another event causing interrupt has occurred.

If an interrupt from a certain source is not required, it can be disabled by setting corresponding bit in the *Mask Interrupt Register*. When masking a given interrupt source the interrupt is not produced, but the source of interrupt bit is still set in *Interrupt Register*.

After reading the *Interrupt Register* the 13.56 MHz clock coming from the oscillator is used to produce a reset signal that clears it and resets INTR signal. Practically in all interrupt cases the oscillator is running when an interrupt is produced. The only exception is the interrupt in the Initial NFC Target mode where only the Target Activation Detector is operating. In this case the interrupt is cleared with first SCLK rising edge following reading of the *Interrupt Register* (an extra dummy CLK pulse during reading of the *Interrupt Register* or the first SCLK pulse of the next SPI command will do the job).

FIFO water level and FIFO status registers

The ST25R3910 contains a 32 byte FIFO. In case of transmitting the Control logic shifts the data that was previously loaded by the external microcontroller to the Framing Block and further to the transmitter. During reception, the demodulated data is stored in the FIFO and the external microcontroller can download received data at a later moment.

Transmit and receive capabilities of the ST25R3910 are not limited by the FIFO size due to a FIFO water level interrupt system. During transmission an interrupt is sent (*INTR* due to FIFO water level in the *Interrupt Register*) when the content of data in the FIFO still to be sent is lower than the FIFO water level for receive. The external microcontroller can now add more data in the FIFO. The same stands for the reception: when the number of received bytes exceeds the FIFO water level for receive an interrupt is sent to inform the external controller that data has to be downloaded from FIFO.

The external controller has to serve the FIFO faster than data is transmitted or received. Using SCLK frequency that is at least double than the actual receive or transmit bit rate is recommended.

There are two settings of the FIFO water level available for receive and transmit in the *Configuration Register 5*.

After data are received the external microcontroller needs to know how long the received data string was before downloading data from the FIFO: This information is available in the *FIFO Status Register*, which displays number of bytes in the FIFO that were not read out.

The *FIFO Status Register* also contains a FIFO overflow bit, set when during reception the external processor did not react on time and more than 32 bytes were written in FIFO (the received data are lost in this case).

1.2.10 Direct commands

Table 4. Direct commands

Code	Command	Comments
000001	Set default	Puts the ST25R3910 in default state (same as after power-up)
000010	Clear	Stops all activities and clears FIFO
000100	Transmit with CRC	Starts a transmit sequence using automatic CRC generation
000101	Transmit without CRC	Starts a transmit sequence without automatic CRC generation
000110	Transmit REQA	Transmits REQA command (ISO-14443A mode only
000111	Transmit WUPA	Transmits WUPA command (ISO-14443A mode only)
001000	NFC transmit with Initial RF Collision Avoidance	Equivalent to Transmit with CRC with additional RF Collision Avoidance
001001	NFC transmit with Response RF Collision Avoidance	
001010	NFC transmit with Response RF Collision Avoidance with n=0	
010000	Mask receive data	Receive after this command is ignored

Table 4. Direct commands (continued)

Code	Command	Comments
010001	Unmask receive data	Received data following this command are normally processed (this command has priority over internal mask receive timer)
010010	AD convert	A/D conversion of signal on AD_IN pin is performed, result is stored in *A/D Output Register*
010011	Measure RF	RF amplitude is measured, result is stored in *A/D Output Register*
010100	Squelch	Performs gain reduction based on the current noise level.
010101	Clear Squelch	Resumes gain settings in place before sending Squelch command
010110	Adjust regulators	Adjusts supply regulators according to the current supply voltage level
010111	Calibrate modulation depth	Starts sequence which activates the TX, measures the modulation depth and adapts it to comply with the specified modulation depth
011000	Calibrate antenna	Starts the sequence to adjust parallel capacitances connected to TRIMx_y pins so that the antenna LC is in resonance.
011001	Check antenna resonance	Measurement of antenna LC tank resonance to determine whether calibration is needed.
011010	Clear RSSI	Clears RSSI bits and restarts the measurement
011100	Transparent mode	Enters in Transparent mode

Set Default

This direct command puts the ST25R3910 in the same state as power-up initialization. All registers are initialized to the default state.

Note: Results of different calibration and adjust commands are also lost.

This direct command is accepted in all operating modes.

Clear

This direct command stops all current activities (transmission or reception) and clears FIFO. It also clears collision and interrupt registers. This command has to be sent first in a sequence preparing a transmission (except in case of direct commands Transmit REQA and Transmit WUPA).

Transmit commands

All Transmit commands (Transmit With CRC, Transmit Without CRC, Transmit REQA and Transmit WUPA) are accepted only in case the transmitter is enabled (bit tx_en is set).

NFC transmit commands

The NFC transmit commands (NFC transmit with Initial RF Collision Avoidance, NFC transmit with Response RF Collision Avoidance, NFC transmit with Response RF Collision Avoidance with n=0) are used to transmit requests and responses in the NFC mode. Before actual transmission the RF Collision avoidance with Collision avoidance threshold defined in the *NFCIP Field Detection Threshold Register* is performed.

In the command NFC transmit with Response RF Collision Avoidance n is randomly set in a range from 0 to 3, while in the command NFC transmit with Response RF Collision Avoidance with n=0 it is set to 0. In case collision is detected during the RF Collision Avoidance the transmission is not done and an interrupt is sent with flag INTR due to NFC event.

The NFC transmit commands switch on and off the transmission block, setting the *Operation Control Register* bit tx_en in the NFC mode is not allowed.

Timing of the NFC transmit commands (see *Table 5*) is according to the ISO/IEC 18092 standard, which specifies a range for some of them.

Table 5. NFC P2P timings implemented in ST25R3910

Symbol	Parameter	Value	Unit	Comments
T_{IDT}	Initial delay time	302	µs	Initial RF Collision Avoidance
T_{RWF}	RF waiting time	37.76		-
T_{IRFG}	Initial guard time	5.11	ms	Initial RF Collision Avoidance
T_{ADT}	Active delay time	151	µs	Response RF Collision Avoidance
T_{ARFG}	Active guard time	84		
T_{GAS}	Guard time after sending response or request	65		Time during which RF field stays switched on after sending a response or a request. Not specified in the ISO/IEC 18092.

An interrupt due to end of transmission is sent when RF field is switched off.

All NFC Transmit commands are only authorized in case the ISO mode configuration bit nfc is set and the oscillator and regulators are running.

Mask Receive Data and Unmask Receive Data

After the direct command Mask Receive Data the signal rx_on that enables the RSSI and AGC operation of the receiver (see *Section 1.1.2: Receiver*) is forced to low, processing of the receiver output by the receive data framing block is disabled. This command is useful to mask receiver and receive framing from processing the data when there is actually no input and only a noise would be processed..

The direct command Unmask Receive Data is enabling normal processing of the received data (signal rx_on is set high to enable the RSSI and AGC operation), the receive data framing block is enabled. A common use of this command is to enable again the receiver operation after it was masked by the command Mask Receive Data.

The command Unmask Receive Data has to be used in the NFC target mode. The sequence implemented in the ST25R3910 supposes that every action is started with a transmit command, after sending the transmit data, the receive mode is automatically entered to process the response. Such a sequence is always in place in case of the

ISO-14443 reader mode and in the NFCIP mode, where the ST25R3910 is the initiator. In case of NFC target mode this sequence is started by receiving the interrogator request. After the interrupt caused by the first initiator request command Unmask Receive Data is sent to force the ST25R3910 in receive mode.

The commands Mask Receive Data and Unmask Receive Data are only accepted when the receiver is enabled (bit rx_en is set).

AD Convert

A/D conversion of signal on AD_IN pin is performed; result is stored in *A/D Output Register* (see *Section 1.1.4 on page 8*).

Duration time: 42 µs max.

This command is accepted in any mode where the oscillator and regulators are running.

Measure RF

This command measures the amplitude on the RFI inputs and stores result in the *A/D Output Register* (see also *Section 1.1.4 on page 8* and *Section 1.1.3 on page 8*).

When this command is executed the output of the Amplitude detector is multiplexed to the A/D converter input (the A/D converter is in absolute mode). The Amplitude Detector conversion gain is 0.6 V_{inpp}/V_{out}. One LSB of the A/D converter output represents 13.02 mV_{pp} on the RFI inputs, a 3 V_{pp} signal (the maximum allowed level on each of the two RFI inputs) results in 1.8 V output DC voltage and produces the value 1110 0110 on the A/D converter output.

Duration time: 42 µs max.

This command is accepted in any mode where the oscillator and regulators are running.

Squelch

This direct command is intended to avoid demodulation problems of tags that produce a lot of noise during data processing. It can also be used in a noisy environment. The operation of this command is explained in *Squelch*.

Duration time: 500 µs max.

This command is only accepted when the transmitter and the receiver are operating.

Clear Squelch

Clears the gain reduction that was set by sending Squelch command.

This command is accepted in any mode.

Adjust Regulators

When this command is sent the power supply level of V_{DD} is measured in maximum load conditions and the regulated voltage reference is set 250 mV below this measured level to ensure maximum possible stable regulated supply (see *Section 1.2.8: Power supply, Regulators*). The use of this command increases the system PSSR.

At the beginning of execution of the command, both the receiver and transmitter are switched on to have the maximum current consumption, and the regulators are set to their maximum regulated voltage (5.1 V in case of 5 V supply and 3.4 V in case of 3.3 V supply). After 300 µs V_{SP_RF} is compared to V_{DD}, if is not at least 250 mV lower the regulator setting

is reduced by one step (120 mV in case of 5 V supply and 100 mV in case of 3.3 V supply) and measurement is done after another 300 µs. The procedure is repeated until V_{SP_RF} drops at least 250 mV below V_{DD}, or until the minimum regulated voltage (3.9 V in case of 5 V supply and 2.4 V in case of 3.3 V supply) is reached.

Duration time: 5 ms max.

This command is accepted in any mode where the oscillator and regulators are running.

This command is not accepted when the external definition of the regulated voltage is selected in the *Regulated Voltage Definition Register* (bit reg_s is set to H).

Calibrate Modulation Depth

Starts a sequence that activates the transmission, measures the modulation depth and adapts it to comply with the modulation depth specified in the *Modulation Depth Definition Register*. The result of the calibration procedure is stored in the *Modulation Depth Display Register*. Refer to *Section 1.2.14: AM modulation depth: definition and calibration* for details about setting the AM modulation depth and running this command.

Duration time: 10 ms max.

This command is accepted in any mode where the oscillator and regulators are running.

Calibrate Antenna

Sending this command starts a sequence that adjusts the parallel capacitances connected to TRIMx_y pins so that the antenna LC tank is in resonance. See *Section 1.2.15: Antenna tuning* for details.

Duration time: 400 µs max.

This command is accepted in any mode where the oscillator and regulators are running.

Check Antenna Resonance

This command measures the antenna LC tank resonance to determine whether a calibration is needed. See *Check Antenna Resonance* for details.

Duration time: 42µs max.

This command is accepted in any mode where the oscillator and regulators are running.

Clear RSSI

The receiver automatically clears the RSSI bits in the *Receiver State Display Register* and starts to measure the RSSI of the received signal when the signal rx_on is asserted. Since the RSSI bits store peak value (peak-hold type) the variations of the receiver input signal will not be followed (this may happen in case of long messages or test procedures). The direct command Clear RSSI clears the RSSI bits in the *Receiver State Display Register*, and the RSSI measurement is restarted (in case, of course, rx_on is still high).

Transparent Mode

Enters in the Transparent mode. The Transparent mode is entered on the falling edge of signal SEN and is maintained as long as signal SEN is kept low.

This command is accepted only when the Transmitter and the Receiver are operating.

1.2.11 Operating sequence

At power-up, the ST25R3910 enters the Power-down mode. The content of all registers is set to the default state.

1. The microcontroller, after a power-up, should load the *ISO Mode Definition Register* and the configuration registers to configure reader operation.
2. Configure the regulators. It is recommended to use direct command Adjust Regulators to improve the system PSRR.
3. When implementing the LC tank tuning, send the direct command Calibrate Antenna.
4. When using the AM modulation (ISO-14443B for example), set the modulation depth in the *AM Modulation Depth Control Register* and send the command Calibrate Modulation Depth.
5. The ST25R3910 is now ready to operate.

1.2.12 ISO-14443 reader operation

To begin with, the Ready mode has to be entered by setting the en bit of the *Operation Control Register* or by asserting pin EN. In this mode the oscillator is started and the regulators are enabled. When the oscillator operation is stable an interrupt is sent.

Before sending any command to a tag, the transmitter and receiver have to be enabled by setting the bits rx_en and tx_en.

If REQA or WUPA have to be sent, this is simply done by sending the appropriate direct command, otherwise the following sequence has to be followed:

1. Send the direct command Clear
2. Define the number of transmitted bytes in the *Number of Transmitted Bytes Register 0* and *Number of Transmitted Bytes Register 1*
3. Write the bytes to be transmitted in the FIFO
4. Send the direct command Transmit With CRC or Transmit Without CRC (whichever is appropriate)
5. When all the data is transmitted an interrupt is sent to inform the microcontroller that the transmission is finished (INTR due to end of transmission)

After the transmission is executed, the ST25R3910 receiver automatically starts to observe the RFI inputs to detect a tag response. The RSSI and AGC (when enabled) start. The framing block processes the sub-carrier signal from receiver and fills the FIFO with data. When the reception is finished and all the data is in the FIFO an interrupt is sent to the microcontroller (INTR due to end of receive), additionally the *FIFO Status Register* displays the number of bytes in the FIFO so that the microcontroller can proceed with data download.

In case of an error or bit collision detected during reception, an interrupt with appropriate flag is sent.

Transmit and Receive when the data packet is longer than FIFO

In case a data packet is longer than FIFO the sequence explained above is modified.

Before transmit the FIFO is filled. During transmit an interrupt is sent when remaining number of bytes is lower than the water level (IRQ due to FIFO water level). The microcontroller in turn adds more data in the FIFO. When all the data is transmitted an interrupt is sent to inform the microcontroller that transmission is finished.

During reception situation is similar. In case the FIFO is loaded with more data than the receive water level, an interrupt is sent and the microcontroller in turn reads the data from the FIFO.

When reception is finished an interrupt is sent to the microcontroller (INTR due to end of receive), additionally the *FIFO Status Register* displays the number of bytes in the FIFO that are still to be read out.

1.2.13 NFCIP-1 operation

The ST25R3910 supports only NFCIP-1 106 kbit/s active mode.

For operation in this mode, the bit nfc has to be set in the *ISO Mode Definition Register*. Next, the *NFCIP Field Detection Threshold Register* has to be written to define the thresholds for Target activation and RF Collision avoidance (see *Section 1.1.5: External field detector on page 8*).

Note: In the NFC mode the transmitter enable bit (tx_en) is never set in the Operation Control Register. The transmitter is activated automatically by the NFC transmit commands.

NFCIP target

The ST25R3910 enters in the Initial NFC Target mode by setting the nfc_t bit in the *Operation Control Register*. In this low power mode only the Target Activation Detector is running.

When presence of an external the RF field is detected an interrupt is sent (INTR due to NFC event). The microcontroller can now activate the oscillator, regulators and receiver. As explained in *Target Activation Detector*, the Target Activation Detector may also be used to detect the moment when initiator turns off its RF field. If the delay time after which the initiator turns off its field after sending its request is known, this feature is not needed and the Target Activation Detector can be turned off by setting bit nfc_t low after presence of the initiator field is detected.

At this point direct command Unmask Receive Data has to be sent to put the Receiver and control logic in the receive mode. The ST25R3910 is now ready to receive request from the initiator. Procedure during the reception is the same as in case of the ISO-14443 mode.

The target response is done in the same way as in case of the ISO-14443 transmission, only that the command which actually starts the transmission is either NFC transmit with Response RF Collision Avoidance or NFC transmit with Response RF Collision Avoidance with n=0. These two commands perform the RF Collision avoidance procedure before actually starting the transmission. In case an external RF field is detected during the RF Collision avoidance procedure an interrupt is sent (INTR due to NFC event) and the transmission is not performed.

At this point the ST25R3910 is waiting for a new request from the initiator.

In case the Target Activation Detector is still enabled an interrupt will be generated when the initiator switch on its field. This is additional information for the external controller, but it is not required by the receiver. The receiver is already running, reception will be done automatically and an interrupt will be sent when reception will be completed (or when the FIFO water level will be reached in case of a long request).

NFCIP initiator

If the ST25R3910 is an NFCIP initiator, the microcontroller activates the oscillator and the receiver, and prepares everything for transmitting as in case of the ISO-14443 transmission. The transmission is actually executed by direct command NFC Transmit with Initial RF Collision Avoidance.

The events that follow are the same as described in *NFCIP target*, with the difference that the roles of the initiator and target are interchanged.

The Target Activation Detector may also be used in case of the NFCIP initiator operation to detect the moment when the target RF field turns on and off.

1.2.14 AM modulation depth: definition and calibration

The AM modulation of the transmitted carrier is used for communication reader to tag in two configuration cases:

- ISO-14443B mode is configured in the *ISO Mode Definition Register*
- Transparent mode with AM modulation (direct command Transparent Mode, bit am of the *Configuration Register 5* is set to 1)

In other cases the OOK modulation is used.

The AM modulation depth can be automatically adjusted by setting the *Modulation Depth Definition Register* and sending the direct command Calibrate Modulation Depth. There is also an alternative possibility where the command Calibrate Modulation Depth is not used and the modulated level is defined by writing the *Antenna Driver AM Modulated Level Definition Register*.

AM modulation depth definition using the direct command Calibrate Modulation Depth

Before sending the direct command Calibrate Modulation Depth the *Modulation Depth Definition Register* has to be configured in the following way:

- Bit 7 (am_s) has to be set to 0 to choose definition by the command Calibrate Modulation Depth
- Bits 6 to 1 (mod5 to mod0) define target AM modulation depth

Definition of modulation depth using bits mod5 to mod0

The RFID standard documents usually define the AM modulation level in form of the modulation index. The modulation index is defined as (a-b)/(a+b), where a and b are, respectively, the amplitude of the non-modulated carrier and of the modulated carrier.

The bits mod5 to mod0 are used to calculate the amplitude of the modulated level. The non-modulated level that was before measured by the A/D converter and stored in an 8 bit register is divided by a binary number in range from 1 to 1.98. Bits mod5 to mod0 define binary decimals of this number.

Example

In case of the modulation index 10% the modulated level amplitude is 1.2222 times lower than the non-modulated level.

1.2222 converted to binary and truncated to 6 decimals is 1.001110. So in order to define the modulation index 10% the bits mod5 to mod0 have to be set to 001110.

Table 6 shows setting of the mod bits for some often used modulation indexes.

Table 6. Setting mod bits

Modulation Index (%)	a/b (dec)	a/b (bin)	mod5 … mod0
8	1.1739	1.001011	001011
10	1.2222	1.001110	001110
14	1.3256	1.010100	010100
20	1.5000	1.100000	100000
30	1.8571	1.110111	110111
33	1.9843	1.111111	111111

Execution of direct command Calibrate Modulation Depth

The modulation level is adjusted by increasing the RFO1 and RFO2 driver output resistance. The RFO drivers are composed of 8 binary weighted segments. Usually all these segments are turned on to define the normal, non-modulated level, there is also a possibility to increase the output resistance of the non-modulated state by writing the *Antenna Driver Non-Modulated Level Definition Register*.

Before sending the direct command Calibrate Modulation Depth the oscillator and regulators have to be turned on. When the direct command Calibrate Modulation Depth is sent the following procedure is executed:

1. The transmitter is turned on, non-modulated level is established.
2. The amplitude of the non-modulated carrier level established on the inputs RFI1 and RFI2 is measured by the A/D converter and stored.
3. Based on the measurement of the non-modulated level and the target modulated level defined by the bits mod5 to mod0 the target modulated level is calculated.
4. The output driver control is taken over by an internal register with initial level defined in the *Antenna Driver Non-Modulated Level Definition Register*. Content of the internal register is incremented by 1 to increase the driver resistance and thereby reduce the carrier level. The reduced carrier level, in turn, is measured by the A/D converter and compared with the target modulation level.
5. The procedure from previous point is repeated as long as the measured level is higher than the target modulation level.
6. When the measured carrier level is equal to or lower than the target modulation level, the state of the internal register is copied into the *Modulation Depth Display Register*, whose content is used to define the AM modulated level.

Note: After the calibration procedure is finished, the content of the Antenna Driver Non-Modulated Level Definition Register should not be changed. Modifications of the content of this register will change the non-modulated amplitude and therefore the ratio between the modulated and non-modulated level.

Note: In case the calibration of antenna resonant frequency in used, the command Calibrate Antenna has to be run before AM modulation depth adjustment.

AM modulation depth definition using the Antenna Driver AM Modulated Level Definition Register

When bit 7 (am_s) of the *Modulation Depth Definition Register* is set to 1 the AM modulated level is controlled by writing the *Antenna Driver Non-Modulated Level Definition Register*. If the setting of the modulated level is already known it is not necessary to run the calibration procedure, the modulated level can be defined just by writing this register.

It is also possible to implement calibration procedure through an external controller using the *Antenna Driver Non-Modulated Level Definition Register* and the direct command Measure RF.

The procedure is the following:

1. Write the non-modulated level in the *Antenna Driver Non-Modulated Level Definition Register* (usually it is all 0 to have the lower possible output resistance).
2. Switch on the transmitter.
3. After the setting time, send the direct command Measure RF. Read result from the *A/D Output Register*.
4. Calculate the target modulated level from the target modulation index and result of the previous point.
5. In the following iterations content of the *Antenna Driver Non-Modulated Level Definition Register* is modified, the command Measure RF executed and the result compared with the target modulated level as long as the result is not equal (or as close as possible) to the target modulated level.
6. At the end the content of the *Antenna Driver Non-Modulated Level Definition Register* that results in the target modulated level is written in the *Antenna Driver AM Modulated Level Definition Register* while the *Antenna Driver Non-Modulated Level Definition Register* is restored with the non-modulated definition value.

1.2.15 Antenna tuning

The ST25R3910 integrates the blocks needed to check and to adjust the antenna LC tank resonance frequency.

The key block in the resonance frequency checking and adjustment is the *Phase detector*, which measures the phase shift between the Transmitter output signals (RFO1 and RFO2) and the inputs RFI1 and RFI2 (proportional to the voltage on the antenna LC tank). In case of perfect tuning there is a 90º phase shift between them.

Check Antenna Resonance

In case of the perfect 90º phase shift mentioned above, the Phase Detector output results in $V_{SP}/2$ output voltage. A phase shift of 1% of the carrier frequency period (3.6º) results in the output voltage change of 2% of V_{SP} (1% phase shift results in 60mV change at V_{SP} = 3 V).

During execution of the direct command Check Antenna Resonance the Phase Detector output is multiplexed on the input of A/ D converter which is set in relative mode. 1 LSB of the A/D conversion output represents 0.13% of carrier frequency period (0.468º). The result of A/D conversion is in case of the perfect tuning exactly in the middle of range (1000 0000 or 0111 1111).

Values higher than 1000 0000 mean that phase detector output voltage is higher than $V_{SP}/2$, which correspond to resonance frequency higher than target 13.56 MHz. In the

opposite case, when the resonance frequency is lower than target, the result of A/D conversion is lower than 0111 1111.

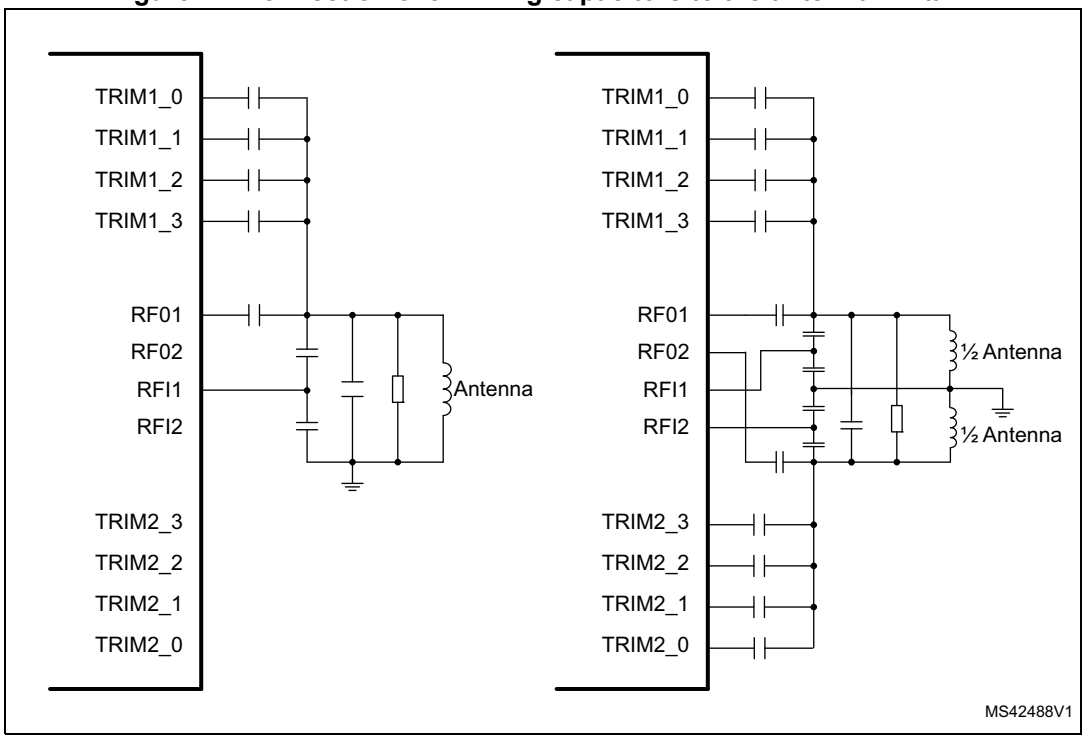
Execution of the command Check Antenna Resonance is fast and can be used frequently to check whether system settings are correct.

Calibrate Antenna Resonance

In order to implement the antenna LC tank calibration binary weighted trimming capacitors have to be connected between the two coil terminals to the pads TRIM1_3 to TRIM1_0 and TRIM2_3 to TRIM2_0. In case single driver is used only the pads TRIM1_3 to TRIM1_0 are used, pads TRIM2_3 to TRIM2_0 are left open.

Figure 11 shows connection of the trim capacitors for both single (left side) and differential (right side) driving. The TRIMx_y pads contain the HVNMOS switch transistors to V_{SS}. During trimming procedure the resonance frequency is adjusted by connecting some of the trimming capacitors to V_{SS} and leaving the other ones floating.

Figure 11. Connection of trimming capacitors to the antenna LC tank



The switches of the same binary weight are driven from the same source and are both on or off (the switches TRIM1_2 and TRIM2_2 are for example both either on of off). The breakdown voltage of the HVNMNOS switch transistors is 30 V, this limits the maximum peak to peak voltage on LC tank in case trimming is used. The on resistance of TRIM1_0 and TRIM2_0 switch transistors (to be connected to LSB trimming capacitor) is typically 50 Ω at V_{SP} = 3 V, the on resistance of other pads is binary weighted (the on resistance of TRIM1_3 and TRIM2_3 is 6.25 Ω).

Antenna calibration using command Calibrate Antenna

The calibration of LC tank resonance frequency is automatically done by running the direct command Calibrate Antenna. During execution of this command the comparator at the output of Phase Detector is used. In case the LC tank resonance frequency is higher than the target 13.56 MHz, the Phase Detector output gets higher than $V_{SP}/2$ and the comparator output is high. In the opposite case, when the resonance frequency is lower, the Phase Detector output gets lower than $V_{SP}/2$ and the comparator output is low.

At the beginning of the command Calibrate Antenna execution the switches in all TRIMx_y pads are turned off. As a consequence, all the trimming capacitors are disconnected so in case the LC tank dimensioning is correct the resonance frequency has to be higher than the target and the comparator output has to be high. In case the comparator output is low at this initial state the resonance frequency is too low even when all the trimming capacitor are disconnected, and adjustments of the resonance frequency are not possible. An error flag is set and execution of the command is terminated.

In case the comparator output was high at the initial state, the LSB switches (TRIM1_0 and TRIM2_0) are switched on and after 10 µs state of the comparator output is checked again. This procedure is repeated until the comparator output transitions to low, or until the final state with all switches turned on is reached. The switch state at which the comparator output is transitional is the one at which the LC tank is in resonance.

In case the state with all switched turned on is reached while the comparator output is still high, the resonance frequency is too high even when all the capacitors are connected and adjustments are not possible. The error flag is set.

The result of the direct command Calibrate Antenna can be observed by reading the *Antenna Calibration Register*, which displays the state of four bits representing the state of the switches when the resonance was reached and the error flag.

After the execution of the direct command Calibrate Antenna the resonance can be checked by running the direct command Check Antenna Resonance.

Antenna calibration using External Trim Register

There is also a possibility to control the position of the TRIM switches by writing the *External Trim Register*. When bit trim_s is set to 1 position of the trim switches is controlled by bits tre_3 to tre_0. Using this register and the direct command Check Antenna Resonance an external trimming procedure can be implemented.

Another possible external trimming procedure is to use this register and the direct command Measure RF. In this case the resonance is adjusted by looking for operating point with the maximum amplitude.

Transparent mode

The AS3909/10 framing supports the ISO-14443 standard.

Other standards as well as custom 13.56 MHz RFID reader protocols can be implemented by using the ST25R3910 AFE and framing implemented in the external microcontroller.

After sending the direct command Transparent Mode the external microcontroller directly controls the transmission modulator and gets the Receiver output (the control logic becomes “transparent”).

The Transparent mode is entered on falling edge of signal SEN after sending the command Transparent Mode and is maintained as long as the signal SEN is kept low. Before sending

the direct command Transparent Mode the Transmitter and Receiver have to be turned on, and the AFE has to be configured properly.

While the ST25R3910 is in the Transparent mode the AFE is controlled directly through the SPI interface:

- The Transmitter modulation is controlled by pin SDATAI (high is modulator on)
- Signal rx_on is controlled by pin SCLK (high enables RSSI and AGC)
- The Receiver output is sent to pin SDATAO

By controlling the rx_on advanced Receiver features like the RSSI and AGC can be used.

Configuration bits related to the ISO mode, framing and FIFO are meaningless in Transparent mode, but all other configuration bits are respected.

The transmitter modulation type used (OOK or AM) is defined by bit am of the *Configuration Register 5*.

The direct command Calibrate Modulation Depth supports modulation depths up to 30%, deeper AM modulation is possible by writing the *Antenna Driver AM Modulated Level Definition Register*.

The receiver filters support the subcarrier frequencies from 212 to 848 kHz. The filter characteristics can be configured via bits fs2 to fs0 in the *Receiver Configuration Register*.

Active receive – Use in ISO-14443B Anticollision

In some cases it is useful to know that a response from a tag is being received. This information is provided by bit rx_act in the *FIFO Status Register*. This bit is set to 1 when the start of the tag message is detected, and stays high until the end of reception.

This information can be used to speed up the ISO-14443B anticollision procedure when more slots are used. When there is no message in a certain slot, the reader does not have to wait for the time a complete ATQB takes before sending the next Slot-MARKER command, but it can send the next Slot-MARKER as soon as it is clear that there is no answer in that particular slot. The microcontroller can obtain this info by reading the rx_act flag at the time the receiver should already be processing the ATQB message. In case rx_act flag is set to one the receiver is processing a message and the microcontroller has to wait for the end of receive interrupt, in opposite case when the rx_act flag is set to zero there is no ATQB message in that particular slot and the next Slot-MARKER command can be sent immediately.

ISO-14443B, reduction of TR0 and TR1 and suppression of EOF/SOF in PICC response

The ISO-14443-3 standard, chapter 7.10.3 Coding of Param 1 defines possibility to reduce the TR0 and TR1 and suppress the EOF/SOF in PICC response.

Note: The ST25R3910 Receiver and Framing blocks do not support the reduction of TR0 and TR1 and suppression of EOF/SOF. If default settings of these parameters are changed, the framing block will not be able to decode the PICC response.

Test pins

Pins TEST and TIO are used to test the ST25R3910. Pin TEST is a digital pin with pull down, it is used to enter the test mode, pin TIO is used in test mode as a digital IO, in normal mode it is in tristate. It is recommended to connect pin TEST to V_{SS} and to leave pin TIO open.

1.3 Registers

The 6-bit register addresses below are defined in hexadecimal notation. The possible addresses range from 00h to 3Fh.

There are two types of registers implemented in the ST25R3910:

- configuration registers
- display registers

The configuration registers are used to configure the ST25R3910. They can be read and written (RW) through the SPI. The display registers are read only (R); they contain information about the ST25R3910 internal state.

Table 7. Registers map

Address (hex)	Main function	Content	Type
00	Main	*ISO Mode Definition Register*	RW
01		*Operation Control Register*	RW
02	Configuration	*Configuration Register 2*	RW
03		*Configuration Register 3 (ISO-14443A and NFC)*	RW
04		*Configuration Register 4 (ISO-14443B)*	RW
05		*Configuration Register 5*	RW
06		*Receiver Configuration Register*	RW
07	Interrupt and associated reporting	*Mask Interrupt Register*	RW
08		*Interrupt Register*	R
09		*FIFO Status Register*	R
0A		*Collision Register (ISO-14443A only)*	R
0B		*Number of Transmitted Bytes Register 0*	RW
0C		*Number of Transmitted Bytes Register 1*	RW
0D	ADC output	*A/D Output Register*	R
0E	Antenna calibration	*Antenna Calibration Register*	R
0F		*External Trim Register*	RW
10	AM modulation depth and Antenna driver	*Modulation Depth Definition Register*	RW
11		*Modulation Depth Display Register*	R
12		*Antenna Driver AM Modulated Level Definition Register*	RW
13		*Antenna Driver Non-Modulated Level Definition Register*	RW
14	NFCIP field detection	*NFCIP Field Detection Threshold Register*	RW
15	Regulators	*Regulator Display Register*	R
16		*Regulated Voltage Definition Register*	RW
17	Receiver state	*Receiver State Display Register*	R

1.3.1 ISO Mode Definition Register

Address: 00h

Type: RW

Table 8. ISO Mode Definition Register(1)

Bit	Name	Default	Function				Comments
7	nfc(2)	0	1: NFCIP-1 0: ISO-14443				Enables NFCIP-1, 106 kbps active communication mode
6	b_a	0	1: ISO-14443B 0: ISO-14443A				Applicable if nfc = 0
5	tx_rate2	0	**tx_rate2**	**tx_rate1**	**tx_rate0**	**Bit rate**	Select ISO-14443 data rate for transmit. Applicable if nfc = 0
4	tx_rate1	0	0	0	0	106 kbps	
3	tx_rate0	0	0	0	1	212 kbps	
			0	1	0	424 kbps	
			0	1	1	848 kbps	
			1	x	x	RFU	
2	rx_rate2	0	**rx_rate2**	**rx_rate1**	**rx_rate0**	**Bit rate**	Select ISO-14443 data rate for receive. Applicable if nfc = 0
1	rx_rate1	0	0	0	0	106 kbps	
0	rx_rate0	0	0	0	1	212 kbps	
			0	1	0	424 kbps	
			0	1	1	848 kbps	
			1	x	x	RFU	

1. Default setting takes place at power-up and after Set Default command.
2. If nfc=1, both transmit and receive data rates are set to 106 kbps independently from TX and RX setting.

1.3.2 Operation Control Register

Address: 01h

Type: RW

Table 9. Operation Control Register(1)

Bit	Name	Default	Function	Comments
7	en	0	1: Enables oscillator and regulator (Ready mode)	Internally OR-ed with the EN pin
6	rx_en	0	1: Enables Rx operation	-
5	rx_lp	0	1: Enables Low power receiver operation	Receive consumption is reduced
4	tx_en	0	1: Enables RF output	-
3	nfc_t	0	1: Enables Initial NFC target mode	When RF field is detected, interrupt is sent
2	-	-	Not used	-
1	-	-		-
0	-	-		-

1. Default setting takes place at power-up and after Set Default command.

Note: Receive low power operation reduces the input sensitivity in exchange for lower power consumption. If Rx consumption is reduced from 10 to 5 mA, 10 mA reader operation is possible.

1.3.3 Configuration Register 2

Address: 02h

Type: RW

Table 10. Configuration Register 2(1)

Bit	Name	Default	Function			Comments
7	sing	0	1: Only RFO1 driver will be used			Choose between single and differential antenna driving
6	envi	0	1: Input applied to RFI1 is envelope			RF envelope input
5	tf2	0	1: Reduces first stage gain by 11 dB			When both bits are set there is a 17 dB gain reduction
4	tf1	0	1: Reduces first stage gain by 6 dB			
3	osc	1	0: 13.56 MHz Xtal 1: 27.12 MHz Xtal			Selector for crystal oscillator
2	out_cl1	0	**out_cl1**	**out_cl0**	**MCU_CLK**	Selection of clock frequency on MCU_CLK output. In case of “11” MCU_CLK output is permanently low.
1	out_cl0	0	0	0	3.39 MHz	
			0	1	6.78 MHz	
			1	0	13.56 MHz	
			1	1	No output	
0	-	-	Not used			-

1. Default setting takes place at power-up and after Set Default command.

1.3.4 Configuration Register 3 (ISO-14443A and NFC)

Address: 03h

Type: RW

Table 11. Configuration Register 3 (ISO-14443A and NFC)(1)

Bit	Name	Default	Function					Comments
7	crc_rx	0	1: Receive without CRC					For ISO-14443A anticollision. Valid only for ISO14443A mode, receive without CRC is not supported in ISO14443B mode.
6	no_par	0	1: No byte parity check					When set to 1 parity bits are still detected and removed before received data is put in FIFO, but without checking their correctness.
5	p_len3	0	**p_len3**	**p_len2**	**p_len1**	**p_len0**	**Reduction**	Modulation pulse reduction, defined in number of 13.56 MHz clock periods.
4	p_len2	0	0	0	0	0	0	
3	p_len1	0	0	0	0	1	74 ns	
2	p_len0	0	⋮	⋮	⋮	⋮	⋮	
			1	1	1	1	1106 ns	
1	-	-	Not used					-
0	-	-						-

1. Default setting takes place at power-up and after Set Default command.

1.3.5 Configuration Register 4 (ISO-14443B)

Address: 04h

Type: RW

Table 12. Configuration Register 4 (ISO-14443B)(1)

Bit	Name	Default	Function				Comments
7	egt2	0	**egt2**	**egt1**	**egt0**	**No. of EGT**	EGT time defined in number of etu
6	egt1	0	0	0	0	0	
5	egt0	0	0	0	1	1	
			⋮	⋮	⋮	⋮	
			1	1	1	6	
4	sof_0	0	0: 10 etu 1: 11 etu				SOF, number of etu with logic 0 (10 or 11)
3	sof_1	0	0: 2 etu 1: 3 etu				SOF, number of etu with logic 1 (2 or 3)
2	eof	0	0: 10 etu 1: 11 etu				EOF, number of etu with logic 0 (10 or 11)
1	egt	0	0: no EGT after last character 1: EGT after each character				-
0	-	-	Not used				-

1. Default setting takes place at power-up and after Set Default command.

1.3.6 Configuration Register 5

Address: 05h

Type: RW

Table 13. IO Configuration Register 5(1)

Bit	Name	Default	Function	Comments
7	pmd	0	0: AM demodulation 1: PM demodulation	AM/PM demodulation selection
6	am	0	0: OOK 1: AM	Valid for Transparent mode. For ISO-14443 and NFC modes, modulation type is set automatically (ISO-14443A and NFC is OOK, ISO-14443B is AM, see *Modulation Depth Definition Register*)
5	-	-	Not used	-
4	-	-		-
3	-	-		-
2	fifo_lr	0	0: 28 1: 24	FIFO water level for receive
1	fifo_lt	0	0: 4 1: 8	FIFO water level for transmit
0	-	-	Not used	-

1. Default setting takes place at power-up and after Set Default command.

1.3.7 Receiver Configuration Register

Address: 06h

Type: RW

Table 14. Receiver Configuration Register(1)

<table>
<tr><th>Bit</th><th>Name</th><th>Default</th><th colspan="5">Function</th><th>Comments</th></tr>
<tr><td>7</td><td>agc_en</td><td>0</td><td colspan="5">1: AGC enabled</td><td rowspan="2">AGC operation mode</td></tr>
<tr><td>6</td><td>agc_m</td><td>0</td><td colspan="5">1: AGC operates on first eight subcarrier pulses
0: AGC operates during the whole receive period</td></tr>
<tr><td>5</td><td>rg2</td><td>0</td><td>rg2</td><td>rg1</td><td>rg0</td><td colspan="2">Gain reduction</td><td rowspan="5">Gain reduction from 0 to 21 db, in 3 db steps</td></tr>
<tr><td>4</td><td>rg1</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">0</td></tr>
<tr><td rowspan="3">3</td><td rowspan="3">rg0</td><td rowspan="3">0</td><td>0</td><td>0</td><td>1</td><td colspan="2">3 db</td></tr>
<tr><td>⋮</td><td>⋮</td><td>⋮</td><td colspan="2">⋮</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td colspan="2">21 db</td></tr>
<tr><td>2</td><td>fs2</td><td>0</td><td>fs2</td><td>fs1</td><td>fs0</td><td>Filter selection(2)</td><td>Comments</td><td rowspan="11">Filter selection is automatically set when ISO mode or receive data rate changes (change of ISO Mode Definition Register). After automatic preset filter, selection can be changed by writing these bits.</td></tr>
<tr><td>1</td><td>fs1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>ISO-14443A 106 kbps</td><td rowspan="4">Automatic preset</td></tr>
<tr><td rowspan="6">0</td><td rowspan="6">fs0</td><td rowspan="6">0</td><td>0</td><td>0</td><td>1</td><td>ISO-14443B 106 kbps</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ISO-14443A/B 212 kbps</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>ISO-14443A/B 424 kbps</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>ISO-14443A/B 848 kbps</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>424/848 kHz subcarriers</td><td rowspan="2">No automatic preset</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>212 kHz subcarrier</td></tr>
<tr><td colspan="6">Other combinations not supported, or used for block testing purposes</td></tr>
</table>

1. Default setting takes place at power-up and after Set Default command.
2. Filter selection bits are preset also when ISO mode or receive data rate change.

1.3.8 Mask Interrupt Register

Address: 07h

Type: RW

Table 15. Mask Interrupt Register(1)r

Bit	Name	Default	Function	Comments
7	M_osc	0	Mask INTR when oscillator frequency is stable	-
6	M_nfc	0	Mask INTR due to NFC event	-
5	M_wl	0	Mask INTR due to FIFO water level	-
4	M_rxs	0	Mask INTR due to end of receive	-
3	M_txe	0	Mask INTR due to end of transmission	-
2	M_err	0	Mask INTR due to error in receive data coding	-
1	M_crc	0	Mask INTR due to CRC error	-
0	M_col	0	Mask INTR due to bit collision	-

1. Default setting takes place at power-up and after Set Default command.

1.3.9 Interrupt Register

Address: 08h

Type: RW

Table 16. Interrupt Register(1)(2)

Bit	Name	Default	Function	Comments
7	I_osc	0	INTR when oscillator frequency is stable	Set after enable
6	I_nfc	0	INTR due to NFC event	Set when nfc_t is 1 and en=0 informing that an RF field has been detected, Set when transmission could not be done due to detection of RF field during RF Collision Avoidance
5	I_wl	0	INTR due to FIFO water level	Set during receive, informing that FIFO is almost full and has to be read out. Set during transmit, informing that FIFO is almost empty and that additional data has to be sent.
4	I_rxs	0	INTR due to end of receive	-
3	I_txe	0	INTR due to end of transmission	-
2	I_err	0	INTR due to error in receive data coding	Includes parity error and framing error
1	I_crc	0	INTR due to CRC error	-
0	I_col	0	INTR due to bit collision	Valid only for ISO-14443A

1. Default setting takes place at power-up and after Set Default command.
2. After register is read, its content is set to 0.

1.3.10 FIFO Status Register

Address: 09h

Type: RW

Table 17. FIFO Status Register(1)

Bit	Name	Default	Function	Comments
7	fifo_b5	0	Number of bytes (binary coded) in the FIFO that have not been read out	Valid range is from 000000 to 100000
6	fifo_b4	0		
5	fifo_b3	0		
4	fifo_b2	0		
3	fifo_b1	0		
2	fifo_b0	0		
1	fifo_ovr	0	1: FIFO overflow	-
0	rx_act	0	1: Reception active	This bit is set to 1 when the start of a tag message is detected, and stays high until the end of the tag message is detected.

1. Default setting takes place at power-up, after Set Default and after Clear commands.

1.3.11 Collision Register (ISO-14443A only)

Address: 0Ah

Type: R

Table 18. Collision Register (ISO-14443A only)(1)

Bit	Name	Default	Function	Comments
7	c_byte3	0	Number of full bytes before the byte where the collision happened	-
6	c_byte2	0		
5	c_byte1	0		
4	c_byte0	0		
3	c_bit2	0	Number of bits before the bit where the collision happened	-
2	c_bit1	0		
1	c_bt0	0		
0	rfu	0	Not used	-

1. Default setting takes place at power-up, after Set Default and after Clear content commands.

1.3.12 Number of Transmitted Bytes Register 0

Address: 0Bh

Type: RW

Table 19. Number of Transmitted Bytes Register 0(1)

Bit	Name	Default	Function	Comments
7	ntx1	0	Number of bytes to be transmitted in one command (LSB bits)	Maximum supported number of bytes is 1023
6	ntx0	0		
5	nbtx2	0	Number of bits in the split byte, 000 means that the split byte is actually a complete byte	Applicable only to ISO-14443A bit oriented anticollision frame in case last byte is a split byte
4	nbtx1	0		
3	nbtx0	0		
2	-	0	Not used	-
1	frm4(2)	0	1: 4bit response frame	Has to be set to 1 when 4bit response frame is expected (Mifare Ultralight)
0	antcl(2)	0	1: ISO-14443 anticollision frame	Has to be set to 1 when ISO-14443A bit-oriented anticollision frame is sent

1. Default setting takes place at power-up, after Set Default and after Clear commands.
2. Cleared after transmission.

1.3.13 Number of Transmitted Bytes Register 1

Address: 0Ch

Type: RW

Table 20. Number of Transmitted Bytes Register 1(1)

Bit	Name	Default	Function	Comments
7	ntx9	0	Number of bytes to be transmitted in one command (MSB bits)	Maximum supported number of bytes is 1023
6	ntx8	0		
5	ntx7	0		
4	ntx6	0		
3	ntx5	0		
2	ntx4	0		
1	ntx3	0		
0	ntx2	0		

1. Default setting takes place at power-up, after Set Default and after Clear commands.

1.3.14 A/D Output Register

Address: 0Dh

Type: R

Table 21. A/D Output Register(1)

Bit	Name	Default	Function	Comments
7	ad7	-	Displays result of A/D conversion	-
6	ad6	-		
5	ad5	-		
4	ad4	-		
3	ad3	-		
2	ad2	-		
1	ad1	-		
0	ad0	-		

1. At power-up and after Set Default command content of this register is set to 0.

1.3.15 Antenna Calibration Register

Address: 0Eh

Type: R

Table 22. Antenna Calibration Register(1)

Bit	Name	Default	Function	Comments
7	tri_3	-	MSB	This register stores result of Calibrate Antenna command. LC trim switches are defined by data written in this register in case trim_s = 0. A bit set to 1 indicates that the corresponding transistor on TRIM1_x and TRIM2_x pin is switched on.
6	tri_2	-	-	
5	tri_1	-	-	
4	tri_0	-	LSB	
3	tri_err	-	1: Antenna calibration error	Set when Calibrate Antenna sequence has not been able to adjust resonance
2	-	-	Not used	-
1	-	-		
0	-	-		

1. At power-up and after Set Default command content of this register is set to 0.

1.3.16 External Trim Register

Address: 0Fh

Type: RW

Table 23. External Trim Register(1)

Bit	Name	Default	Function	Comments
7	trim_s	0	0: LC trim switches are defined by result of Calibrate Antenna command 1: LC trim switches are defined by bits tre_x written in this register	Defines source of driving switches on TRIMx pins
6	tre_3	0	MSB	LC trim switches are defined by data written in this register when trim_s=1. A bit set to 1 indicates that the corresponding transistor on TRIM1_x and TRIM2_x pin is switched on.
5	tre_2	0	-	
4	tre_1	0	-	
3	tre_0	0	LSB	
2	-	-	Not used	-
1	-	-		-
0	-	-		-

1. Default setting takes place at power-up and after Set Default command.

1.3.17 Modulation Depth Definition Register

Address: 10h

Type: RW

Table 24. Modulation Depth Definition Register(1)

Bit	Name	Default	Function	Comments
7	am_s	0	0: AM modulated level is defined by bits mod5 to mod0. Level is adjusted automatically by Calibrate Modulation Depth command 1: AM modulated level is defined by bits dram7 to dram0.	-
6	mod5	0	MSB	See *Section 1.2.14: AM modulation depth: definition and calibration on page 30* for details about AM modulation lavel definition.
5	mod4	0	-	
4	mod3	0	-	
3	mod2	0	-	
2	mod1	0	-	
1	mod0	0	LSB	
0	-	-	Not used	-

1. Default setting takes place at power-up and after Set Default command.

1.3.18 Modulation Depth Display Register

Address: 11h

Type: R

Table 25. Modulation Depth Display Register(1)

Bit	Name	Default	Function	Comments
7	md_7	0	MSB	Displays result of Calibrate Modulation Depth command. Antenna drivers are composed of 8 binary weighted segments. Bit md_x set to 1 indicates that this particular segment will be disabled during AM modulated state.
6	md_6	0	-	
5	md_5	0	-	
4	md_4	0	-	
3	md_3	0	-	
2	md_2	0	-	
1	md_1	0	-	
0	md_0	0	LSB	

1. At power-up and after Set Default command content of this register is set to 0.

1.3.19 Antenna Driver AM Modulated Level Definition Register

Address: 12h

Type: RW

Table 26. Antenna Driver AM Modulated Level Definition Register(1)

Bit	Name	Default	Function	Comments
7	dram7	0	MSB	Antenna drivers are composed of 8 binary weighted segments. Setting one of dram bits to 1 will disable the corresponding segment during AM modulated state in case am_s bit is set to 1.
6	dram6	0	-	
5	dram5	0	-	
4	dram4	0	-	
3	dram3	0	-	
2	dram2	0	-	
1	dram1	0	-	
0	dram0	0	LSB	

1. At power-up and after Set Default command content of this register is set to 0.

1.3.20 Antenna Driver Non-Modulated Level Definition Register

Address: 13h

Type: RW

Table 27. Antenna Driver Non-Modulated Level Definition Register(1)

Bit	Name	Default	Function	Comments
7	droff7	0	MSB	Antenna drivers are composed of 8 binary weighted segments. Setting one of droff bits to 1 will disable the corresponding segment during normal non-modulated operation.
6	droff6	0	-	
5	droff5	0	-	
4	droff4	0	-	
3	droff3	0	-	
2	droff2	0	-	
1	droff1	0	-	
0	droff0	0	LSB	

1. At power-up and after Set Default command content of this register is set to 0.

1.3.21 NFCIP Field Detection Threshold Register

Address: 14h

Type: RW

Table 28. NFCIP Field Detection Threshold Register(1)

Bit	Name	Default	Function	Comments
7	trg_l3	0	Target activation level MSB	Threshold used to detect presence of interrogator magnetic field. See *Table 29* for threshold definition.
6	trg_l2	0	-	
5	trg_l1	0	-	
4	trg_l0	0	Target activation level LSB	
3	trg_t3	0	Collision avoidance threshold MSB	Threshold used to detect presence of external field during collision avoidance. See *Table 30* for threshold definition.
2	trg_t2	0	-	
1	trg_t1	0	-	
0	trg_t0	0	Collision avoidance threshold LSB	

1. At power-up and after Set Default command content of this register is set to 0.

Table 29. Target activation threshold as seen on RFI1 input

trg_l3	trg_l2	trg_l1	trg_l0	Target activation threshold voltage
x	0	0	0	Forbidden (measurement is deactivated)
0	0	0	1	590 mV_{pp}
0	0	1	0	420 mV_{pp}
0	0	1	1	350 mV_{pp}
1	0	0	1	350 mV_{pp}
0	1	0	0	300 mV_{pp}
0	1	0	1	265 mV_{pp}
1	0	1	0	265 mV_{pp}
0	1	1	0	235 mV_{pp}
0	1	1	1	220 mV_{pp}
1	0	1	1	220 mV_{pp}
1	1	0	0	190 mV_{pp}
1	1	0	1	175 mV_{pp}
1	1	1	0	155 mV_{pp}
1	1	1	1	145 mV_{pp}

Table 30. Collision avoidance threshold as seen on RFI1 input

rfe_3	rfe_2	rfe_1	rfe_0	Collision avoidance threshold voltage
x	0	0	0	Forbidden (measurement is deactivated)
0	0	0	1	50 mV_{pp}
0	0	1	0	67 mV_{pp}
0	0	1	1	88 mV_{pp}
0	1	0	0	120 mV_{pp}
1	0	0	1	145 mV_{pp}
0	1	0	1	172 mV_{pp}
1	0	1	0	185 mV_{pp}
0	1	1	0	240 mV_{pp}
1	0	1	1	255 mV_{pp}
1	1	0	0	340 mV_{pp}
0	1	1	1	350 mV_{pp}
1	1	0	1	480 mV_{pp}
1	1	1	0	700 mV_{pp}
1	1	1	1	1080 mV_{pp}

1.3.22 Regulator Display Register

Address: 15h

Type: R

Table 31. Regulators Display Register(1)

Bit	Name	Default	Function	Comments
7	reg_3	0	MSB	Displays actual regulated voltage when regulator is operating. In Power-down mode its content is forced to 00h. See *Table 33* for definition.
6	reg_2	0	-	
5	reg_1	0	-	
4	reg_0	0	LSB	
3	-	0	Not used	-
2	-	0		-
1	-	0		-
0	-	0		-

1. At power-up and after Set Default command regulated voltage is set to 3.4 V (maximum value).

1.3.23 Regulated Voltage Definition Register

Address: 16h

Type: RW

Table 32. Regulated Voltage Definition Register(1)

Bit	Name	Default	Function	Comments
7	reg_s	0	0: Regulated voltages are defined by result of Adjust Regulators command 1: Regulated voltages are defined by rege_x bits written in this register	Defines mode of regulator voltage setting.
6	rege_3	0	MSB	External definition of regulated voltage. Refer to *Table 33* for definition.
5	rege_2	0	-	
4	rege_1	0	-	
3	rege_0	0	LSB	
2	-	0	Not used	-
1	-	0		-
0	-	0		-

1. Default setting takes place at power-up and after Set Default command.

Table 33. Regulated voltages

reg_3 rege_3	reg_2 rege_2	reg_1 rege_1	reg_0 rege_0	Regulated voltage (V)
1	1	1	1	3.4
1	1	1	0	3.3
1	1	0	1	3.2
1	1	0	0	3.1
1	0	1	1	3.0
1	0	1	0	2.9
1	0	0	1	2.8
1	0	0	0	2.7
0	1	1	1	2.6
0	1	1	0	2.5
0	1	0	1	2.4
Other combinations				2.4

1.3.24 Receiver State Display Register

Address: 17h

Type: R

Table 34. Receiver State Display Register(1)

Bit	Name	Default	Function				Comments
7	rssi_3	0	MSB				Stores peak value of AM channel RSSI measurement. Automatically cleared at beginning of tag message and with Clear RSSI command.
6	rssi_2	0	-				
5	rssi_1	0	-				
4	rssi_0	0	LSB				
3	oscok/rfp	0	Unlatched osc_ok flag when nfc=0 Target activation detector output when nfc=1				-
2	gr_2	0	**gr_2**	**gr_1**	**gr_0**	**Gain reduction**	Displays status of receiver gain reduction (result of AGC, gain reduction setting and Squelch command).
1	gr_1	0	0	0	0	0	
0	gr_0	0	0	0	1	3 db	
			⋮	⋮	⋮	⋮	
			1	1	1	21 db	

1. At power-up and after Set Default command content of this register is set to 0.

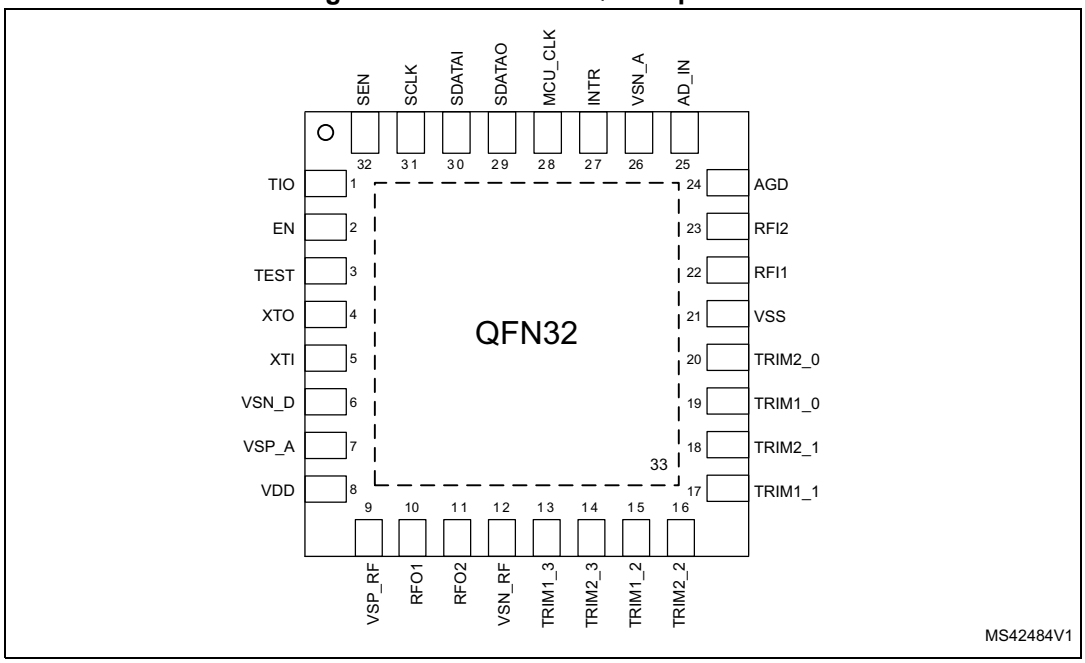
Table 35. RSSI

rssi_3	rssi_2	rssi_1	rssi_0	Typical signal on RFI1 (mV_{RMS})
0	0	0	0	0 to 0.28
0	0	0	1	0.28 to 0.35
0	0	1	0	0.35 to 0.45
0	0	1	1	0.45 to 0.57
0	1	0	0	0.57 to 0.74
0	1	0	1	0.74 to 0.95
0	1	1	0	0.95 to 1.21
0	1	1	1	1.21 to 1.56
1	0	0	0	1.56 to 2.00
1	0	0	1	2.00 to 2.55
1	0	1	0	2.55 to 3.27
1	0	1	1	3.27 to 4.20
1	1	0	0	4.20 to 5.37
1	1	0	1	5.37 to 6.88
1	1	1	0	6.88 to 8.80
1	1	1	1	> 8.80

2 Pinouts and pin description

The ST25R3910 pin and pad assignments are described in *Figure 12* .

Figure 12. ST25R3910 QFN32 pinout(1)



1. The above figure shows the package top view.

Table 36. ST25R3910 pin definitions - QFN32 package

Pin number	Pin name	Pin type	Description
1	TIO	Digital bidirectional	Test IO pin
2	EN	Digital input with pull down	Enable input
3	TEST		Test input
4	XTO	Analog output	Xtal oscillator output
5	XTI	Analog input	Xtal oscillator input
6	VSN_D	Supply pad	Digital ground
7	VSP_A	Analog input/output	Analog supply, regulator output
8	VDD	Supply pad	External positive supply
9	VSP_RF	Analog input/output	Supply, regulator output for antenna drivers
10	RFO1	Analog output	Antenna driver output
11	RFO2		
12	VSN_RF	Supply pad	Ground of antenna drivers

Table 36. ST25R3910 pin definitions - QFN32 package (continued)

Pin number	Pin name	Pin type	Description
13	TRIM1_3	Analog input	Input to trim antenna resonant circuit
14	TRIM2_3		
15	TRIM1_2		
16	TRIM2_2		
17	TRIM1_1		
18	TRIM2_1		
19	TRIM1_0		
20	TRIM2_0		
21	VSS	Supply pad	Ground, die substrate potential
22	RFI1	Analog input	Receiver input
23	RFI2		
24	AGD	Analog I/O	Analog reference voltage
25	AD_IN	Analog input	A/D converter input
26	VSN_A	Supply pad	Analog ground
27	INTR	Digital output	Interrupt request output
28	MCU_CLK		Microcontroller clock output
29	SDATAO	Digital output / tristate	Serial Peripheral Interface data output
30	SDATAI	Digital input	Serial Peripheral Interface data input
31	SCLK		Serial Peripheral Interface clock
32	SEN		Serial Peripheral Interface enable
33	VSUB	Supply	Ground, die substrate potential, connected to V_{SS} on PCB

3 Electrical characteristics

3.1 Absolute maximum ratings

Stresses beyond those listed *Table 37*, *Table 38* and *Table 39* may cause permanent damage to the device. These are stress ratings only.

Functional operation of the device at these or any other conditions beyond those indicated in *Section 3.2: Operating conditions* is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 37. Electrical parameters

Symbol	Parameter	Min	Max	Unit	Comments
V_{DD}	DC supply voltage	-0.5	5.0	V	-
V_{IN}	Input pin voltage (all except TRIM pins)	-0.5	5.0	V	-
V_{INTRIM}	Input pin voltage TRIM pins	-0.5	30	V	-
I_{scr}	Input current (latch-up immunity)	-100	100	mA	Norm: JEDEC 78

Table 38. Electrostatic discharge

Symbol	Parameter	Min	Max	Unit	Comments
ESD	Electrostatic discharge	±2	-	kV	MIL 883 E method 3015 (Human Body Model)

Table 39. Temperature ranges and storage conditions

Symbol	Parameter	Min	Max	Unit	Comments
T_{strg}	Storage temperature	-55	125	°C	-
T_{body}	Package body temperature	-	260	°C	The refllow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.”
RH_{NC}	Relative Humidity non-condensing	5	85	%	-
MSL	Moisture Sensitivity Level	3		-	Represents a max. floor life time of 168 h

3.2 Operating conditions

All defined tolerances for external components in this specification need to be assured over the whole operating conditions range and over lifetime.

Table 40. Operating conditions

Symbol	Parameter	Min	Max	Unit	Comments
V_{DD}	Positive supply voltage	2.4	3.6	V	In case power supply is lower than 2.6 V, PSSR cannot be improved using internal regulators (minimum regulated voltage is 2.4 V).
V_{SS}	Negative supply voltage	0	0	V	-
V_{INTRIM}	Input pin voltage TRIM pins	-	30	V	-
T_{AMB}	Ambient temperature	-40	85	°C	-

3.3 DC/AC characteristics for digital inputs and outputs

3.3.1 CMOS inputs

Valid for input pins EN, SEN, SDATAI, TEST and SCLK.

Table 41. CMOS inputs

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High level input voltage	0.7 * V_{DD}	-	-	V
V_{IL}	Low level input voltage	-	-	0.3 * V_{DD}	V
I_{LEAK}	Input leakage current	-	-	2	µA
R_{PD}	Pull down resistance (pad EN)	-	100	-	kΩ

3.3.2 CMOS outputs

Valid for output pins SDATAO, INTR and MCU_CLK.

Table 42. CMOS outputs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High level output voltage	I_{SOURCE} = 1mA	0.9 * V_{DD}	-	-	V
V_{OL}	Low level output voltage	I_{SINK} = 1mA	-	-	0.1 * V_{DD}	V
C_L	Capacitive load	-	0	-	50	pF
R_O	Output resistance	-	0	250	550	Ω

3.4 Electrical specifications

V_{DD}= 3.3 V, temperature 25 °C unless noted otherwise.

Table 43. Electrical specifications

Symbol	Parameter	Min	Typ	Max	Unit	Comments
I_{PD}	Supply current in Power-down mode	-	0.3	2	µA	-
I_{NFCT}	Supply current in initial NFC target mode	-	3.5	7	µA	-
I_{RD}	Supply current in Ready mode	-	2	3	mA	13.56 MHz Xtal, MCU_CLK disabled
I_{AL}	Supply current, receiver active	-	5	7	mA	
I_{LP}	Supply current, receiver active, low power mode	-	3	5	mA	
R_{RFO}	RFO1 and RFO2 driver output resistance	-	1.5	4	Ω	I_{RFO}=10 mA, all segments ON
V_{RFI}	RFI input sensitivity(1)	-	0.5	-	mV_{rms}	f_{SUB}=848 kHz
V_{RFI_LP}	RFI input sensitivity, low power receiver mode	-	1.5	-	mV_{rms}	
R_{RFI}	RFI input resistance	-	10	-	kΩ	-
V_{POR}	Power on Reset voltage	1.0	1.4	2.4	V	-
V_{AGD}	AGD voltage	1.4	1.5	1.6	V	-
V_{AR}	Regulator drop	-	250	-	mV	After execution of direct command Adjust Regulators
T_{OSU}	Oscillator start-up time	-	0.7	-	ms	13.56 MHz or 27.12 MHz crystal R_S=50 Ω max Load capacitance according to crystal specification

1. Amplitude of carrier signal at RFI inputs is 2.5 V_{pp}, maximum amplitude is 3 V_{pp}.

4 Package information

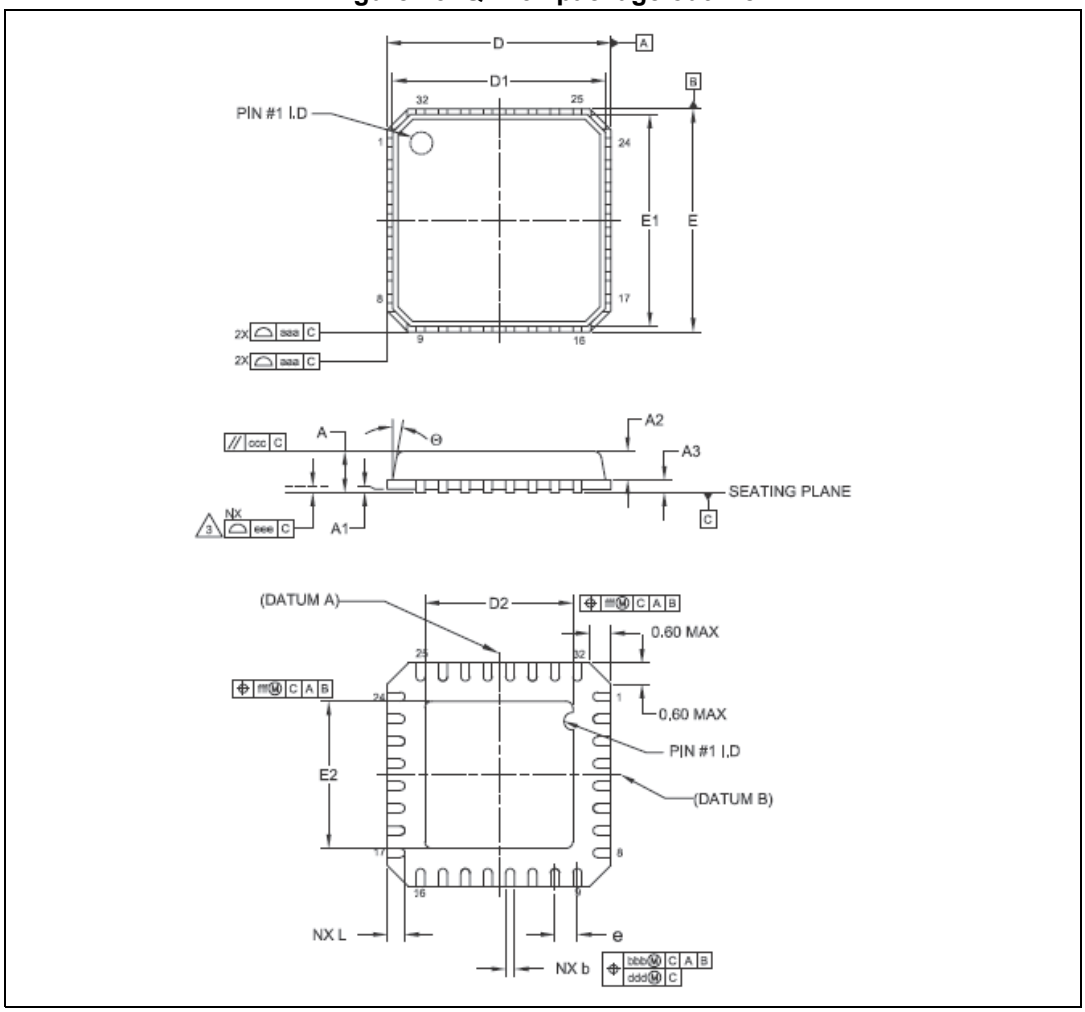
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at *www.st.com*.

ECOPACK® is an ST trademark.

4.1 QFN32 package information

The ST25R3910 is available in a 32-pin QFN (5 mm x 5 mm) package (see *Figure 13*). Dimensions are detailed in *Table 44*.

Figure 13. QFN32 package outline



1. Dimensioning and tolerances conform to ASME Y14.5M-1994.
2. Co-planarity applies to the exposed heat slug as well as to the terminal.
3. Radius on terminal is optional.
4. N is the total number of terminals.
5. This drawing is subject to change without notice.

Table 44. QFN32 5 mm x 5 mm dimensions[1]

Symbol (as specified in *Figure 13*)	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	-	0.65	1.00
A3	-	0.20	-
L	0.35	0.40	0.45
q	0°	-	14°
b	0.18	0.25	0.30
D	-	5.00 (with BSC)	-
E	-	5.00 (with BSC)	-
e	-	0.50 (with BSC)	-
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
D1	-	4.75 (with BSC)	-
E1	-	4.75 (with BSC)	-
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N[2]	32		

1. All dimensions are in mm. All angles are in degrees.
2. Total number of terminals.

5 Part numbering

Table 45. Ordering information scheme

Example: ST25 R 39 10 - B QF T

Device type

ST25 = NFC/RFID tags and readers

Product type

R = Reader

Frequency range

39 = HF products

Product feature

10 = Mid range reader / NFC initiator

Temperature range

B = -40 °C to 85 °C

Package/Packaging

QF = 32-pin QFN (5 mm x 5 mm)

Tape and Reel

T = 4000 pcs/reel

Note: Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6 Revision history

Table 46. Document revision history

Date	Revision	Changes
21-Nov-2016	1	Initial release.
08-Feb-2017	2	Updated *Section 1.1.2: Receiver*, *Section 1.1.3: Phase and amplitude detector*, *Section 1.1.4: A/D converter*, *Section 1.1.6: Quartz crystal oscillator*, *Section 1.1.7: Power supply regulators*, *Section 1.1.8: POR and Bias*, *Squelch* and *RSSI*. Updated *Table 45: Ordering information scheme*.