User's Guide

ISO1640DEVM Evaluation Module Users Guide

ABSTRACT

This user's guide describes the ISO1640DEVM evaluation module (EVM) for TI's ISO1640 and ISO1641 isolated I2C transceivers. This EVM helps designers evaluate the devices' performance for quick development and analysis of data transmission systems using TI's ISO1640 and ISO1641 isolated I2C devices in 8-pinD and 16-pinDW packages.

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1 Introduction

This User's Guide presents a typical laboratory setup used with this EVM.

CAUTION

This Evaluation Module (EVM) is made available for isolator parameter performance evaluation only and is not intended for isolation voltage testing. Do not use this EVM for isolation voltage tests even though the I2C devices have galvanic isolation protection. To prevent damage to the EVM, any voltage applied as a supply or digital input/output must be maintained within the 0 V to 5.5 V recommended operating range.

Exceeding the specified input voltage range and applying loads outside the specified output range may cause unexpected operation and irreversible damage to the EVM. If there is uncertainty as to the input voltage range or load specification, please contact a TI field representative or create a post on e2e.ti.com/ prior to connecting power.

2 Overview

The ISO164x family of devices are low-power, bidirectional isolators that are compatible with I2C interfaces. The logic input and output buffers on these devices are separated by TI's Isolation technology utilizing a silicon dioxide (SiO2) barrier. Devices with a B suffix are 3-kVRMS basic isolated transceivers while devices without a B suffix are 5-kVRMS reinforced isolated devices. When used with isolated power supplies, these devices block high voltages, isolate different grounds, and prevent noise currents from entering isolated grounds and interfering with or damaging sensitive circuitry.

The ISO1640 has two bidirectional channels for clock and data lines and is fit for multi-master and clock-stretching applications. The ISO1641 has a bidirectional data and unidirectional clock channel and is suitable in applications that have a single master device and do not implement clock-stretching features.

These devices achieve isolated bidirectional communication by introducing a static voltage offset (SVO), making the side 1 low-level output greater than the side 1 low-level input, thus preventing an internal logic latch that otherwise would occur with standard digital isolators.

This EVM can be used to evaluate different system parameters of ISO1640 and ISO1641 devices. Test signals and sequences can be applied to the device channels to evaluate performance characteristics of parameters such as propagation delay, rise / fall times, and power consumption for different device conditions. Users can evaluate these parameters in their own lab environment.

This EVM can physically support evaluation of ISO1640DW and ISO1641DW devices by soldering either device in the U2 landing component and removing the ISO164xD device from the U1 position.

Note

Ensure that U1 and U2 are not populated at the same time

If ISO1641 devices are evaluated by the user, please note that the SCL channel will not support bidirectional operation, and although the DW-IC landing pattern is the same as other isolator devices, these devices may have different pin configurations than ISO1640DW and ISO1641DW, and **SHOULD NOT** be installed on this EVM.

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3 Pin Configurations of Isolated I2C Transceivers

The pin configurations of ISO1640 and ISO1641 in D and DW packages are shown in Figure 3-1.

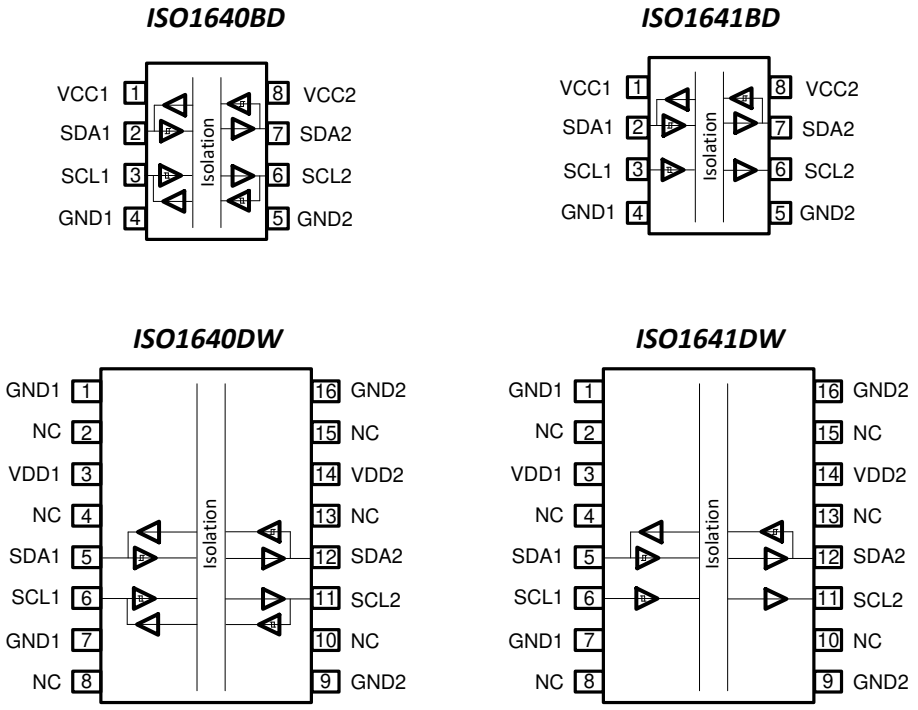

Figure 3-1. ISO1640 and ISO1641 Pinouts

The EVM PCB is shown in Figure 3-2 and comes with an ISO1640D installed in place of U1. However, this EVM can also be configured for evaluation of ISO1641D by replacing the included ISO1640D device in place of U1 or ISO1640DW and ISO1641DW devices by removing U1 and soldering an ISO1640DW or ISO1641DW in place of U2.

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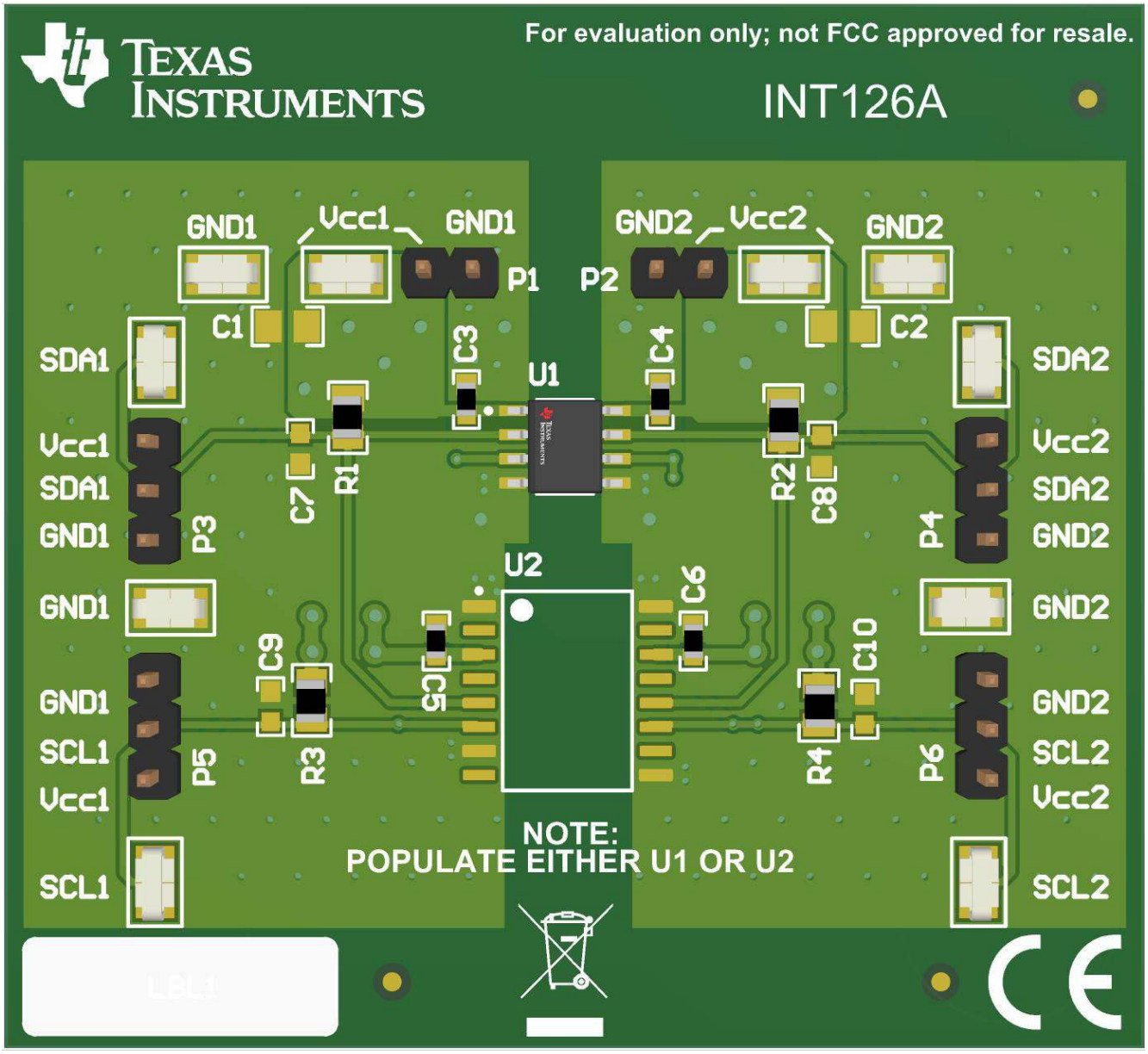

Figure 3-2. ISO1640DEVM Top View

4 EVM Setup and Operation

CAUTION

Note that this EVM is for operating-parameter performance evaluation only and not designed for isolation voltage testing. Any voltage applied above the 5.5-V maximum recommended operating voltage of the isolators may damage the EVM.

This section describes the setup and operation of the EVM for parameter-performance evaluation. Figure 4-1 shows the basic setup of the EVM with two power supplies needed to evaluate isolator performance. Power this Evaluation Module by connecting voltages to Vcc1 and Vcc2 that are within the Recommended Operating Range in the ISO164x device datasheet. Typical voltage levels for the Vcc1 and Vcc2 supplies are 3.3V and 5V. Separate power supplies can be used to provide each supply voltage, and they do not need to have the same value. If both sides are to be evaluated at the same supply voltage, only one power supply is required and can power both sides of the EVM.

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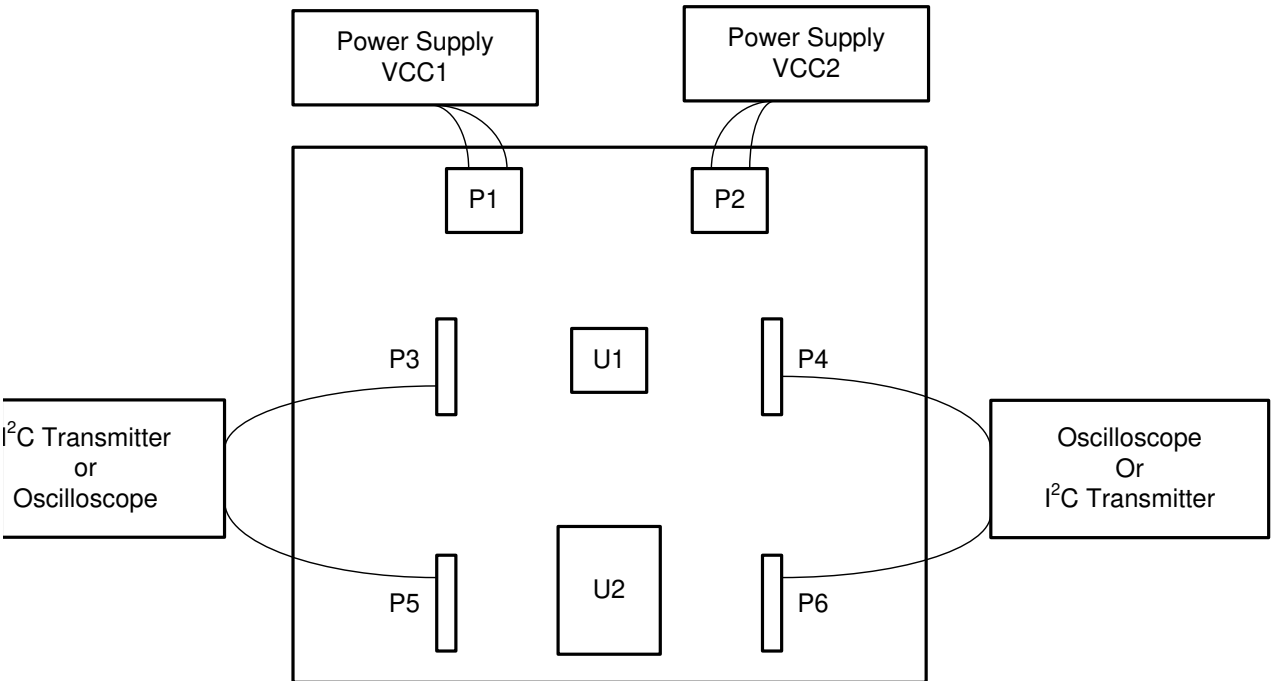

Figure 4-1. Basic EVM Operation

Although the ISO1640 and ISO1641 devices feature bidirectional data channels, the devices perform optimally when side 1 (SDA1 and SCL1) is connected to a single controller or node of an I2C network while side 2 (SDA2 and SCL2) is connected to the I2C bus. Please note that if the ISO1641 is used, providing an input signal on the SCL2 pin does not yield any changing output on SCL1: SCL1 remains pulled up to Vcc1

Table 4-1 shows the information on jumper configurations for basic tests

Table 4-1. Jumper Descriptions

Label	Description
U1	ISO164xD,by default populated as ISO1640D
U2	ISO1640DW/ISO1641DW,by default not populated
P1	2-pin jumper for Side 1 power supply, Vcc1
P2	2-pin jumper for Side 2 power supply, Vcc2
P3	3-pin jumper to Vcc1, GND1, and SDA1
P4	3-pin jumper to Vcc2, GND2, and SDA2
P5	3-pin jumper to Vcc1, GND1, and SCL1
P6	3-pin jumper to Vcc2, GND2, and SCL2

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5 Bill of Materials

Table 5-1 lists the bill of materials (BOM) for ISO1640DEVM.

Table 5-1. ISO164xDEVM EVM Bill of Materials

Item	Qty.	Designator	Description	Manufacturer	Part Number
1	4	C3, C4, C5, C6	CAP, CERM, 0.1 µF, 25 V, +/-10%, X7R, 0603	TDK	C1608X7R1E104K080AA
2	4	R1, R2, R3, R4	RES, 4.75 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	Panasonic	ERJ-6ENF4751V
3	2	P1, P2	Header, 2.54 mm, 2x1, Gold, TH	Wurth Elektronik	61300211121
4	4	P3, P4, P5, P6	Header, 2.54 mm, 3x1, Gold, TH	Wurth Elektronik	61300311121
5	10	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10	Test Point, Miniature, SMT	Keystone	5019
6	4	H1, H2, H3, H4	Bumpon, Hemisphere, 0.44 X 0.20, Clear	3M	SJ-5303 (CLEAR)
7	1	U1	IC, ISO1640, SMT, SOIC8D Robust-EMC Bidirectional I2C Digital Isolator	Texas Instruments	ISO1640D

6 EVM Schematic and PCB

The ISO1640 isolated I2C EVM comes with an ISO1640D installed in place of U1. This EVM can also be configured for use with an ISO1641D, ISO1640DW, or ISO1641DW.

Each signal line (SDAx, SCLx) is configured with a 4.75-kΩ pull-up resistor (R1 to R4) to the corresponding power supply (Vccx). These resistors may be replaced with 0805 resistors of other values per the application requirements; for insight on calculating appropriate pull-up resistor values for I2C buses, please refer to SLVA689, I2C Bus Pullup Resistor Calculation.

Note

ISO164x devices are designed to sink different amounts of current on Side 1 and Side 2, so be careful to choose resistors that keep I_{OL1} and I_{OL2} within the recommended operating range if replacing resistors R1 to R4.

Signal pins my be tied directly to ground using the ground jumpers (P3 and P5 on side 1; P4 and P6 on side 2) to simulate a device pulling the I2C line low. While not being actively driven low, the lines will be pulled up through the included pull-up resistors. Signal lines should not be tied directly to a supply voltage without a pull-up resistor to limit input current. These jumpers also provide input /output signal access, including for oscilloscope probes, to each pin.

Note

Ensure that SDAx and SCLx signal lines are not tied directly to Vccx. A current-limiting pull-up resistor is required, and populated by default, to limit current in the cases where the device pins drive a low-voltage.

A schematic diagram for this EVM is shown in Figure 6-1 below, and Figure 6-2 and Figure 6-3 show the printed circuit board (PCB) layout.

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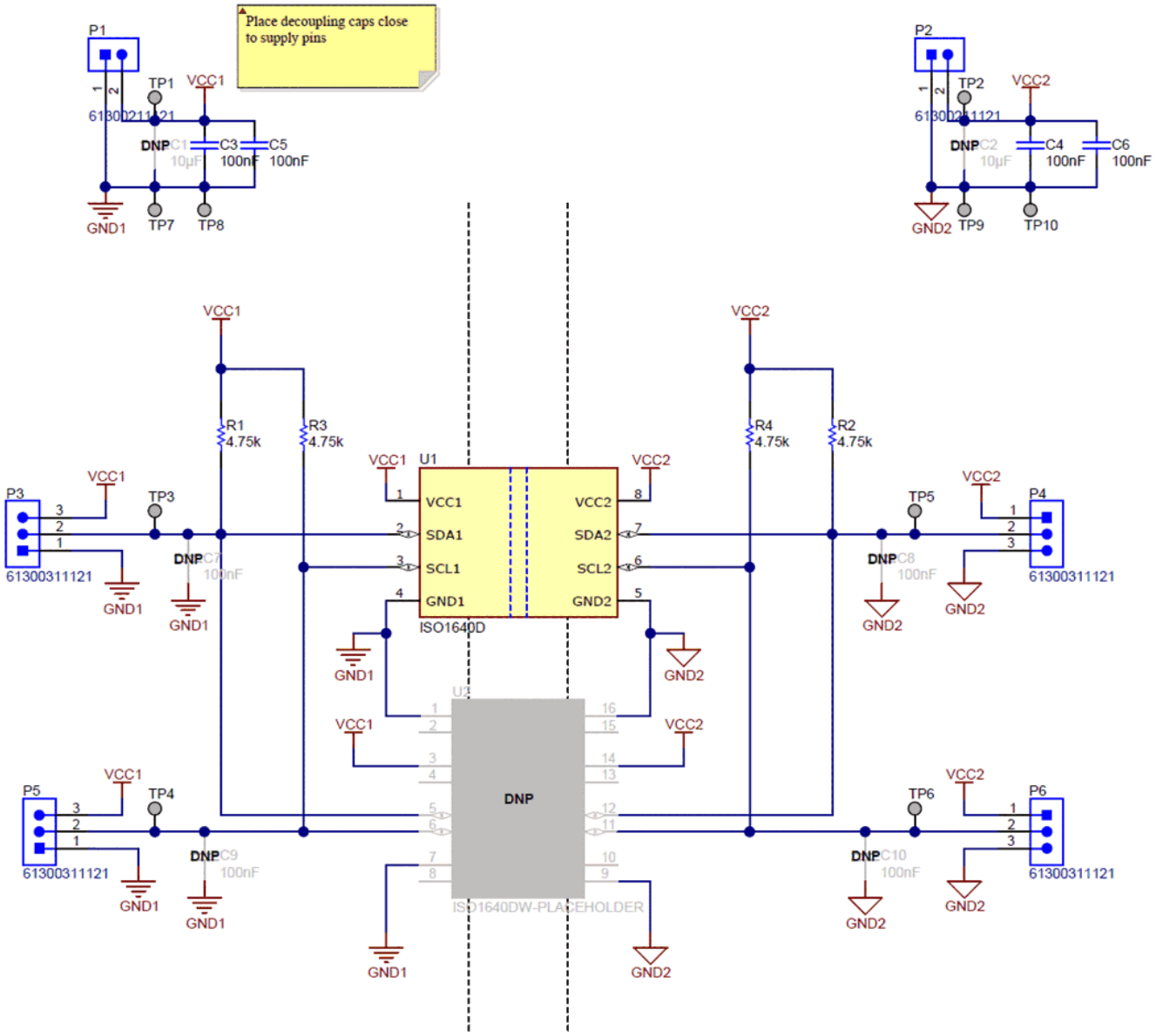

Figure 6-1. ISO1640DEVM Schematic

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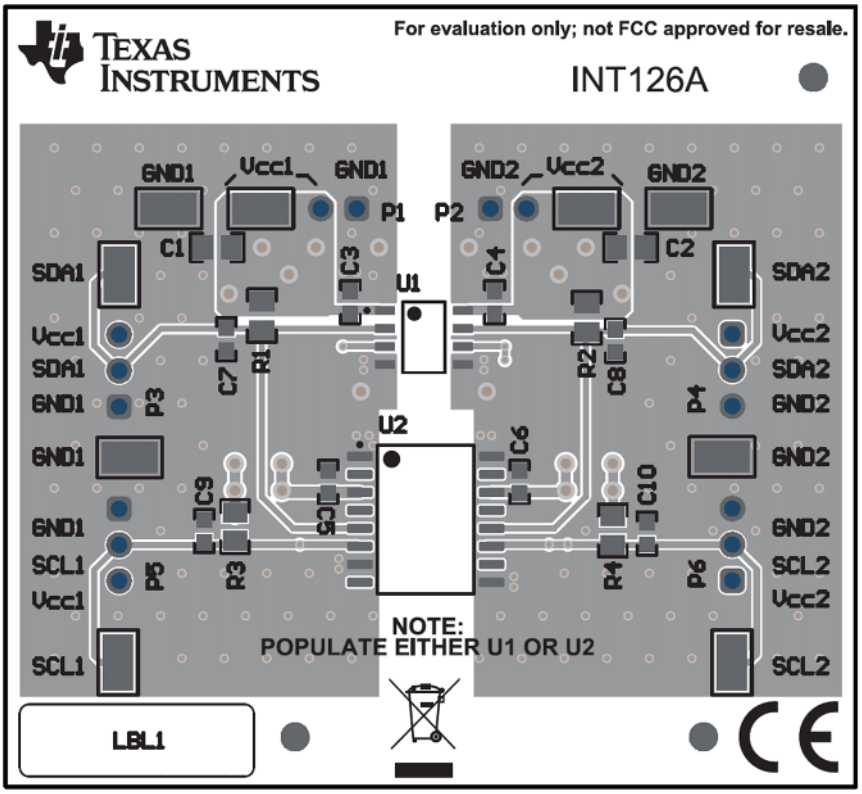

Figure 6-2. ISO1640DEVM Top PCB Layout

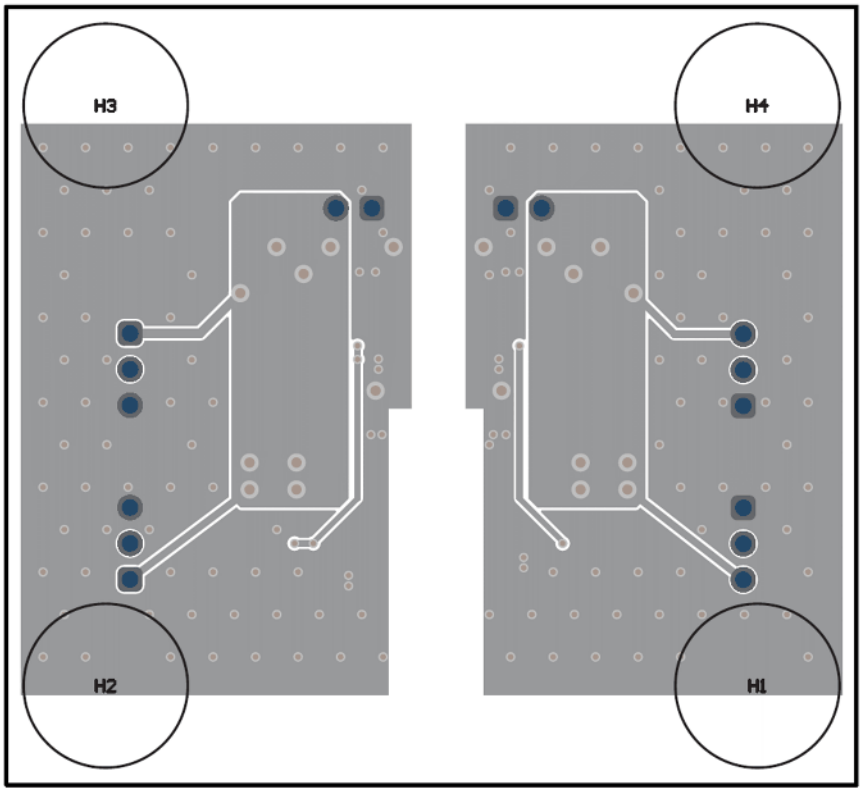

Figure 6-3. ISO1640DEVM Bottom PCB Layout

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