

bq24070/1 1.5-A Single-Chip Li-Ion and Li-Pol Charge Management IC EVM

This user's guide describes the bq24070/1 evaluation module (EVM). The EVM provides a convenient method for evaluating the performance of a charge management and system power solution for portable applications using the bq24070/1 product family. A completely designed and tested module is presented. The charger is designed to deliver up to 1.5 A of continuous current to the system or charger for one-cell Li-ion or Li-polymer applications using a dc power supply. The charger is programmed from the factory to deliver 1 A of charging current.

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1 Introduction

The bq24070/1 powers the system while independently charging the battery. This feature reduces the charge and discharge cycles on the battery, allows for proper charge termination, and allows the system to run with an absent or defective battery pack. This feature also allows for the system to turn on instantaneously from an external power source even when using a deeply discharged battery pack.

The IN pin can be programmed to perform like a USB input by pulling the MODE pin low or like an adapter input if the MODE pin is pulled high. An external resistor, RSET1, sets the magnitude of the charge current. If the charge current exceeds the available input current, the voltage on the OUT pin drops to the $DPPM_{OUT}$ threshold or the battery voltage, whichever is higher. The charging current is reduced to what current is available ($I_{BAT} = I_{IN} - I_{OUT}$).

The bq24070/1 charges the battery in three phases: conditioning, constant-current, and constant-voltage. Charge is terminated based on minimum current. A resistor-programmable charge timer provides a backup safety for charge termination. The bq24070/1 automatically restarts the charge if the battery voltage falls below an internal threshold. The bq24070/1 automatically enters sleep mode when both supplies are removed (a drop to the battery voltage).

The bq24070 regulates the OUT pin at 4.4 VDC whereas the BQ24071 regulates the output at 6 VDC if the input is greater than $6\text{ VDC} + V_{DO}$ (V_{DO} = dropout voltage between IN and OUT). For lower input voltages, the OUT pin is $V_{IN} - V_{DO}$.

2 Considerations When Testing and Using bq24070/1 ICs

It is recommended to read the bq24070/1 data sheet prior to evaluating this EVM. Consider the following noteworthy items while testing and using the bq24070/1 IC.

The two potential sources to power the system (V_{OUT}) are: IN (adapter or USB source) and the battery. The IC is designed to power the system continuously. The battery, in most cases, is the last line of backup. If the adapter or USB input is not available (or disabled), the battery connects to the system.

In thermal regulation condition ($T_J = 125^\circ\text{C}$ —not a first-choice design mode of operation), the charge current is reduced to the battery, and the system still gets its power from the input. The battery supplement is still available in thermal regulation if V_{OUT} falls to V_{BAT} . In thermal cutoff ($\sim 155^\circ\text{C}$), the input sources are disconnected, but the internal battery FET connects the battery to V_{OUT} .

There are two types of OUT-pin short circuit, one associated with the input IN pin ($V_{OUT} < 1\text{ V}$) and the other associated with the BAT pin ($V_{BAT} - V_{OUT} > 200\text{ mV}$). For the BAT short circuit, the battery FET opens if a short on V_{OUT} pulls more than $\sim 4\text{ A}$ of current ($>200\text{-mV}$ drop across the BAT FET) from the battery. The recovery method is from a 10-mA current source between the BAT and OUT pins, so the short and any system load must be removed before the OUT pin can recover within 200 mV of V_{BAT} . Note that the current source is $\sim 10\text{ mA}$ with the OUT pin near 0 V, but falls off to $\sim 2\text{ mA}$ as the OUT pin goes above 1 V. For the IN-to-OUT short-circuit case where the OUT pin is less than 1 V, the recovery method is by a 500- Ω pullup resistor from IN to OUT. The system load must be reduced ($>200\ \Omega$) such that the pullup can pull V_{OUT} above 1 V.

When there is no power to the system and the battery is hot-plugged, the BAT-pin voltage leads the OUT-pin voltage due to the system capacitance, and the output may go into BAT short-circuit mode. To avoid this, a feature was added to the DPPM pin. If the voltage on the DPPM pin is held below 1 V, then the short-circuit feature is disabled. Therefore, placing a small capacitor ($\sim 1\text{ nF}$ to 10 nF) across the DPPM resistor delays the short-circuit protection on input power-up by a few microseconds.

Another feature that protects system integrity is dynamic power path management (DPPM). The voltage on the DPPM pin ($DPPM_{IN}$) times a scaling factor of ~ 1.15 is the $DPPM_{OUT}$ voltage. The $DPPM_{OUT}$ voltage is the critical voltage, determined by the designer, where battery charging current is reduced to keep the system voltage (V_{OUT}) from further decay. A special feature to keep in mind is that when in DPPM mode, the internal oscillator timer is slowed in proportion to the reduction in programmed charger current. This allows the timers (safety and others) to be appropriately adjusted during operation. Therefore, when performing any test where time is measured, keep in mind this adjustment factor.

The MODE (High/Low) sets which input source is present (adapter or USB). The CE pin (going high) immediately enables the chip; disabling it (going low) delays handoff for 5 ms.

3 Performance Specification Summary

Table 1 summarizes the performance specifications of the EVM.

Table 1. Performance Specification Summary For bq24070/1 EVM

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input dc voltage, $V_{I(AC)}$		4.8	5	6.5	V
Input dc USB voltage, $V_{I(USB)}$			5		
Battery charge current, $I_{O(CHG)}$			1	2+	A
Power dissipation, bq24070/1 IC, 1 cell	$P_{DISS} = (V_{IN} - V_{OUT})I_{out} + (V_{IN} - V_{BAT})I_{BAT} + (V_{IN} - V_{LDO})I_{LDO}$			See ⁽¹⁾	W

(1) The HPA180 (bq24070/1) thermal design is optimized (8+ vias, 0.031-inch PWB, 2 oz. copper) to give $\theta_{JA} \sim 27^{\circ}\text{C/W}$.

4 Test Summary

This section covers the setup and tests performed in evaluating the EVM.

4.1 Equipment

- Power supply (5.25 ± 0.25 VDC), current limit set to 2.0 A ± 0.2 A for AC input to the UUT
- Three Fluke 75 DMMs (equivalent or better)
- Oscilloscope, Model TDS220 (equivalent or better)

4.2 Equipment Setup

- Preset the UUT power supply voltage and current prior to connection to UUT; turn off the power supply and connect the supply to J1-IN/GND (+ to IN and – to GND).
- Connect a 10-Ω to 30-Ω load to J4-OUT/GND.
- Connect a fully discharged (< 2.8-VDC) single-cell Li-ion or Li-polymer battery to J2-BAT+/BAT–.
- Connect the DMMs as shown in Figure 1.

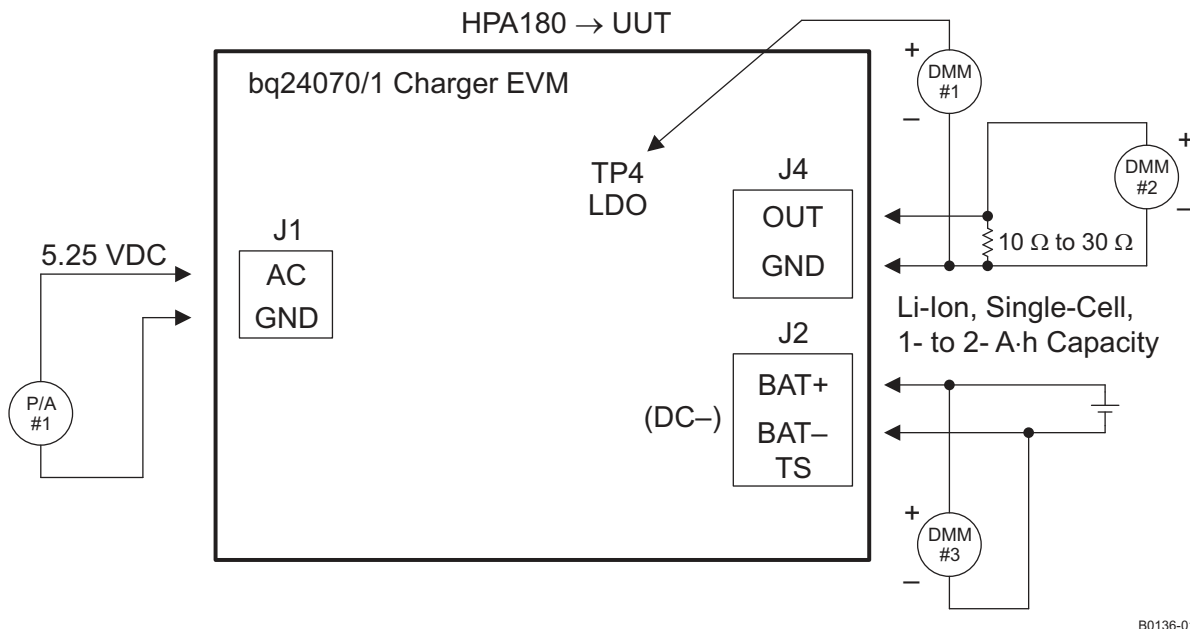


Figure 1. Test Diagram

4.3 Test Procedure

1. Verify that the equipment is set up according to *Equipment Setup*, [Section 4.2](#).
2. Set jumpers on the UUT as follows: JMP1 to 0.5; JMP2 to HI; JMP3 to EN; install jumpers on JMP4 through JMP6.
3. Adjust **R_DPPM** until TP1 is **35.7 kΩ ±0.1 kΩ** with respect to GND, and adjust **R_TMR** until TP2 is 50 kΩ with respect to GND.
4. Verify that **V_{OUT}** is approximately equal to **V_{BAT}** (if **V_{OUT}** < 1.1 V, the output is in short-circuit mode. To get out of this mode, momentarily disconnect the load on the OUT pin).
5. Power up the **5.25-VDC supply** to the UUT.
6. Verify **V_{BAT}** is between 2.4 VDC and 3 VDC, and the charger is in pre-charge state: LEDs STAT1 (D2), STAT2 (D3), and ACPG (D1) are on.
If **V_{BAT}** is above the low-voltage threshold (**V_(LOWV)** ~3 V), then the IC is in fast-charge mode [STAT2 (D3) is off (High)]. If the IC is in fast charge, skip to step 10.
7. Verify **I_{BAT}** is ~0.1 A (**I_{BAT}** ~ **I_{IN}** - (**V_{OUT}** / **R_{OUT}**) - 0.01 A)
8. Verify **V_{OUT}** is between 4.3 VDC and 4.5 VDC for the bq24070 IC and between 4.8 VDC and 5.5 VDC (**V_{IN}** - **V_{DO}**) for the bq24071 IC.
9. Verify **V_{LDO}** (TP4) is between 3.2 VDC and 3.4 VDC.
10. Allow the battery to charge until **V_{BAT}** is between 3.2 VDC and 4.0 VDC. The charger should deliver the programmed constant current to the battery unless the input cannot source the required current.
11. Verify **D3** (STAT2) has turned off.
12. Verify **I_{BAT}** is ~1.0 A [for a 10-kΩ resistor on *ISET1*, **I_{BAT}** ~ **I_{IN}** - (**V_{OUT}** / **R_{OUT}**) - 0.01 A].
13. Apply a short between J3-4 (CE) and J3-3 (GND) on the UUT. This overrides the JMP3 100-kΩ pullup, disables the charging, puts the IC in low-power mode, and connects the battery to the OUT pin. Note that if CE is floated (JMP3 is removed and J3-3 to 4 connection is removed), the IC may bounce between the charging and disabled states. Verify on the scope that **V_{OUT}** does not drop out when switching between the input source and the battery source.
14. Verify **D2** (STAT1) has turned off.
15. Verify **I_{IN}** drops below 10 mA [should be < 200 μA into the IC if **P_G** LED (current) JMP6 is removed].
16. Verify **V_{OUT}** is within -50 mV of **V_{BAT}**.
17. Remove short between J3-4 and J3-3 on UUT. Verify on the scope that **V_{OUT}** does not drop out. Verify **D2** (STAT1) has turned on, charging has resumed, and **V_{OUT}** is powered from the input.
18. Disconnect the **5.25-VDC input supply** from the UUT IN input. Verify on the scope that **V_{OUT}** does not drop out. Verify **V_{OUT}** is within -50 mV of **V_{BAT}** and **D2** (STAT1) and **D1** (**P_G**) LEDs turn off. This demonstrates battery power backup for loss of adapter power.
19. Reapply the +5.25-VDC supply to the UUT IN input. Verify on the scope that **V_{OUT}** does not drop out. Verify **D2** (STAT1) and **D1** (**P_G**) LEDs turn on.
20. Reduce the current limit on the input supply to ~ 1 A (going to the IN pin on the UUT) and verify on the scope that **V_{OUT}** has dropped to the VDPPM level of ~4.2 V [(3.57 V at TP1) × 1.15 = 4.1 V]. Note that the current into the battery is ~ 590 mA (1-A input minus 410 mA to the system for a 10-Ω load), which has been reduced to keep the output from falling below the programmed DPPM OUTPUT threshold of 4.1 V. This demonstrates DPPM operation (charging current to the battery is reduced if output drops to the DPPM OUTPUT voltage threshold attempting to keep the output voltage from dropping further).
21. Further reduce the input current limit to 250 mA. Verify on the scope that **V_{OUT}** does not drop out. Verify that **V_{OUT}** drops just below **V_{BAT}** (< 50 mV). Because the available input current is less than the system **OUT** load, reducing the battery charging current to zero is still not enough reduction in load to keep the output from dropping. Once the output drops below ~ 60 mV, the internal battery FET turns on and allows the battery to source the OUT pin system load. This demonstrates battery supplement mode.
22. Return the current limit of the 5.25-V supply to ~2 A. Verify **V_{OUT}** returns to ~4.4 V.
23. Set JMP2 (MODE) to LO (USB mode). Verify that the input current, **I_{IN}**, drops to between 400 mA and 500 mA. The programmed charge current of ~1 A and the system load of 10 Ω exceeds the USB-mode 0.5-A limit; therefore, **V_{OUT}** drops until the DPPM OUTPUT voltage threshold or battery voltage is reached (whichever is higher). If the DPPM OUTPUT threshold is higher, the charging current is reduced to keep the output voltage from dropping further. If the battery voltage is higher, the battery supplements the current to keep the output from dropping too much (20 mV to 200 mV) below the

battery voltage.

24. Set JMP2 (MODE) to HI and verify that the input supply is providing ~1.5 A of current (~0.44, for a 10- Ω resistor, to the load and 1 A to the battery).
25. Set JMP1 to 0.1 on the UUT. Verify that the battery charge has dropped in half. The input current should be $\sim I_{\text{BAT}} (\sim 0.5 \text{ A}) + I_{\text{OUT}} (\sim 4.4 \text{ V}/10 \Omega = 0.44 \text{ A}) \approx 0.94 \text{ A}$.
26. Set JMP1 to 0.5. Continue to let the battery charge. Note that once the battery voltage reaches regulation (~4.2 VDC), the charging current tapers off.
27. Verify that the charging terminates when the battery current tapers to C/10 or 100 mA (1 A/10, programmed charge current divided by 10). Verify D2 (STAT1) turns off (High) and D3 (STAT2) turns on (Low).
28. If a load is applied across the battery such that the battery is discharged to ~4.1 V, the charger starts a new charging cycle.

This concludes the evaluation of the bq24070/1 EVM. Several more features implemented in the IC are not demonstrated in this user's guide. See the data sheet to learn more about thermal regulation, thermal cutoff, USB boot up, and short-circuit protection.

6 Physical Layouts

This section contains the board layout and assembly drawings for the EVM.

6.1 Board Layout

Figure 3 shows the top assembly view of the EVM. Figure 5 shows the top etch layer of the EVM. Figure 6 shows the board second etch layer of the EVM. Figure 7 shows the board third etch layer of the EVM. Figure 8 shows the bottom etch layer of the EVM.

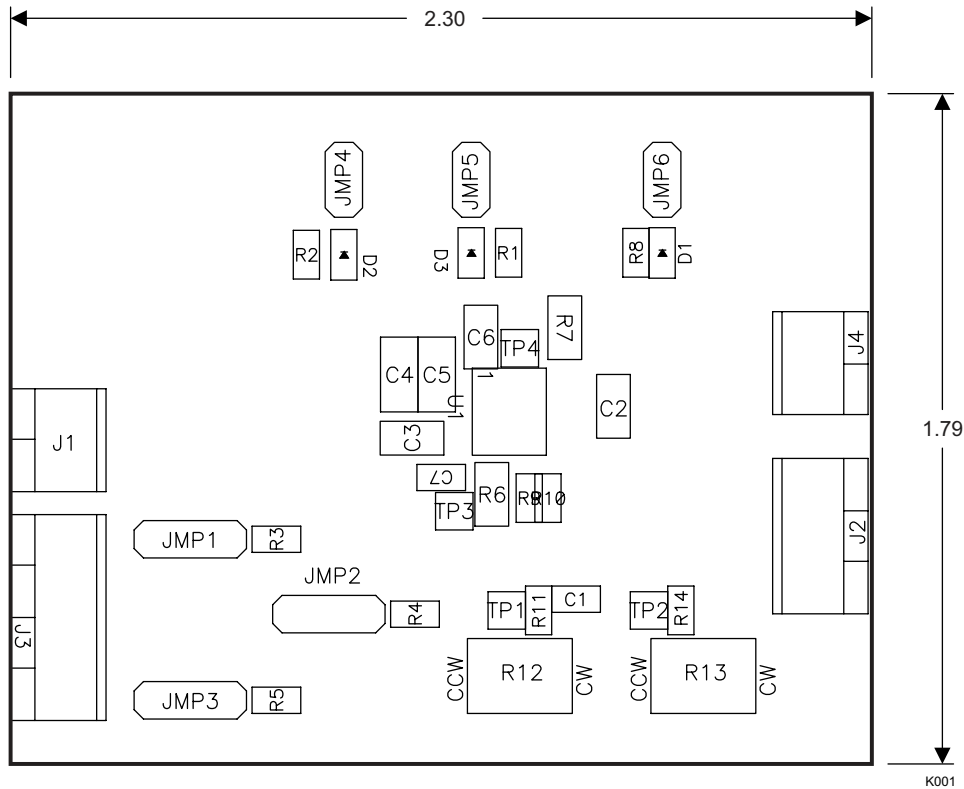


Figure 3. Top Assembly View

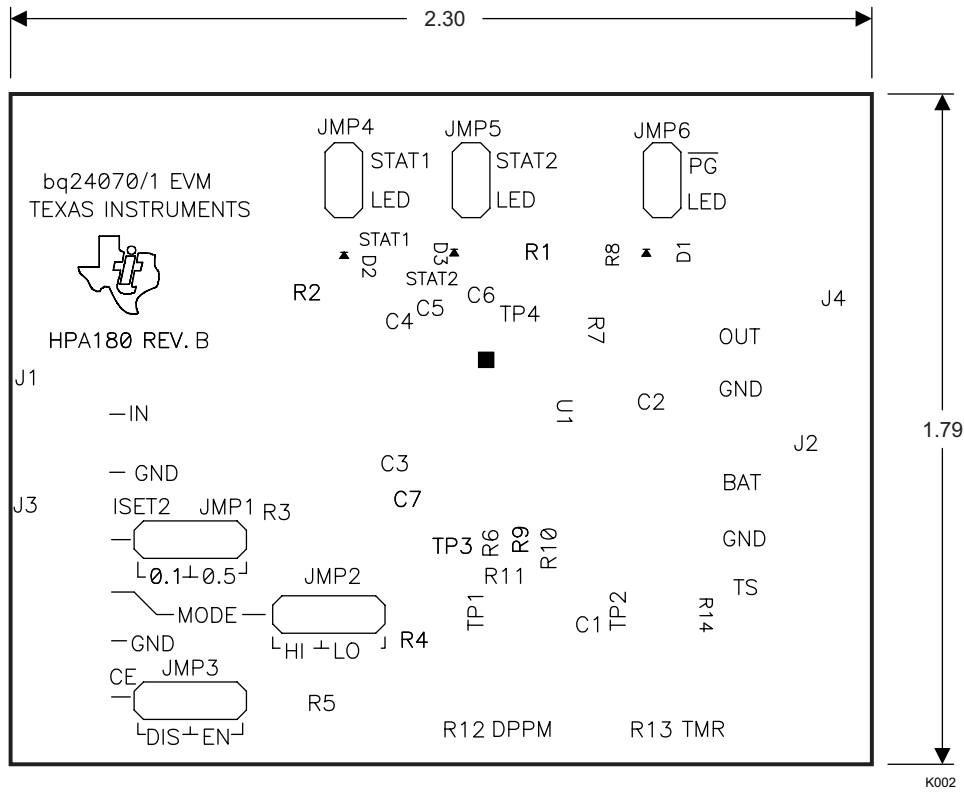


Figure 4. Top Silkscreen

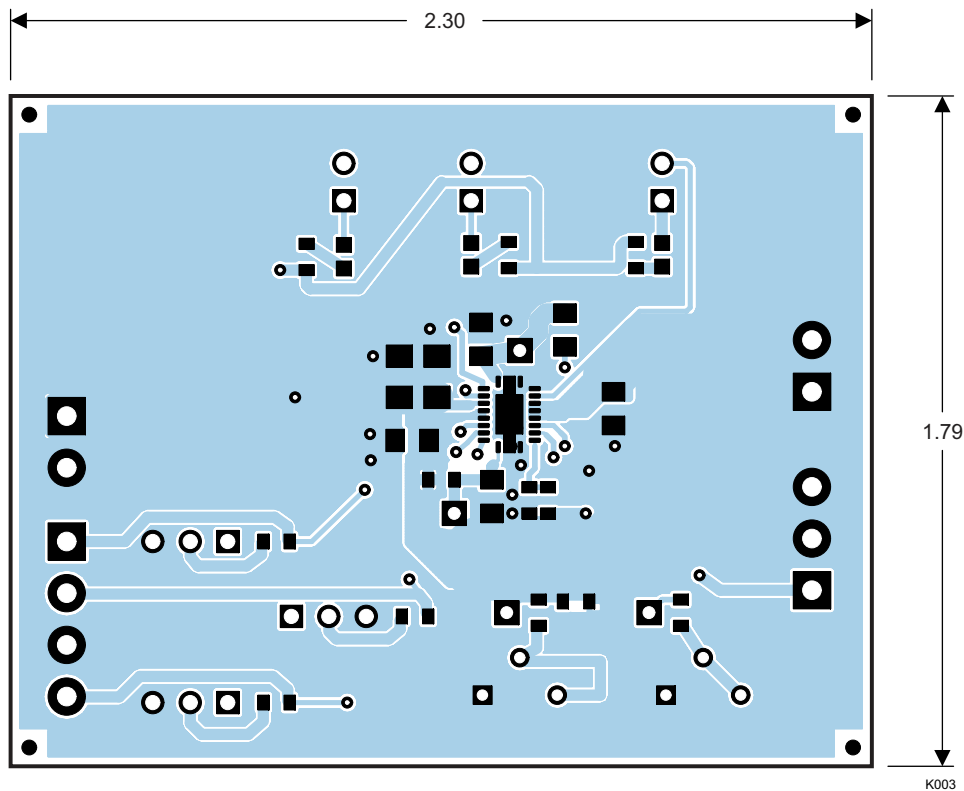


Figure 5. Board Layout – Top Etch Layer

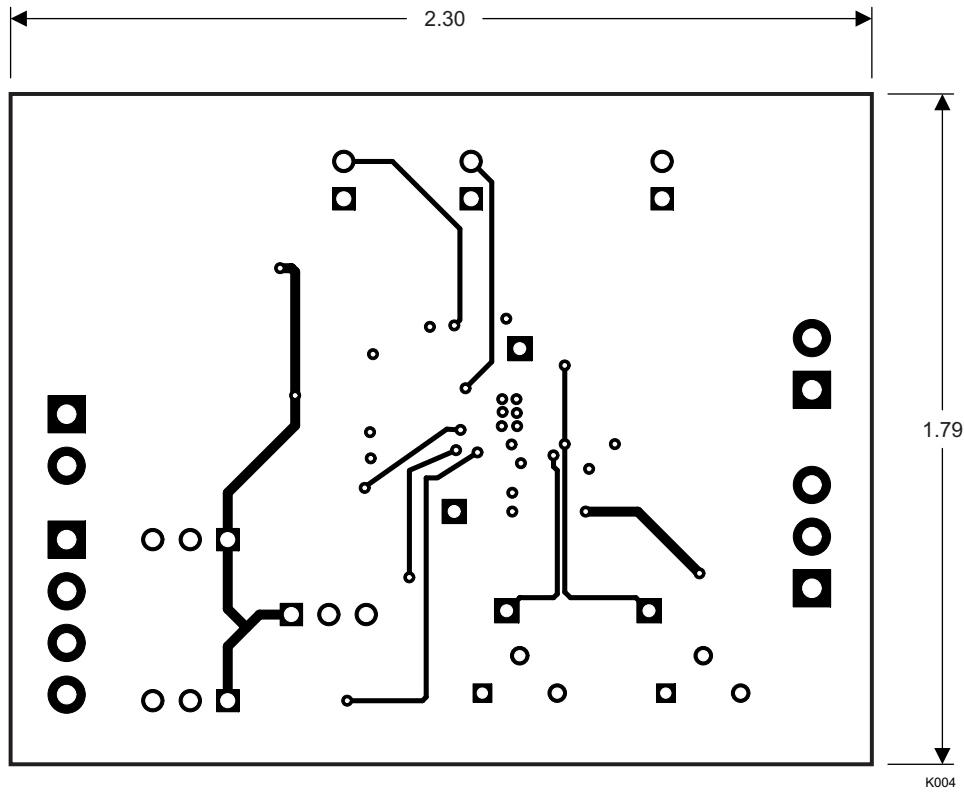


Figure 6. Board Layout – Second Etch Layer

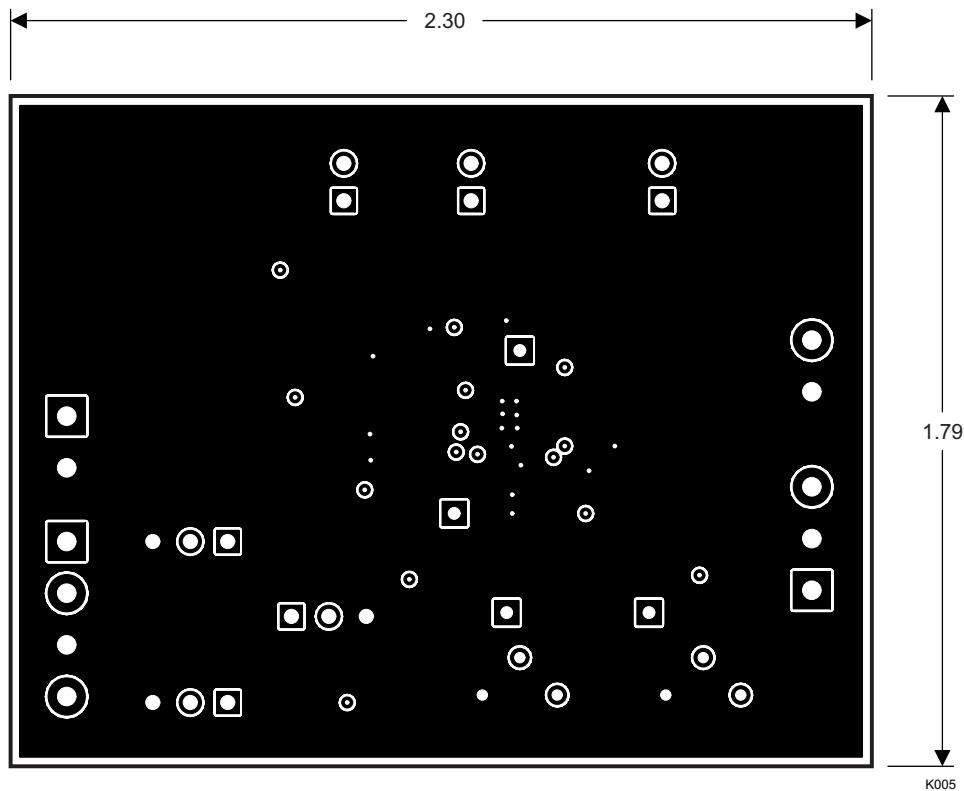


Figure 7. Board Layout – Third Etch Layer

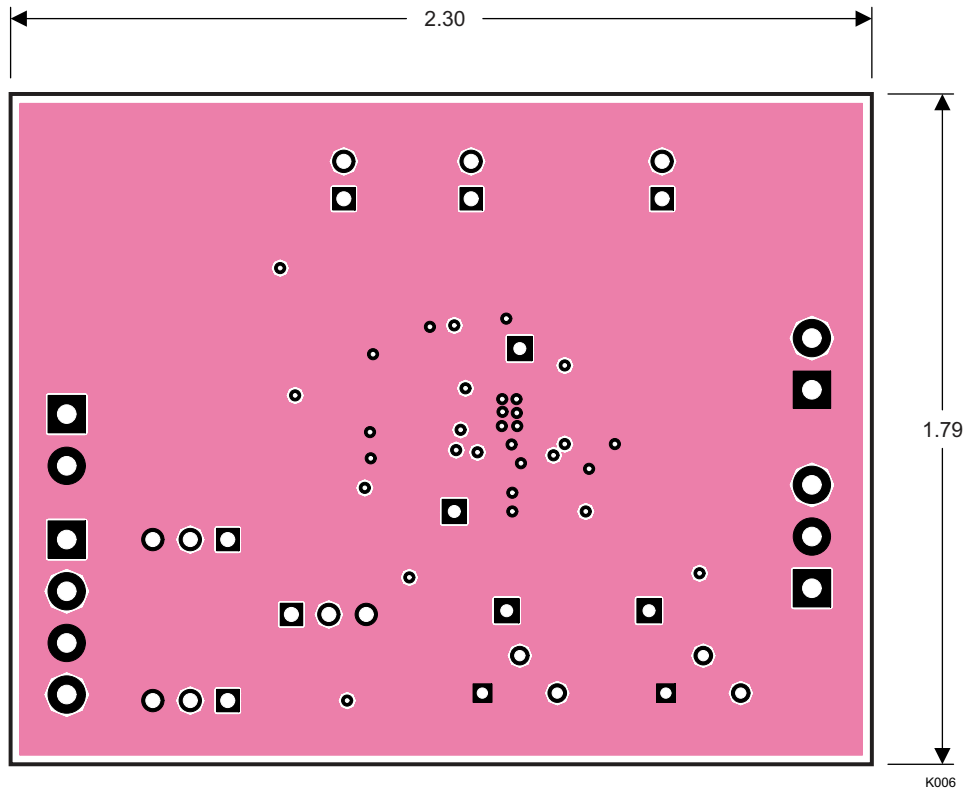


Figure 8. Board Layout – Bottom Etch Layer

7 Bill of Materials

Table 2. Bill of Materials

REFDES		QTY	VALUE	DESCRIPTION	SIZE	MFR	PART NUMBER
-001	-002						
C1	C1	1	0.01 μ F	Capacitor, ceramic, 0.01- μ F, 16-V, X7R, 10%	0603	Std	Std
C2, C3	C2, C3	2	10 μ F	Capacitor, ceramic, 10- μ F, 6.3-V, X5R, 20%	0805	Panasonic	ECJ-2FB0J106M
C4, C5	C4, C5	2	10 μ F	Capacitor, ceramic, 10- μ F, 25-V, X5R, 20%	1206	Panasonic	ECJ-3YB1E106M
C6	C6	1	0.47 μ F	Capacitor, ceramic, 0.47- μ F, 16-V, X7R, 10%	0805	Panasonic	ECJ-2YB1C474K
C7	C7	0	0.22 μ F	Capacitor, ceramic, 0.22- μ F, 10-V, X5R, 10%	0603	muRata	ECJ-1VB1A224K
D1, D2	D1, D2	2	Green	Diode, LED, green, 2.1-V, 20-mA, 6-mcd	0603	Liteon	160-1183-1-ND
D3	D3	1	Red	Diode, LED, red, 1.8-V, 20-mA, 20-mcd	0603	Liteon	160-1181-1-ND
J1, J4	J1, J4	2	ED1514	Terminal block, 2-pin, 6-A, 3,5-mm	0.27 inch \times 0.25 inch	OST	ED1514
J2	J2	1	ED1515	Terminal block, 3-pin, 6-A, 3,5-mm	0.41 inch \times 0.25 inch	OST	ED1515
J3	J3	1	ED1516	Terminal block, 4-pin, 6-A, 3,5-mm	0.55 inch \times 0.25 inch	OST	ED1516
JMP1, JMP2, JMP3 ⁽¹⁾	JMP1, JMP2, JMP3 ⁽¹⁾	3	PTC36SAA N	Header, 3-pin, 100-mil spacing, (36-pin strip)	0.100 inch \times 3	Sullins	PTC36SAAN
JMP4, JMP5, JMP6 ⁽¹⁾	JMP4, JMP5, JMP6 ⁽¹⁾	3	PTC36SAA N	Header, 2-pin, 100-mil spacing, (36-pin strip)	0.100 inch \times 2	Sullins	PTC36SAAN
R1, R2, R8	R1, R2, R8	3	1.5 k Ω	Resistor, chip, 1.5-k Ω , 1/16-W, 1%	0603	Std	Std
R3, R4, R5	R3, R4, R5	3	100 k Ω	Resistor, Chip, 100-k Ω , 1/16-W, 1%	0603	Std	Std
R6	R6	1	1 k Ω	Resistor, chip, 1-k Ω , 1/10W, 1%	0805	Std	Std
R7	R7	0	1 k Ω	Resistor, chip, 1-k Ω , 1/10W, 1%	0805	Std	Std
R9	R9	1	10 k Ω	Resistor, chip, 10-k Ω , 1/16W, 1%	0603	Std	Std
R10	R10	1	0	Resistor, chip, 0- Ω , 1/16-W, 1%	0603	Std	Std
R11	R11	1	22.6 k Ω	Resistor, chip, 22.6-k Ω , 1/16-W, 1%	0603	Std	Std
R12	R12	1	20 k Ω	Potentiometer, 20-k Ω , 1/4-in. Cermet, 12-turn, top-adjust	0.25 inch \times 0.17 inch	Bourns	3266W-203
R13	R13	1	50 k Ω	Potentiometer, 50-k Ω , 1/4-in. Cermet, 12-turn, top-adjust	0.25 inch \times 0.17 inch	Bourns	3266W-503
R14	R14	1	30.1 k Ω	Resistor, chip, 30.1-k Ω , 1/16-W, 1%	0603	Std	Std
TP1, TP2, TP3, TP4	TP1, TP2, TP3, TP4	4		Test point, 0.032-inch hole		Void	None
U1		1	bq24070R HL	IC, single-IC charge and system power-path management	QFN	TI	bq24070RHL
	U1	1	bq24071R HL	IC, single-IC charge and system power-path management	QFN	TI	bq24071RHL
—	—	1		PCB, 2-inch \times 1-inch \times 0.031-inch		Any	HPA180_PCB
6	6	6	N/A	Shunt, 100-mil, black	0.100-inch	3M	929950-00

⁽¹⁾ Add shunt to JMP1-0.5, JMP2-AC, JMP3-EN, JMP4-1/2, JMP5-1/2, JMP6-1/2.

8 References

1. *bq24070 Single-Chip Charge and System Power-Path Management IC* data sheet, [SLUS694](#)
2. *bq24071 Single-Chip Charge and System Power-Path Management IC* data sheet, [SLUS713](#)

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 6.5 V and the output voltage range of 0 V to 6.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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