CY7B9911
RoboClock+™
Programmable Skew Clock Buffer

Features

- All Output Pair Skew <100 ps Typical (250 max)
- 3.75 MHz to 100 MHz Output Operation
- User Selectable Output Functions
  - Selectable Skew to 18 ns
  - Inverted and Non-inverted
  - Operation at ½ and ¼ Input Frequency
  - Operation at 2x and 4x Input Frequency (input as low as 3.75 MHz)
- Zero Input to Output Delay
- 50% Duty Cycle Outputs
- Outputs Drive 50Ω terminated lines
- Low Operating Current
- 32-pin PLCC/LCC Package
- Jitter <200 ps Peak-to-peak (<25 ps RMS)

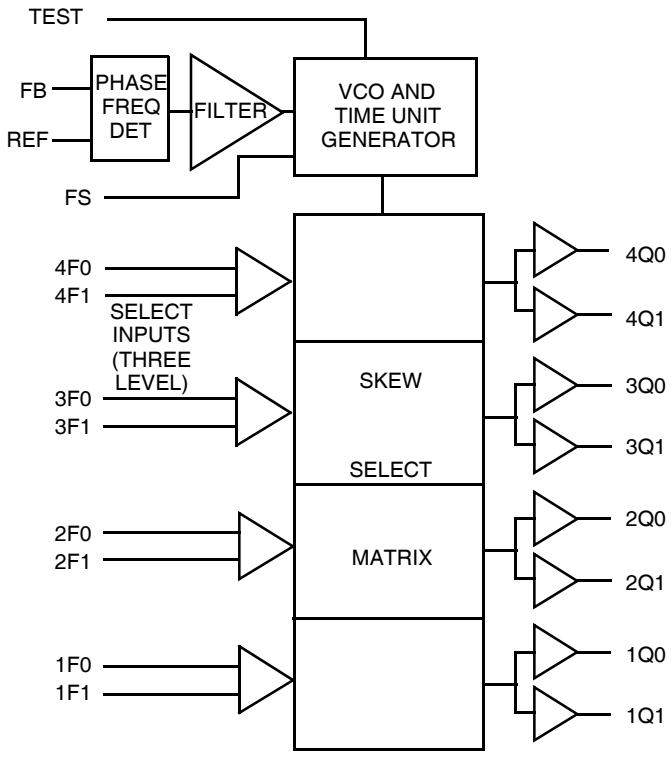
Functional Description

The CY7B9911 High Speed Programmable Skew Clock Buffer (PSCB) offers user selectable control over system clock functions. This multiple output clock driver provides the system integrator with functions necessary to optimize the timing of high performance computer systems. Each of the eight individual TTL drivers, arranged in four pairs of user controllable outputs, can drive terminated transmission lines with impedances as low as 50Ω. They deliver minimal and specified output skews and full swing logic levels.

Each output is hardwired to one of nine delay or function configurations. Delay increments of 0.6 to 1.5 ns are determined by the operating frequency with outputs able to skew up to ±6 time units from their nominal “zero” skew position. The completely integrated PLL allows cancellation of external load and transmission line delay effects. When this “zero delay” capability of the PSCB is combined with the selectable output skew functions, you can create output-to-output delays of up to ±12 time units.

Divide-by-two and divide-by-four output functions are provided for additional flexibility in designing complex clock systems. When combined with the internal PLL, these divide functions enable distribution of a low frequency clock that is multiplied by two or four at the clock destination. This facility minimizes clock distribution difficulty enabling maximum system clock speed and flexibility.

Logic Block Diagram



Contents

Pin Configuration

Figure 1. Pin Configuration – 32-Pin PLCC/LCC Package

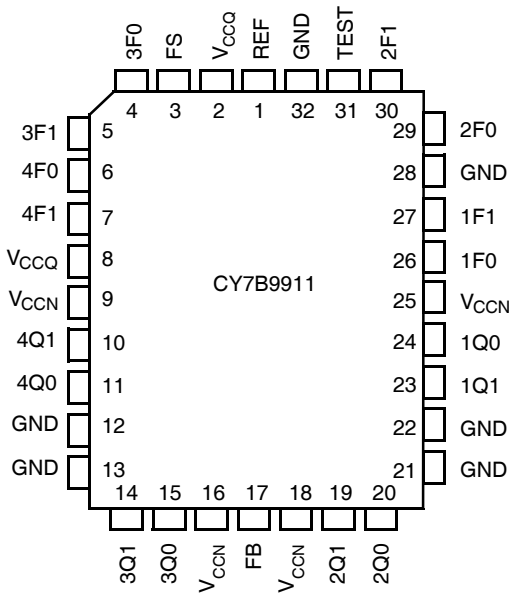


Table 1. Pin Definition

Signal Name	IO	Description
REF	I	Reference frequency input. This input supplies the frequency and timing against which all functional variation is measured.
FB	I	PLL feedback input (typically connected to one of the eight outputs).
FS	I	Three level frequency range select. See Table 2.
1F0, 1F1	I	Three level function select inputs for output pair 1 (1Q0, 1Q1). See Table 3.
2F0, 2F1	I	Three level function select inputs for output pair 2 (2Q0, 2Q1). See Table 3
3F0, 3F1	I	Three level function select inputs for output pair 3 (3Q0, 3Q1). See Table 3
4F0, 4F1	I	Three level function select inputs for output pair 4 (4Q0, 4Q1). See Table 3
TEST	I	Three level select. See test mode section under the block diagram descriptions.
1Q0, 1Q1	O	Output pair 1. See Table 3.
2Q0, 2Q1	O	Output pair 2. See Table 3.
3Q0, 3Q1	O	Output pair 3. See Table 3.
4Q0, 4Q1	O	Output pair 4. See Table 3.
V_{CCN}	PWR	Power supply for output drivers.
V_{CCQ}	PWR	Power supply for internal circuitry.
GND	PWR	Ground.

Block Diagram Description

Phase Frequency Detector and Filter

The Phase Frequency Detector and Filter blocks accept inputs from the reference frequency (REF) input and the feedback (FB) input. They generate correction information to control the frequency of the Voltage controlled Oscillator (VCO). These blocks, along with the VCO, form a Phase Locked Loop (PLL) that tracks the incoming REF signal.

VCO and Time Unit Generator

The VCO accepts analog control inputs from the PLL filter block and generates a frequency that is used by the time unit generator to create discrete time units that are selected in the skew select matrix. The operational range of the VCO is determined by the FS control pin. The time unit (t_U) is determined by the operating frequency of the device and the level of the FS pin as shown in Table 2.

Table 2. Frequency Range Select and t_U Calculation[1]

FS[2,3]	f_{NOM} (MHz)		$t_U = \frac{1}{f_{NOM} \times N}$ where N =	Approximate Frequency (MHz) At Which t_U = 1.0 ns
	Min	Max		
LOW	15	30	44	22.7
MID	25	50	26	38.5
HIGH	40	100	16	62.5

Skew Select Matrix

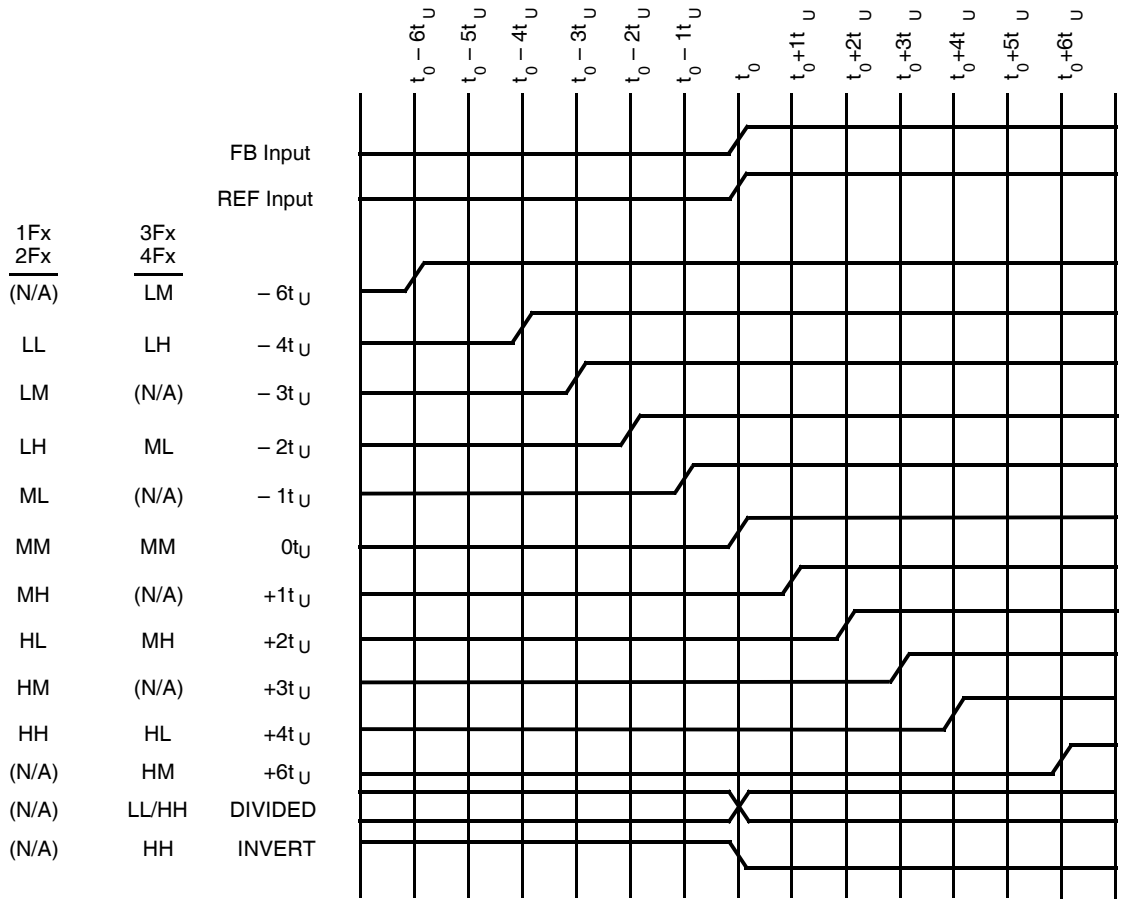
The skew select matrix contains four independent sections. Each section has two low skew, high fanout drivers (xQ0, xQ1), and two corresponding three level function select (xF0, xF1) inputs. Table 3 shows the nine possible output functions for each section as determined by the function select inputs. All times are measured with respect to the REF input assuming that the output connected to the FB input has $0t_U$ selected.

Table 3. Programmable Skew Configurations[1]

Function Selects		Output Functions		
1F1, 2F1, 3F1, 4F1	1F0, 2F0, 3F0, 4F0	1Q0, 1Q1, 2Q0, 2Q1	3Q0, 3Q1	4Q0, 4Q1
LOW	LOW	$-4t_U$	Divide by 2	Divide by 2
LOW	MID	$-3t_U$	$-6t_U$	$-6t_U$
LOW	HIGH	$-2t_U$	$-4t_U$	$-4t_U$
MID	LOW	$-1t_U$	$-2t_U$	$-2t_U$
MID	MID	$0t_U$	$0t_U$	$0t_U$
MID	HIGH	$+1t_U$	$+2t_U$	$+2t_U$
HIGH	LOW	$+2t_U$	$+4t_U$	$+4t_U$
HIGH	MID	$+3t_U$	$+6t_U$	$+6t_U$
HIGH	HIGH	$+4t_U$	Divide by 4	Inverted

Notes
1. For all three state inputs, HIGH indicates a connection to VCC, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to VCC/2.
2. The level to be set on FS is determined by the “normal” operating frequency (fNOM) of the VCO and Time Unit Generator (see Logic Block Diagram). Nominal frequency (fNOM) always appears at 1Q0 and the other outputs when they are operated in their undivided modes (see Table 3). The frequency appearing at the REF and FB inputs are fNOM when the output connected to FB is undivided. The frequency of the REF and FB inputs are fNOM/2 or fNOM/4 when the part is configured for a frequency multiplication by using a divided output as the FB input.
3. When the FS pin is selected HIGH, the REF input must not transition upon power-up until VCC has reached 4.3V.

Figure 2. Typical Outputs with FB Connected to a Zero-Skew Output[4]



Test Mode

The TEST input is a three level input. In normal system operation, this pin is connected to ground, enabling the CY7B9911 to operate as explained in the previous section (for testing purposes). Any of the three level inputs can have a removable jumper to ground or be tied LOW through a 100Ω resistor. This enables an external tester to change the state of these pins.

If the TEST input is forced to its MID or HIGH state, the device operates with its internal phase locked loop disconnected, and input levels supplied to REF directly control all outputs. Relative output to output functions are the same as in normal mode.

In contrast with normal operation (TEST tied LOW), all outputs function based only on the connection of their own function select inputs (xF0 and xF1) and the waveform characteristics of the REF input.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

Output Current into Outputs (LOW)..... 64 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch Up Current ..... >200 mA

Note
4. FB connected to an output selected for “zero” skew (i.e., xF1 = xF0 = MID).

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	CY7B9911 Min	CY7B9911 Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –16 mA	2.4		V
		V_{CC} = Min, I_{OH} =–40 mA			
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 46 mA		0.45	V
		V_{CC} = Min, I_{OL} = 46 mA			
V_{IH}	Input HIGH Voltage (REF and FB inputs only)		2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (REF and FB inputs only)		–0.5	0.8	V
V_{IHH}	Three Level Input HIGH Voltage (Test, FS, xFn)[5]	Min £ V_{CC} £ Max	V_{CC} – 0.85	V_{CC}	V
V_{IMM}	Three Level Input MID Voltage (Test, FS, xFn)[5]	Min £ V_{CC} £ Max	V_{CC}/2 – 500 mV	V_{CC}/2 + 500 mV	V
V_{ILL}	Three Level Input LOW Voltage (Test, FS, xFn)[5]	Min £ V_{CC} £ Max	0.0	0.85	V
I_{IH}	Input HIGH Leakage Current (REF and FB inputs only)	V_{CC} = Max, V_{IN} = Max.		10	µA
I_{IL}	Input LOW Leakage Current (REF and FB inputs only)	V_{CC} = Max, V_{IN} = 0.4V	–500		µA
I_{IHH}	Input HIGH Current (Test, FS, xFn)	V_{IN} = V_{CC}		200	µA
I_{IMM}	Input MID Current (Test, FS, xFn)	V_{IN} = V_{CC}/2	–50	50	µA
I_{ILL}	Input LOW Current (Test, FS, xFn)	V_{IN} = GND		–200	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max, V_{OUT} = GND (25×C only)		–250	mA
I_{CCQ}	Operating Current Used by Internal Circuitry	V_{CCN} = V_{CCQ} = Max, All Input Selects Open — Com'l		85	mA
I_{CCN}	Output Buffer Current per Output Pair[6]	V_{CCN} = V_{CCQ} = Max, I_{OUT} = 0 mA Input Selects Open, f_{MAX}		14	mA
PD	Power Dissipation per Output Pair[8]	V_{CCN} = V_{CCQ} = Max, I_{OUT} = 0 mA Input Selects Open, f_{MAX}		78	mW

Notes

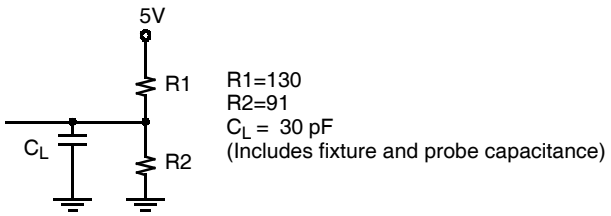
5. These inputs are normally wired to VCC, GND, or left unconnected (actual threshold voltages vary as a percentage of VCC). Internal termination resistors hold unconnected inputs at VCC/2. If these inputs are switched, the function and timing of the outputs glitch and the PLL requires an additional tLOCK time before all datasheet limits are achieved.
6. CY7B9911 must be tested one output at a time, output shorted for less than one second, less than 10% duty cycle. Room temperature only.
7. Total output current per output pair is approximated by the following expression that includes device current plus load current:
   CY7B9911:ICCN = [(4 + 0.11F) + [((835 – 3F)/Z) + (.0022FC)]N] x 1.1
   Where F = frequency in MHz; C = capacitive load in pF; Z = line impedance in ohms; N = number of loaded outputs; 0, 1, or 2; FC = F * C.
8. Total power dissipation per output pair is approximated by the following expression that includes device power dissipation plus power dissipation due to the load circuit: CY7B9911:PD = [(22 + 0.61F) + [((1550 – 2.7F)/Z) + (.0125FC)]N] x 1.1.

Capacitance

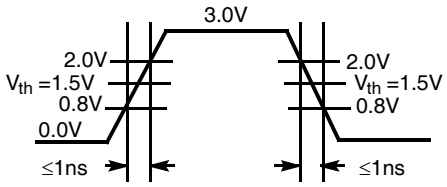
Test conditions assume signal transition times unless otherwise specified.

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF

Figure 3. AC Test Loads and Waveforms



TTL AC Test Load (CY7B9911)



TTL Input Test Waveform (CY7B9911)

Switching Characteristics

Over the Operating Range[2, 10]

Parameter	Description		CY7B9911–5			CY7B9911–7			Unit
			Min	Typ	Max	Min	Typ	Max	
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW[1, 2]	15		30	15		30	MHz
		FS = MID[1, 2]	25		50	25		50	
		FS = HIGH[1, 2, 3]	40		100	40		100	
t_{RPWH}	REF Pulse Width HIGH		4.0			4.0			ns
t_{RPWL}	REF Pulse Width LOW		4.0			4.0			ns
t_U	Programmable Skew Unit		See Table 2			See Table 2			
t_{SKEWPR}	Zero Output Matched Pair Skew (XQ0, XQ1)[11, 12]			0.1	0.25		0.1	0.25	ns
t_{SKEW0}	Zero Output Skew (All Outputs)[11, 13]			0.25	0.5		0.3	0.75	ns
t_{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs)[11, 14]			0.6	0.7		0.6	1.0	ns
t_{SKEW2}	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided)[11, 14]			0.5	1.2		1.0	1.7	ns
t_{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs)[11, 14]			0.5	0.9		0.7	1.4	ns
t_{SKEW4}	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted)[11, 14]			0.5	1.2		1.2	1.9	ns
t_{DEV}	Device-to-Device Skew[10, 15]				1.25			1.65	ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		–0.5	0.0	+0.5	–0.7	0.0	+0.7	ns
t_{ODCV}	Output Duty Cycle Variation[18]		–1.0	0.0	+1.0	–1.2	0.0	+1.2	ns
t_{PWH}	Output HIGH Time Deviation from 50%[17, 18]				2.0			2.5	ns
t_{PWL}	Output LOW Time Deviation from 50%[17, 18]				2.5			3	ns
t_{ORISE}	Output Rise Time[17, 19]		0.15	1.0	1.5	0.15	1.5	2.5	ns
t_{OFALL}	Output Fall Time[17, 19]		0.15	1.0	1.5	0.15	1.5	2.5	ns
t_{LOCK}	PLL Lock Time[20]				0.5			0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter	RMS[10]			25			25	ps
		Peak-to-Peak[10]			200			200	ps

Notes

9. Test conditions assume signal transition times of 2 ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
10. Guaranteed by statistical correlation. Tested initially and after any design or process changes that affect these parameters.
11. SKEW is defined as the time between the earliest and the latest output transition among all outputs for which the same t_U delay is selected when all are loaded with 30 pF and terminated with 50Ω to 2.06V.
12. t_{SKEWPR} is defined as the skew between a pair of outputs (XQ0 and XQ1) when all eight outputs are selected for $0t_U$.
13. t_{SKEW0} is defined as the skew between outputs when they are selected for $0t_U$. Other outputs are divided or inverted but not shifted.
14. There are three classes of outputs: Nominal (multiple of t_U delay), Inverted (4Q0 and 4Q1 only with 4F0 = 4F1 = HIGH), and Divided (3Qx and 4Qx only in Divide-by-2 or Divide-by-4 mode).
15. t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{CC} ambient temperature, air flow, and so on).
16. t_{ODCV} is the deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} specifications.
17. Specified with outputs loaded with 30 pF. Devices are terminated through 50Ω to 2.06V.
18. t_{PWH} is measured at 2.0V. t_{PWL} is measured at 0.8V.
19. t_{ORISE} and t_{OFALL} measured between 0.8V and 2.0V.
20. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

AC Timing Diagrams

Figure 4. AC Timing Diagrams

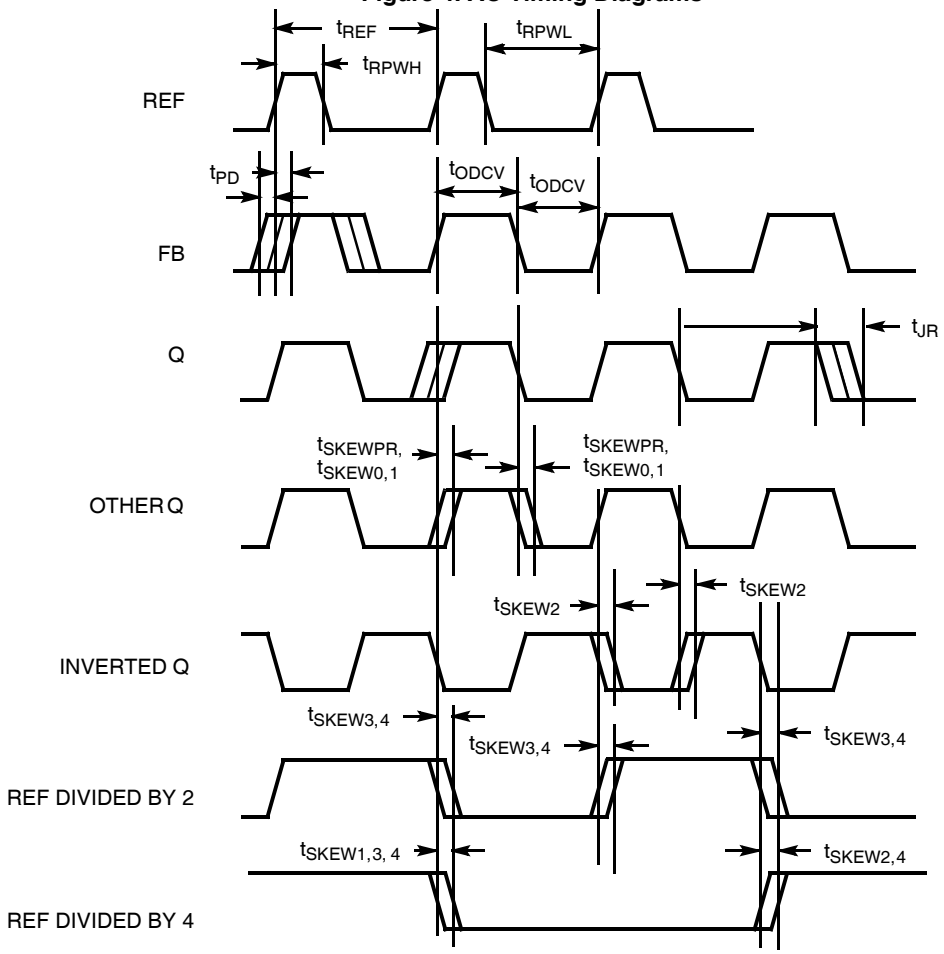
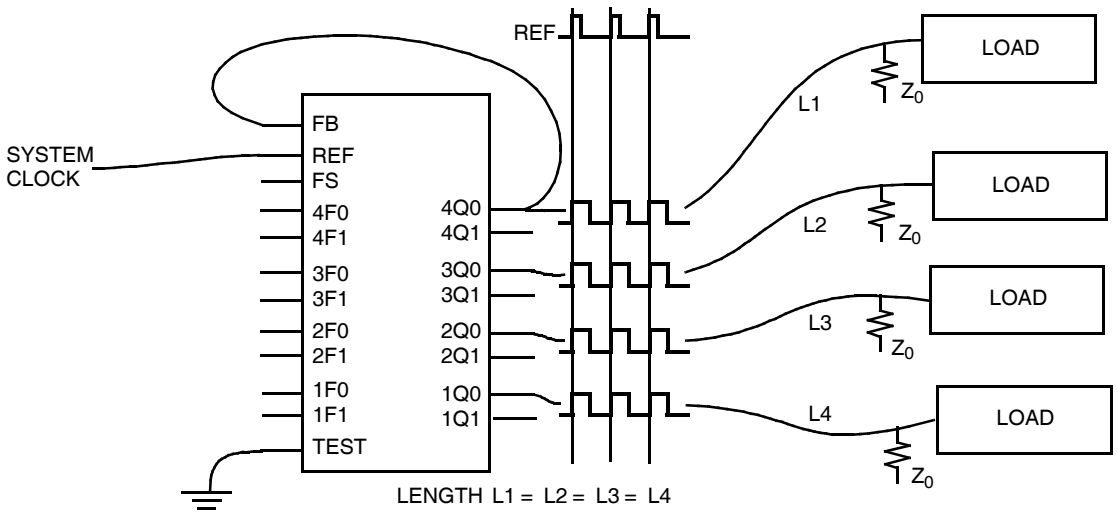


Figure 5. Zero Skew and Zero Delay Clock Driver



Operational Mode Descriptions

Figure 4 shows the PSCB configured as a zero skew clock buffer. In this mode the 7B9911 is used as the basis for a low skew clock distribution tree. When all of the function select inputs (xF0, xF1) are left open, the outputs are aligned and each drive a terminated transmission line to an independent load. The FB input is tied to any output in this configuration and the operating frequency range is selected with the FS pin. The low skew specification, coupled with the ability to drive terminated transmission lines (with impedances as low as 50 ohms), enables efficient printed circuit board design.

Figure 6. Programmable Skew Clock Driver

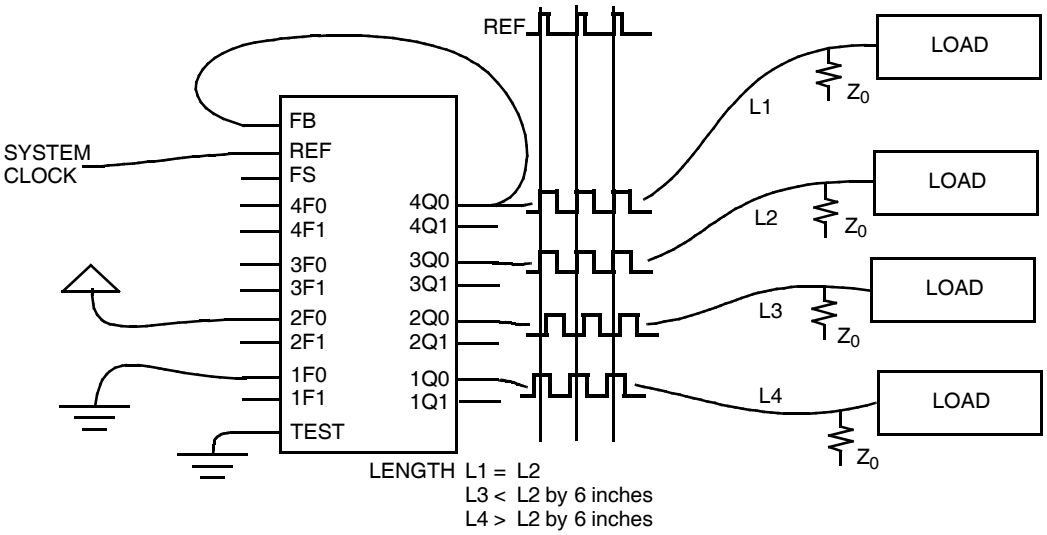


Figure 5 shows a configuration to equalize skew between metal traces of different lengths. In addition to low skew between outputs, the PSCB is programmed to stagger the timing of its outputs. The four groups of output pairs are each programmed to different output timing. Skew timing is adjusted over a wide range in small increments with the appropriate strapping of the function select pins. In this configuration the 4Q0 output is sent to FB and configured for zero skew. The other three pairs of outputs are programmed to yield different skews relative to the feedback. By advancing the clock signal on the longer traces or retarding the clock signal on shorter traces, all loads receive the clock pulse at the same time.

In this illustration the FB input is connected to an output with 0 ns skew (xF1, xF0 = MID) selected. The internal PLL synchronizes the FB and REF inputs and aligns their rising edges to make certain that all outputs have precise phase alignment.

Clock skews is advanced by ±6 time units (tU) when using an output selected for zero skew as the feedback. There is a wider range of delays, if the output connected to FB is also skewed. As “Zero Skew”, +tU, and –tU are defined relative to output groups and the PLL aligns the rising edges of REF and FB, wider output skews are created by proper selection of the xFn inputs. For example, a +10 tU between REF and 3Qx is achieved by connecting 1Q0 to FB and setting 1F0 = 1F1 = GND, 3F0 = MID, and 3F1 = High. (Since FB aligns at –4 tU and 3Qx skews to +6 tU, a total of +10 tU skew is realized.) Many other configurations are realized by skewing both the output used as the FB input and skewing the other outputs.

Figure 7. Inverted Output Connections

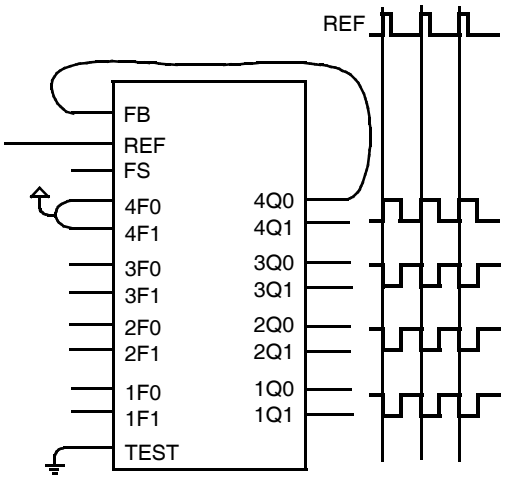


Figure 6 shows an example of the invert function of the PSCB. In this example the 4Q0 output used as the FB input is programmed for invert (4F0 = 4F1 = HIGH) while the other three pairs of outputs are programmed for zero skew. When 4F0 and 4F1 are tied high, 4Q0 and 4Q1 become inverted zero phase outputs. The PLL aligns the rising edge of the FB input with the rising edge of the REF. This causes the 1Q, 2Q, and 3Q outputs to become the “inverted” outputs with respect to the REF input. By selecting the output to connect to FB, you can have two inverted and six non-inverted outputs or six inverted and two

non-inverted outputs. The correct configuration is determined by the need for more (or fewer) inverted outputs. 1Q, 2Q, and 3Q outputs is also skewed to compensate for varying trace delays independent of inversion on 4Q.

Figure 8. Frequency Multiplier with Skew Connections

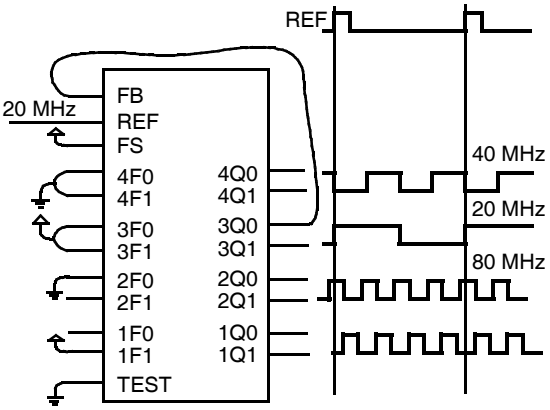


Figure 7 illustrates the PSCB configured as a clock multiplier. The 3Q0 output is programmed to divide by four and is sent back to FB. This causes the PLL to increase its frequency until the 3Q0 and 3Q1 outputs are locked at 20 MHz while the 1Qx and 2Qx outputs run at 80 MHz. The 4Q0 and 4Q1 outputs are programmed to divide by two, that results in a 40 MHz waveform at these outputs. Note that the 20 and 40 MHz clocks fall simultaneously and are out of phase on their rising edge. This enables the designer to use the rising edges of the 1⁄2 frequency and 1⁄4 frequency outputs without concern for rising edge skew. The 2Q0, 2Q1, 1Q0, and 1Q1 outputs run at 80 MHz and are skewed by programming their select inputs accordingly. Note that the FS pin is wired for 80 MHz operation because that is the frequency of the fastest output.

Figure 9. Frequency Divider Connections

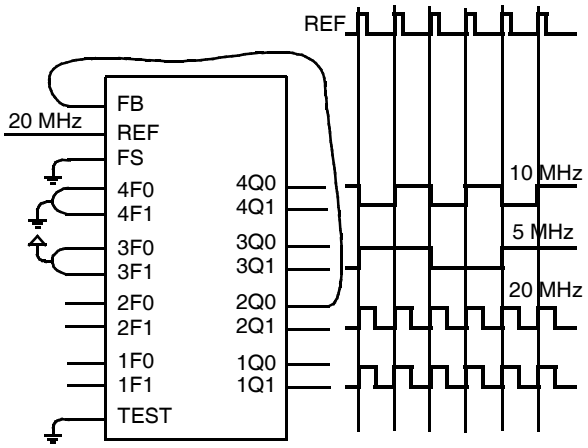


Figure 8 demonstrates the PSCB in a clock divider application. 2Q0 is fed back to the FB input and programmed for zero skew. 3Qx is programmed to divide by four. 4Qx is programmed to divide by two. Note that the falling edges of the 4Qx and 3Qx outputs are aligned. This enables use of the rising edges of the 1⁄2 frequency and 1⁄4 frequency without concern for skew mismatch. The 1Qx outputs are programmed to zero skew and are aligned with the 2Qx outputs. In this example, the FS input is grounded to configure the device in the 15 to 30 MHz range since the highest frequency output is running at 20 MHz.

Figure 9 shows some of the functions that are selectable on the 3Qx and 4Qx outputs. These include inverted outputs and outputs that offer divide-by-2 and divide-by-4 timing. An inverted output allows the system designer to clock different subsystems on opposite edges, without suffering from the pulse asymmetry typical of non-ideal loading. This function enables each of the two subsystems to clock 180 degrees out of phase, but still stay aligned within the skew specification.

The divided outputs offer a zero delay divider for portions of the system that divides the clock by either two or four, and still remain within a narrow skew of the “1X” clock. Without this feature, addition of an external divider is required and the propagation delay of the divider adds to the skew between the different clock signals.

These divided outputs, coupled with the Phase Locked Loop, enable the PSCB to multiply the clock rate at the REF input by either two or four. This mode enables the designer to distribute a low frequency clock between various portions of the system. It also locally multiplies the clock rate to a more suitable frequency, maintaining the low skew characteristics of the clock driver. The PSCB performs all of the functions described in this section at the same time. It can multiply by two and four or divide by two (and four) at the same time that it is shifting its outputs over a wide range or maintaining zero skew between selected outputs.

Figure 10. Multi-Function Clock Driver

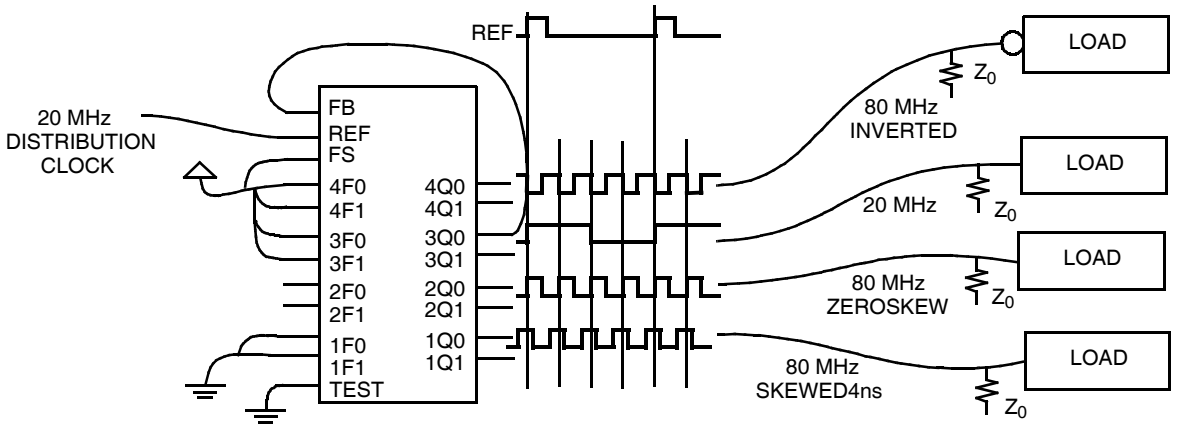


Figure 11. Board-to-Board Clock Distribution

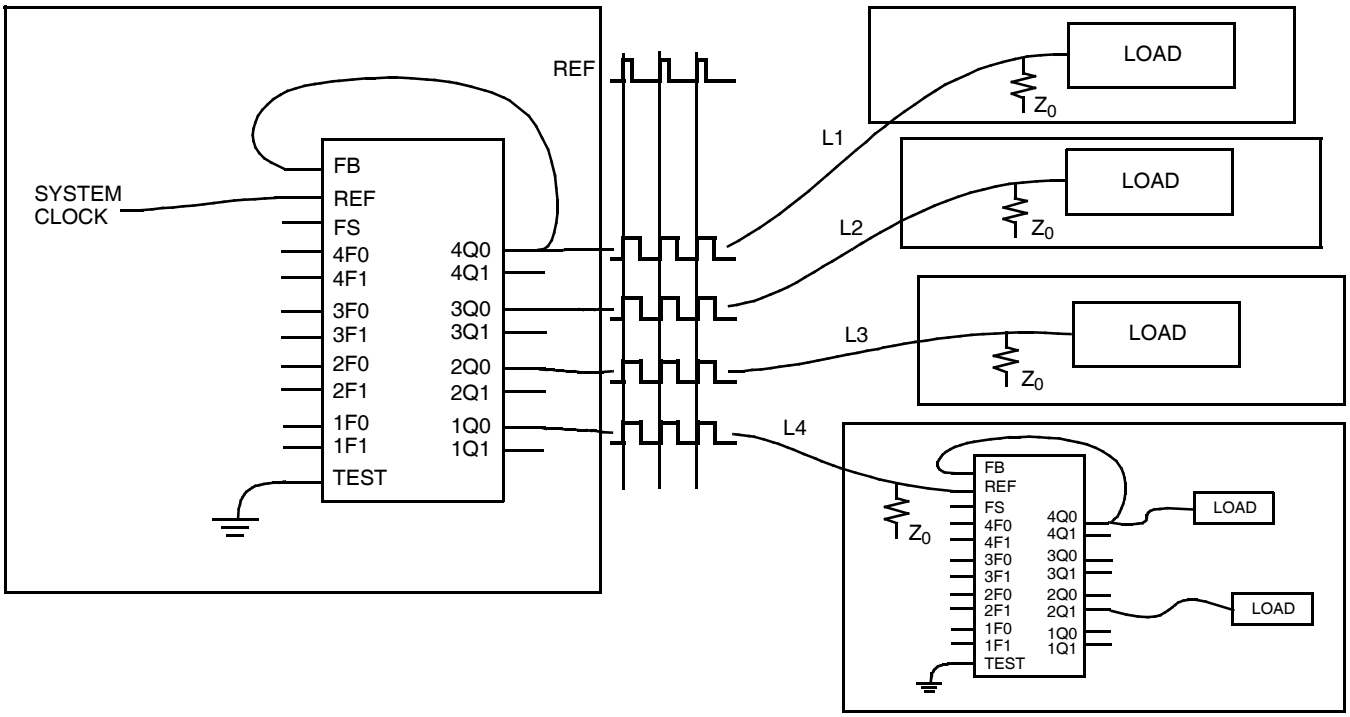
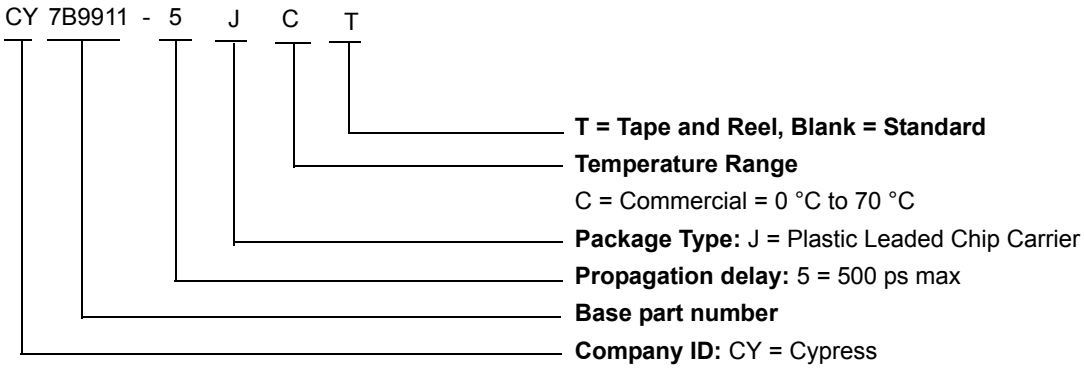


Figure 10 shows the CY7B9911 connected in series to construct a zero-skew clock distribution tree between boards. Delays of the downstream clock buffers are programmed to compensate for the wire length (that is, select negative skew equal to the wire delay) necessary to connect them to the master clock source, approximating a zero delay clock tree. Cascaded clock buffers accumulate low frequency jitter because of the non-ideal filtering characteristics of the PLL filter. Do not connect more than two clock buffers in series.

Ordering Information

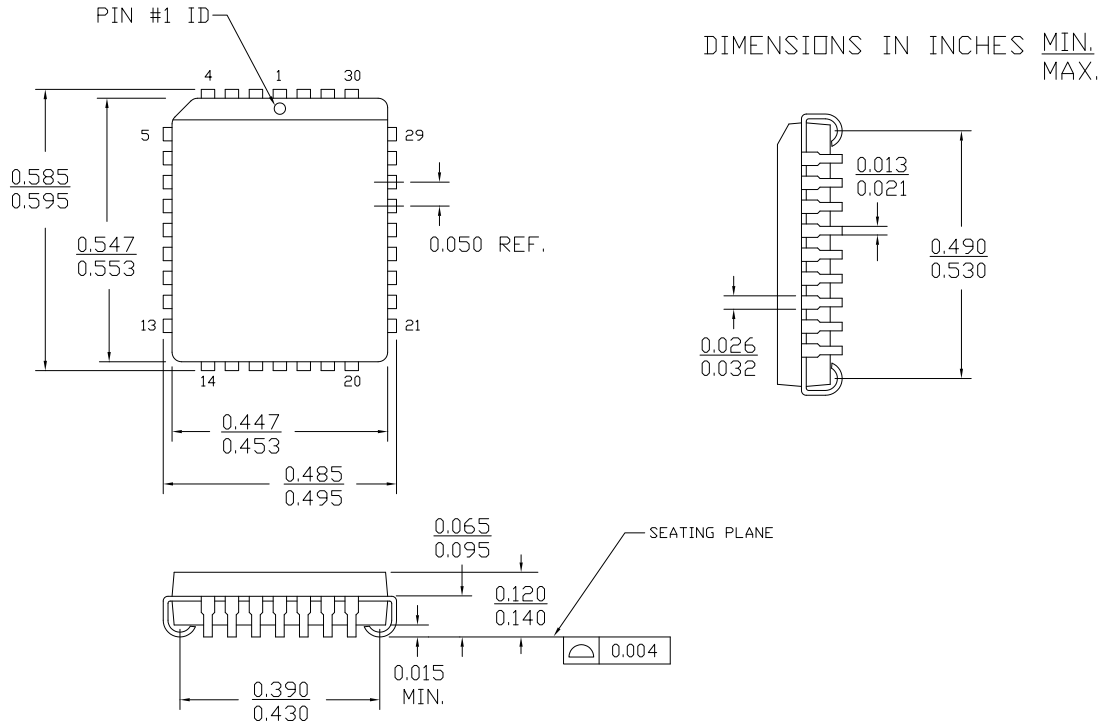
Accuracy (ps)	Ordering Code	Package Type	Operating Range
500	CY7B9911–5JC	32-pin Plastic Leaded Chip Carrier	Commercial
500	CY7B9911–5JCT	32-pin Plastic Leaded Chip Carrier - Tape and Reel	Commercial

Ordering Code Definitions



Package Diagram

Figure 12. 32-Pin Plastic Leaded Chip Carrier J65



51-85002 *C

Document History Page

Document Title: CY7B9911 RoboClock+™ Programmable Skew Clock Buffer Document Number: 38-07209				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110342	SZV	12/21/01	Change from Specification number: 38-00623 to 38-07209
*A	1199925	KVM/AESA	See ECN	Added Tape and Reel part in Ordering Information Added note: Not recommended for the new design
*B	1286064	AESA	See ECN	Change status to final
*C	2593494	CXQ/PYRS	10/20/08	Changed unit of measurement in the Electrical Characteristics table for parameters I_{IH}, I_{IL}, I_{IHH}, I_{IMM}, and I_{ILL}
*D	2761988	CXQ	09/10/09	Changed “Pb” to “lead” in package type section of Ordering Information.
*E	2894070	CXQ	03/17/2010	Added Table of Contents Removed part number CY7B9911–7JC in Ordering Information. Removed Note “Not recommended for the new design.” Updated Package Diagram (Figure 12) Updated Sales, Solutions, and Legal Information
*F	3076920	CXQ	11/02/2010	Added Ordering Code Definitions.

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