2-wire Serial Interface Lens Driver For Voice Coil Motor

BU64244GWZ BU64249GWX

General Description

The BU64244GWZ and BU64249GWX are designed to drive voice coil motor (VCM). The drivers include ISRC (intelligent slew rate control) to reduce mechanical ringing to optimize the camera's auto focus capabilities.

Features

- 2.3V min driver power supply.
- Current sink output.
- 10 bit resolution current control.
- ISRC mechanical ringing compensation.
- 2-wire serial interface.
- Integrated current sense resistor

Applications

- Autofocus in mobile camera modules.
- Driving VCM actuators.

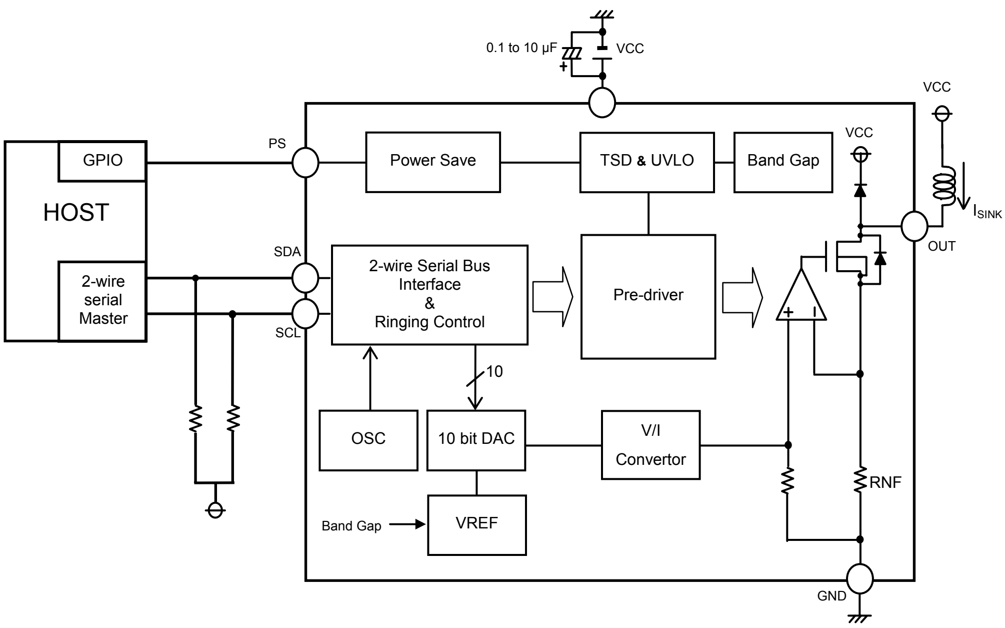
Key Specifications

Power Supply Voltage Range:	2.3V to 4.8V
Standby Current:	0μA (Typ)
Internal Resistance:	1.5Ω(Typ)
Master Clock:	400kHz(Typ)
Output Maximum Current:	130mA(Typ)
Operating Temperature Range:	-25°C to +85°C

Packages W(Typ) x D(Typ) x H(Max)

- BU64244GWZ(UCSP35L1)
  0.77 mm × 1.30 mm × 0.36 mm
- BU64249GWZ(UCSP11X1)
  1.30 mm × 0.77 mm × 0.145 mm

Typical Application Circuit



○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configurations

	1	2
A	OUT	PS
B	GND	SDA
C	VCC	SCL

BU64244GWZ

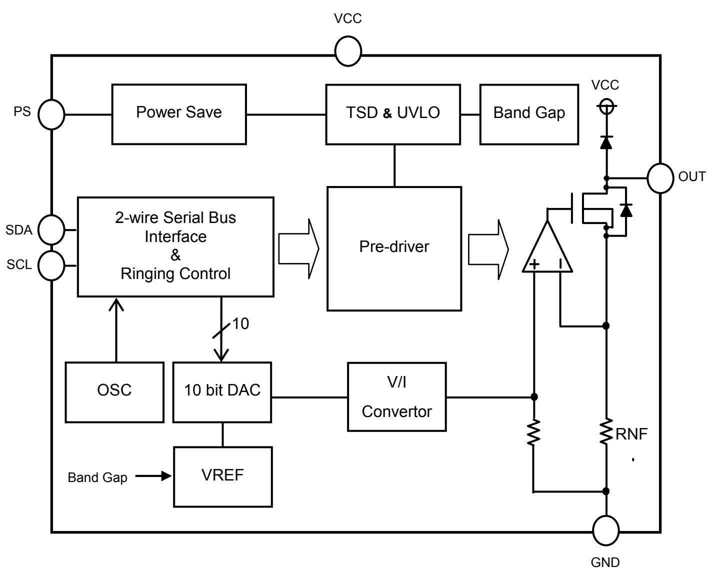
	1	2	3
A	PS	SDA	SCL
B	OUT	GND	VCC

BU64249GWX

Pin Descriptions

Pin Name	Function
PS	Power save
SDA	Serial data input
SCL	Serial clock input
OUT	Current output
GND	Ground
VCC	Power supply voltage

Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{CC}	-0.5 to +5.5	V
Power save input voltage	V_{PS}	-0.5 to +5.5	V
Control input voltage	V_{IN}	-0.5 to +5.5	V
Power dissipation 1 (BU64244GWZ)	P_{d1}	0.33 (Note 1)	W
Power dissipation 2 (BU64249GWX)	P_{d2}	0.2 (Note 2)	W
Operating temperature range	T_{opr}	-25 to +85	°C
Junction temperature	T_{jmax}	125	°C
Storage temperature range	T_{stg}	-55 to +125	°C
Output current	I_{OUT}	+200	mA

(Note 1) Derating in done 3.3 mW/°C for operating above Ta≧25°C (Mount on 8-layer 50.0mm x 58.0mm x 1.75mm board)
(Note 2) Derating in done 2.0 mW/°C for operating above Ta≧25°C (Mount on 8-layer 50.0mm x 58.0mm x 1.75mm board)
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta= -25°C to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	2.3	3.0	4.8	V
Power save input voltage	V_{PS}	0.0	-	4.8	V
Control input voltage	V_{IN}	0.0	-	4.8	V
2-wire serial interface frequency	f_{CLK}	-	-	400	kHz
Output current (Note 3)	I_{OUT}	-	-	200	mA

(Note 3) Pd, ASO should not be exceeded

Electrical Characteristics (Unless otherwise specified VCC=3V Ta=25°C)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Power Consumption						
Standby current	ICCST	-	0	5	μA	Power save pin = L = VPSL
Circuit current	ICC	-	0.6	1.0	mA	Power save pin = H = VPSH 2-wire serial PS bit = 1, SCL = 400 kHz
Power Save Input (VPS = PS)						
High level input voltage	VPSH	1.26	-	VCC	V	
Low level input voltage	VPSL	0	-	0.5	V	
High level input current	IPSH	- 10	-	10	μA	VPS = 3 V
Low level input current	IPSL	- 10	-	10	μA	VPS = 0 V
Control Input (VIN = SCL, SDA)						
High level input voltage	VINH	1.26	-	VCC	V	
Low level input voltage	VINL	0	-	0.5	V	
Low level output voltage	VINOL	-	-	0.4	V	IIN = + 3.0 mA (SDA)
High level input current	IINH	- 10	-	10	μA	Input voltage = 0.9 x VIN
Low level input current	IINL	- 10	-	10	μA	Input voltage = 0.1 x VIN
Under Voltage Lock Out						
UVLO voltage	VUVLO	1.6	-	2.2	V	
Master Clock						
MCLK frequency	MCLK	- 5	-	5	%	MCLK = 400 kHz
10 Bit D/A Converter (for Controlling Output Current)						
Resolution	DRES	-	10	-	bits	
Differential nonlinearity	DNL	- 1	-	1	LSB	
Integral nonlinearity	INL	- 4	-	4	LSB	
Output Current Performance						
Output current resolution	IORES	-	126	-	μA	Per 1 DAC code step
Output maximum current	IOMAX	117	130	143	mA	DAC_code = 0x3FF
Zero code offset current	IOOFS	0	1	5	mA	DAC_code = 0x000
Output voltage	VOUT	-	150	200	mV	Output current = 100 mA
Maximum applied voltage	VOMAX	-	-	VCC	V	
Output resistance	ROUT	-	1.5	2.0	Ω	

Typical Performance Curves

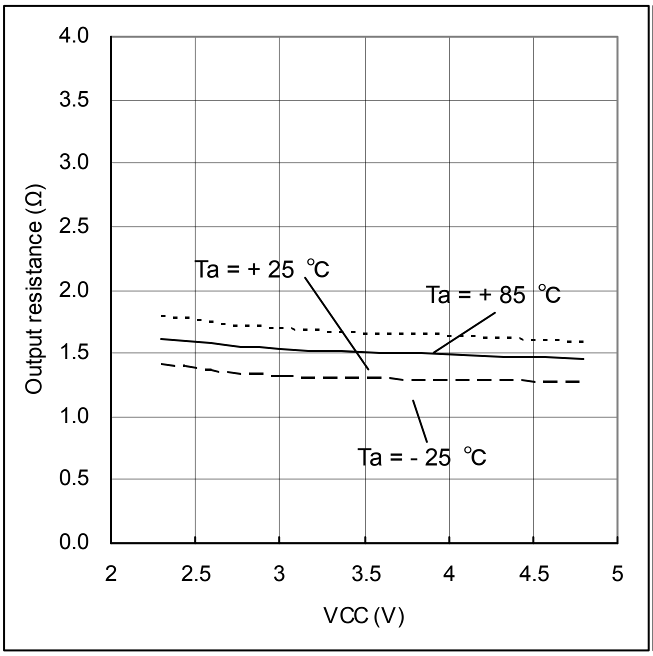


Figure 1. Output resistance vs. VCC voltage

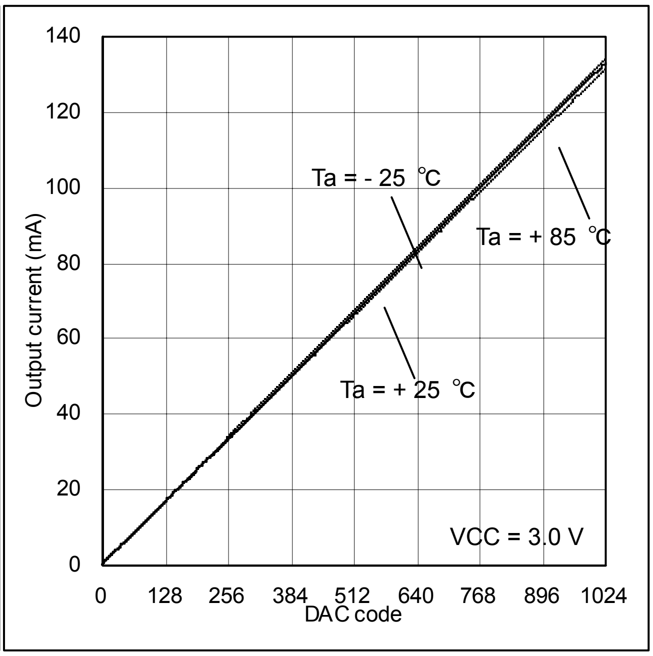


Figure 2. Output current vs. DAC code

Typical Performance Curves - continued

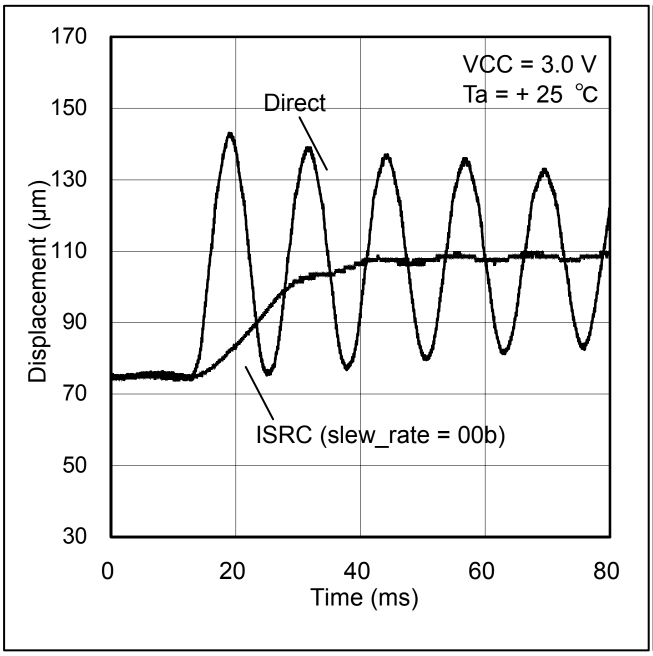


Figure 3. Displacement vs. settling time
(slew_rate = 00b)

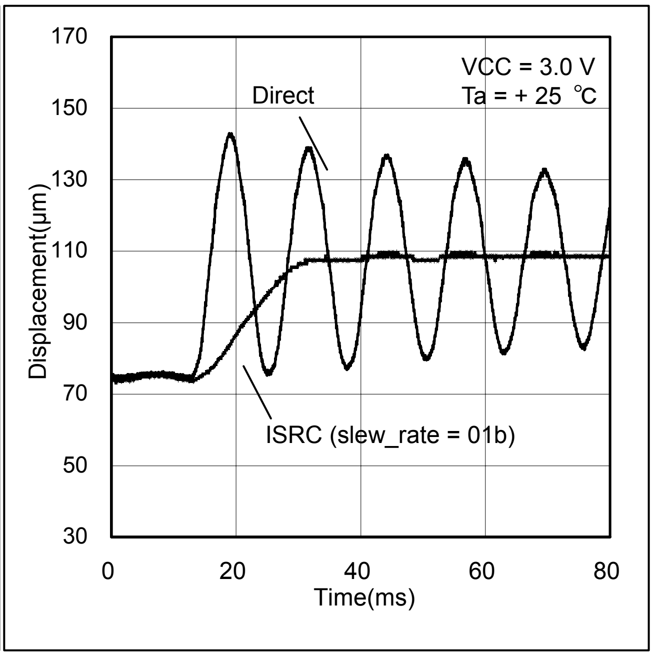


Figure 4. Displacement vs. settling time
(slew_rate = 01b)

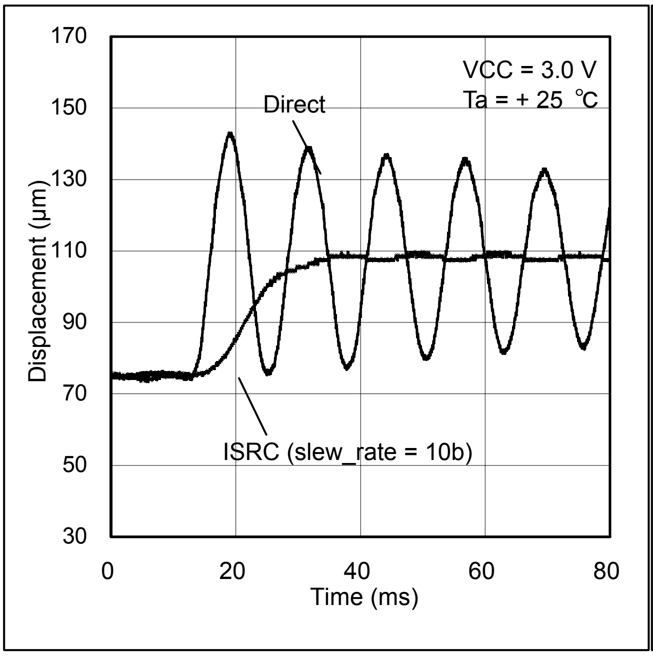


Figure 5. Displacement vs. settling time
(slew_rate = 10b)

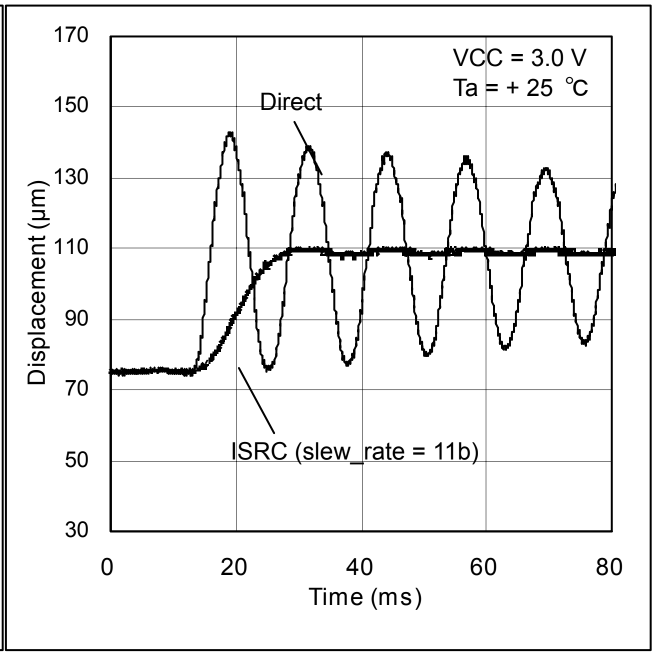
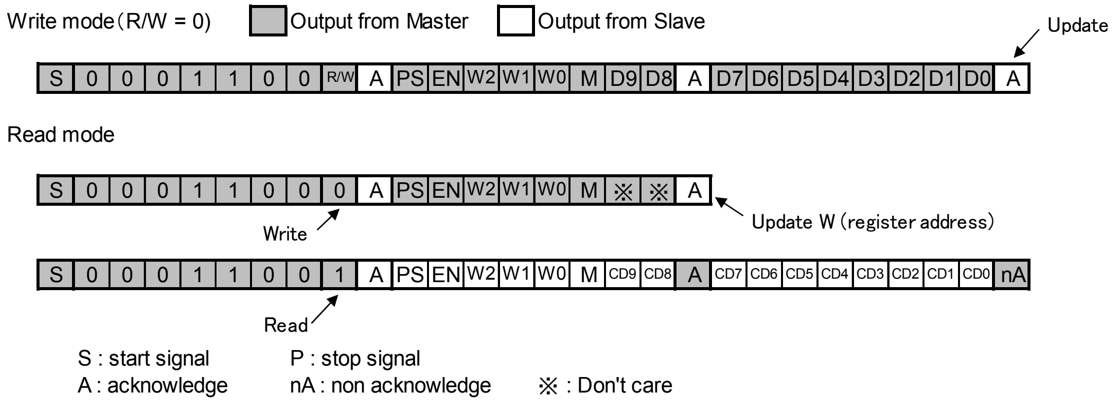


Figure 6. Displacement vs. settling time
(slew_rate = 11b)

2-wire serial BUS Format (Fast mode SCL = 400 kHz)



Register name	Setting item	Description
R/W	Read/Write mode	0 = Write mode (0x18 address), 1 = Read mode (0x19 address)
PS	Serial power save	0 = Driver in standby mode, 1 = Driver in operating mode
EN	Driver output status	0 = Output is Hi-Z 1 = Constant current sink/sequence start
M	Mode select	M=0=ISRC mode disabled M=1=ISRC mode enabled
W2W1W0	Register address	000b = Output current setting
		001b = Parameter setting 1
		010b = Parameter setting 2
		011b = Parameter setting 3
		100b = Parameter setting 4
D9 to D0	Data bits	Register data

Register Update Timing

PS – Register is updated during the 2nd ACK response during a 3 byte 2-wire serial command
EN – Register is updated during the 3rd ACK response during a 3 byte 2-wire serial command
Wx – Register is updated during the 2nd ACK response during a 3 byte 2-wire serial command
M – Register is updated during the 3rd ACK response during a 3 byte 2-wire serial command
Dx – Register is updated during the 3rd ACK response during a 3 byte 2-wire serial command

Note: Setting the external power save pin = VPSL (typically 0 V) will reset all 2-wire serial registers to 0

Register Map

Address	Bit	Bit Name	Function
000b	D[9:0]	C_DAC[9:0]	Point C DAC code setting[9:0]
001b	D[9:8]		
	D[7:3]	rf[4:0]	Resonant frequency setting[4:0]
	D2		
	D[1:0]	slew_rate[1:0]	Slew rate speed setting[1:0]
010b	D[9:0]	A_DAC[9:0]	Point A DAC code setting[9:0]
011b	D[9:0]	B_DAC[9:0]	Point B DAC code setting[9:0]
100b	D[9:8]		
	D[7:5]	str[2:0]	Step resolution setting[2:0]
	D[4:0]	stt[4:0]	Step time setting[4:0]

Characteristics of the SDA and SCL Bus Lines for 2-wire Serial Interface

(Ta = - 25 to +85 °C, VCC = 2.3 to 4.8 V)

Parameter	Symbol	STANDARD-MODE (Note 4)		FAST-MODE (Note 4)		Unit
		Min.	Max.	Min.	Max.	
Pulse width of spikes which must be suppressed by the input filter	tSP	0	50	0	50	ns
Hold time (repeated) start condition. The first clock pulse is generated after this period.	tHD;STA	4.0	-	0.6	-	μs
Low period of the SCL clock	tLOW	4.7	-	1.3	-	μs
High period of the SCL clock	tHIGH	4.0	-	0.6	-	μs
Set-up time for repeated START condition	tSU;STA	4.7	-	0.6	-	μs
Data hold time	tHD;DAT	0	3.45	0	0.9	μs
Data set-up time	tSU;DAT	250	-	100	-	ns
Set-up time for stop condition	tSU;STO	4.0	-	0.6	-	μs
Bus free time between a stop and start condition	tBUF	4.7	-	1.3	-	μs

(Note 4) STANDARD-MODE and FAST-MODE 2-wire serial interface devices must be able to transmit or receive at the designated speed. The maximum bit transfer rates are 100 kbit/s for STANDARD-MODE devices and 400 kbit/s for FAST-MODE devices. This transfer rates is based on the maximum transfer rate. For example the bus is able to drive 100 kbit/s clocks with FAST-MODE.

2-wire Serial Interface Timing

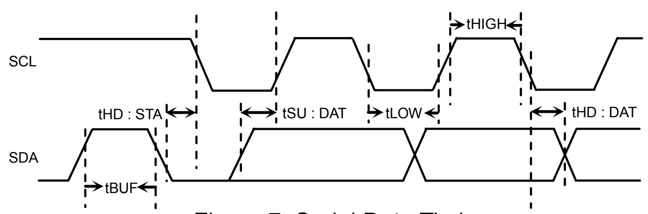


Figure 7. Serial Data Timing

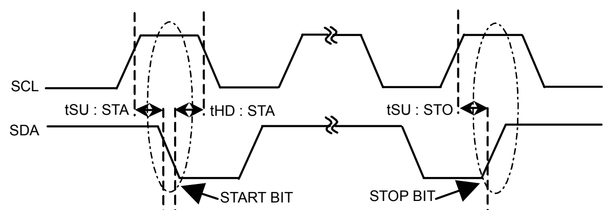


Figure 8. Start and Stop Bit Timing

Initialization Sequence

Item	Symbol	Min.	Typ.	Max.	Unit
Setup time for external power save pin	tPS;r	0	-	-	μs
Hold time for external power save pin	tPS;f	0	-	-	μs
2-wire serial data start time	ti2c;s	15	-	-	μs
2-wire serial data stop time	ti2c;p	1.3	-	-	μs

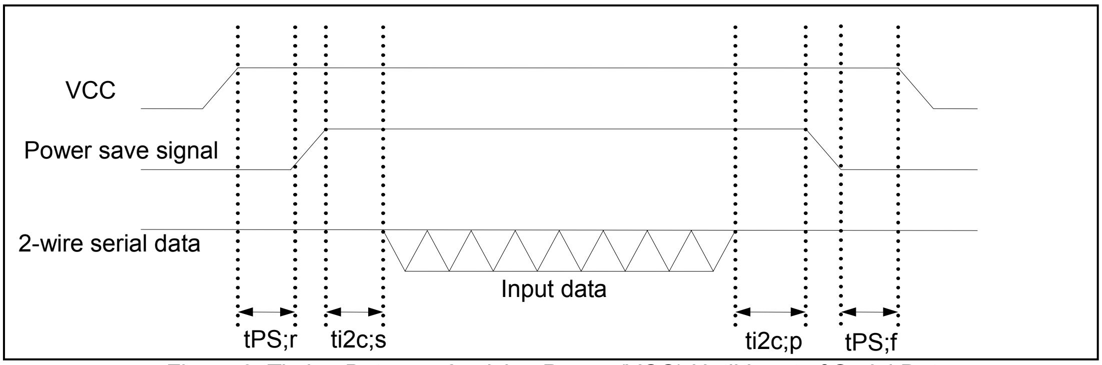
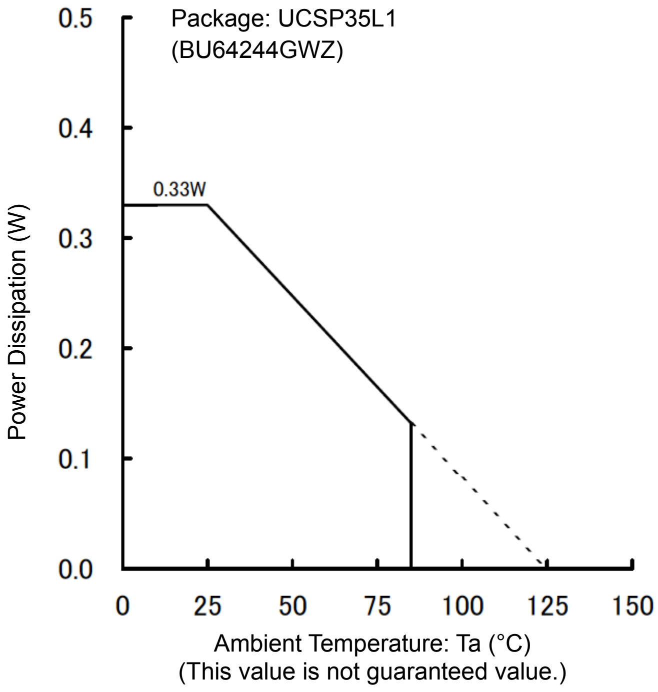


Figure 9. Timing Between Applying Power (VCC) Until Input of Serial Data

Power Dissipation



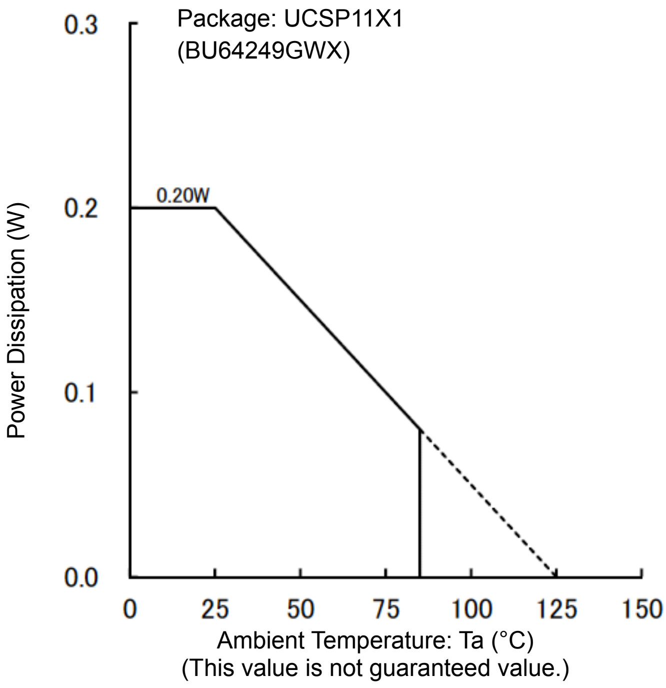
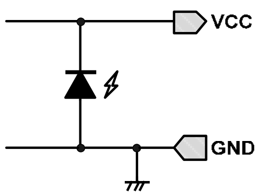
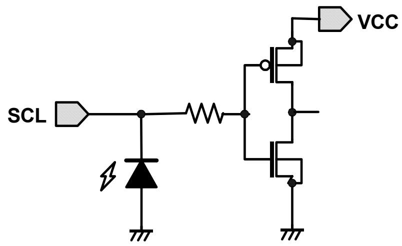
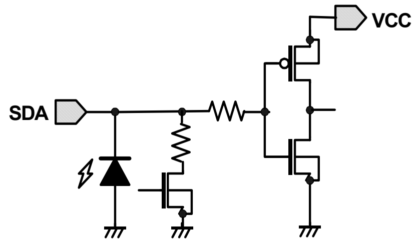
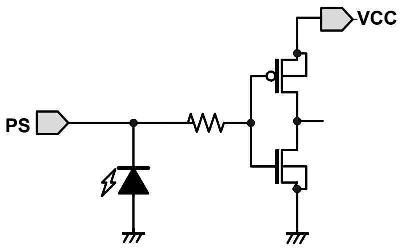
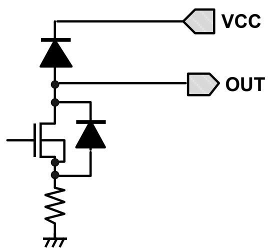


Figure 10. Power Dissipation (W)

I/O equivalent circuits

VCC	SCL	SDA
		
PS	**OUT**	
		

Controlling Mechanical Ringing

A voice coil motor (VCM) is an actuator technology that is intrinsically noisy due to the properties of the mechanical spring behavior. As current passes through the VCM, the lens moves and oscillates until the system reaches a steady state. The BU64244GWZ and BU64249GWX lens drivers are able to control mechanical oscillations by using the integrated ISRC (intelligent slew rate control) function. ISRC is operated by setting multiple control parameters that are determined by the intrinsic characteristics of the VCM. The following steps illustrate how to best utilize ISRC to minimize mechanical oscillations.

・Step A1 – Determining the Resonant Frequency of the VCM

Each VCM has a resonant frequency that can either be provided by the manufacturer or measured. The resonant frequency of an actuator determines the amount of ringing (mechanical oscillation) experienced after the lens as been moved to a target position and the driver output current held constant. To determine the resonant frequency, f_0, input a target DAC code by modifying the 10 bit C_DAC[9:0] value in register W2W1W0 = 000b that will target a final lens position approximately half of the actuator's full stroke. Take care to not apply too much current so that the lens does not hit the mechanical end of the actuator as this will show an incorrect resonant period. In order to start movement of the lens to the DAC code that was set in C_DAC[9:0], the EN bit must be set to 1.

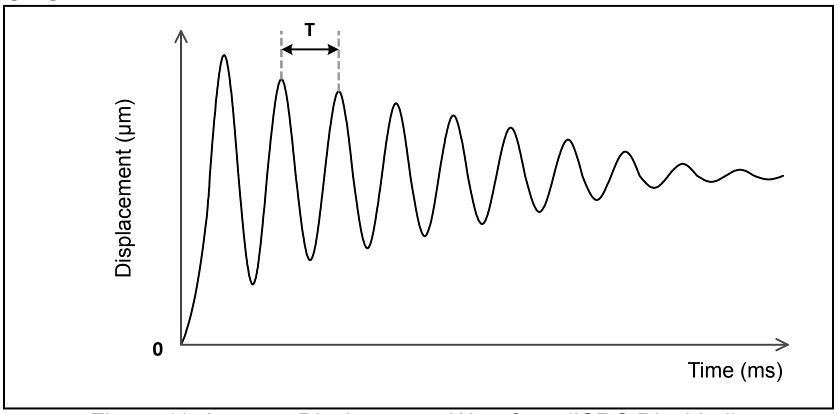


Figure 11. Actuator Displacement Waveform (ISRC Disabled)

The resonant frequency (Hz) of the actuator can be calculated with Equation 1 using the resonant period observed in Figure 11.

$$f_0 = (T)^{-1}$$

Equation1. Resonant Frequency vs. Time Period Relationship

After calculating the correct resonant frequency, program the closest value in the W2W1W0 = 001b register using the 5 bit rf[4:0] values from Table 1. When calculating the resonant frequency take care that different actuator samples' resonant frequencies might vary slightly and that the frequency tolerance should be taken into consideration when selecting the correct driver resonant frequency value.

Table 1. f_0 Settings (rf[4:0])

rf[4:0]	f_0	rf[4:0]	f_0	rf[4:0]	f_0	rf[4:0]	f_0
00000	-	01000	85 Hz	10000	125 Hz	11000	-
00001	50 Hz	01001	90 Hz	10001	130 Hz	11001	-
00010	55 Hz	01010	95 Hz	10010	135 Hz	11010	-
00011	60 Hz	01011	100 Hz	10011	140 Hz	11011	-
00100	65 Hz	01100	105 Hz	10100	145 Hz	11100	-
00101	70 Hz	01101	110 Hz	10101	150 Hz	11101	-
00110	75 Hz	01110	115 Hz	10110	-	11110	-
00111	80 Hz	01111	120 Hz	10111	-	11111	-

・Step A2 – Selecting the Autofocus Algorithm's Target DAC Codes

The ISRC algorithm is a proprietary technology developed to limit the ringing of an actuator by predicting the magnitude of ringing created by an actuator and intelligently controlling the output signal of the driver to minimize the ringing effect. Due to the ringing control behavior of ISRC, it is unable to operate properly unless the lens is floating (lens lifted off of the mechanical end of the actuator). As such the ringing control behavior is broken into three separate operational areas in order to provide the most optimally controlled autofocus algorithm.

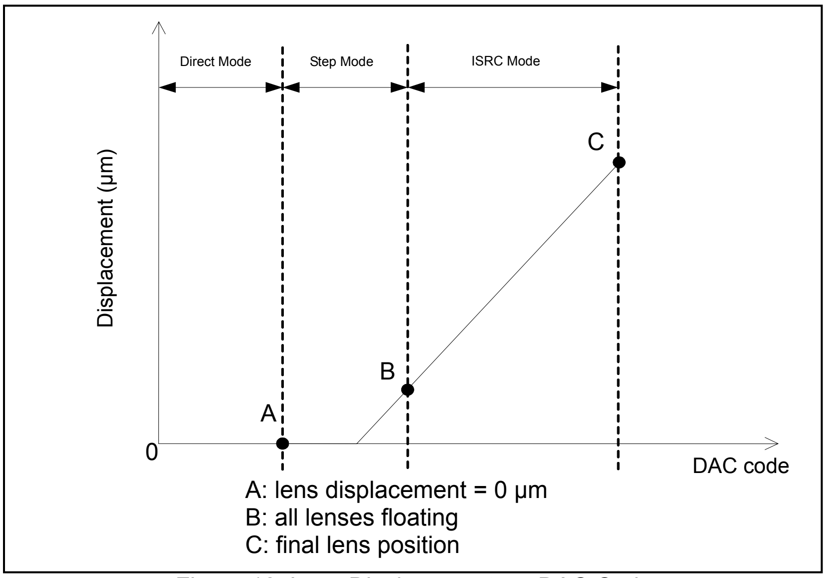


Figure 12. Lens Displacement vs. DAC Code

Figure 12 illustrates the different operational modes that control the autofocus algorithm. Due to ISRC requiring a floating lens, points A and B need to bet set in order to create a floating condition. Point A corresponds to the maximum amount of current that can be applied to all VCM units without floating the lens. Point B corresponds to the minimum amount of current that can be applied to the VCM so that all actuator units are floating. It should be noted that the target DAC codes could vary between different actuator units and that sufficient evaluation should be performed before selecting the point A and B target DAC codes. Point C is the final lens target position determined by the level of focus required for the image capture.

The actuator manufacturer should be able to provide the required current for points A and B, however it is possible to test these points by slowly increasing the 10 bit value of C_DAC[9:0] and measuring the lens movement using a laser displacement meter or some other device to measure lens displacement.

Controlling the Driver

After following steps A1 and A2 to characterize the VCM performance, the following steps should be followed in order to properly control the driver settings for optimized autofocus performance.

・Step B1 – Setting Point A, B, and C DAC Codes

Points A, B, and C are defined by 10 bit DAC codes set with the following registers:

Location	W2W1W0 Register	DAC Code Location	Description
Point C	000b	C_DAC[9:0]	Final lens position before image capture
Point A	010b	A_DAC[9:0]	Maximum output current without floating the lens
Point B	011b	B_DAC[9:0]	Minimum output current required to float the lens

・Step B2 – Controlling Direct Mode

Direct mode is when the driver outputs the desired amount of output current with no output current control. The time in which the lens reaches the position that corresponds to the amount of output current set by the 10 bit DAC code is ideally instant, ignoring the ringing effects. If the driver is set so that the lens is moved from a resting position to point C with direct mode, ringing and settling time will be at a maximum.

Direct mode is used either when M = 0 or when M = 1 and the present DAC code is less than the DAC code of point A.

M = 0 = ISRC mode disabled
When ISRC mode is disabled by setting the M bit equal to 0, the lens will traverse to the DAC code set for point C when the EN bit is set equal to 1.

M = 1 = ISRC mode enabled
The driver automatically uses direct mode if the present DAC code is less than the target DAC code corresponding to point A. Therefore during ISRC operation when the autofocus sequence has been started by setting the EN bit equal to 1, the driver will automatically decide to use direct mode to output current up to point A and then switch to step mode before continuing the autofocus sequence.

・Step B3 – Controlling Step Mode

Step mode is the control period in which the lens is moved by small output current steps. During step mode it is possible to control the step resolution and step time in order to generate just enough output current to float the lens with minimal ringing effects. Ringing can be better controlled by choosing a large value for the step time and a small value for the step resolution with the trade off of a greater settling time. The step time and step resolution should be chosen depending on the acceptable system limits of ringing vs. settling time.

Step mode is used when M = 1 and the present DAC code is in between point A and point B. Typically this mode is only used during ISRC operation between point A and B, however it is possible to move the lens to point C using only step mode if point C is set such that point C is only 1 DAC code greater than point B.

Step mode is controlled by the 5 bit step time, stt[4:0], and 3 bit step resolution, str[2:0], values stored in register W2W1W0 = 100b.

Table 2. Step Time Settings

stt[4:0]	Step Time	stt[4:0]	Step Time	stt[4:0]	Step Time	stt[4:0]	Step Time
00000	-	01000	400 µs	10000	800 µs	11000	1200 µs
00001	50 µs	01001	450 µs	10001	850 µs	11001	1250 µs
00010	100 µs	01010	500 µs	10010	900 µs	11010	1300 µs
00011	150 µs	01011	550 µs	10011	950 µs	11011	1350 µs
00100	200 µs	01100	600 µs	10100	1000 µs	11100	1400 µs
00101	250 µs	01101	650 µs	10101	1050 µs	11101	1450 µs
00110	300 µs	01110	700 µs	10110	1100 µs	11110	1500 µs
00111	350 µs	01111	750 µs	10111	1150 µs	11111	1550 µs

Table 3. Step Resolution Settings

str[2:0]	Step Resolution	str[2:0]	Step Resolution	str[2:0]	Step Resolution	str[2:0]	Step Resolution
000	-	010	2 LSB	100	4 LSB	110	6 LSB
001	1 LSB	011	3 LSB	101	5 LSB	111	7 LSB

・Step B4 – Controlling ISRC Mode

ISRC mode is the control period in which the lens is already floating and the driver smoothly moves the lens based on the proprietary behavior of the ISRC algorithm. ISRC operation keeps ringing at a minimum while achieving the fastest possible settling time based on the ISRC operational conditions.

ISRC mode is used when M = 1 and the present DAC code is greater than the DAC code for point B. If the target DAC code for point C is set so that the value is too large and will cause excess ringing, the point C DAC code is automatically updated with a driver pre-determined value to minimize the ringing effect. When M = 1, the driver will automatically switch between direct mode, step mode, and ISRC mode when the point A, B, and C DAC code conditions are met. The condition for this automatic transitioning to occur is when the register values for point A, point B, point C, step time, and step resolution are all set to values other than 0 and then the sequence will start when the EN bit is set equal to 1.

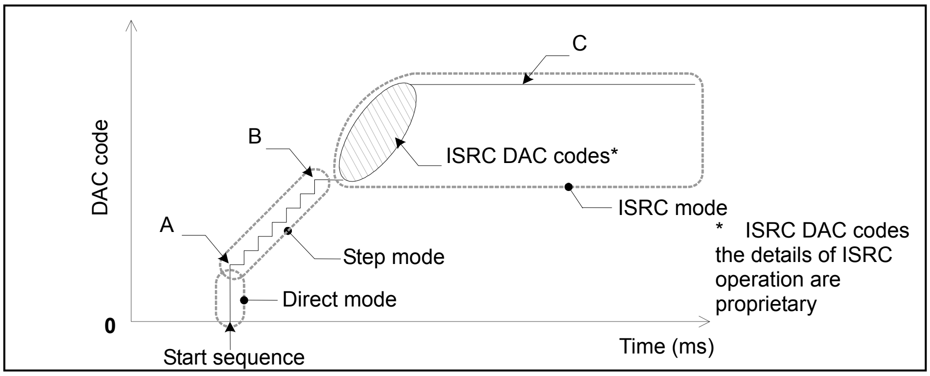


Figure 13. Three Modes Sequential Operation (Shown as DAC Codes)

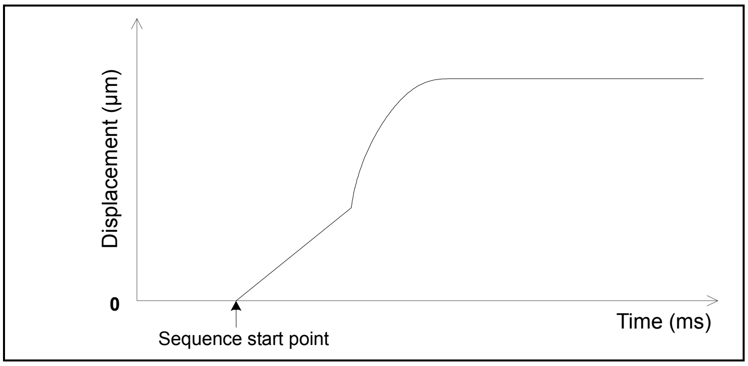


Figure 14. Three Modes Sequential Operation (Shown as Lens Displacement)

・Step B5 – Controlling the ISRC Settling Time

The settling time of an actuator is the time it takes for ringing to cease. The BU64244GWZ and BU64249GWX are able to control the settling time by modifying the slew rate speed parameter, however care must be taken to balance settling time vs. acceptable ringing levels. By increasing the slew rate speed there is the possibility to decrease the settling time but the ability to control ringing is also decreased. Likewise if less ringing is desired then there is a possibility to reduce the ringing level by using a slower slew rate speed setting at the cost of a longer settling time. The slew rate speed can be set by modifying the 2 bit slew_rate[1:0] value in register W2W1W0 = 001b. Figure 15 shows the relationship of displacement vs. settling time.

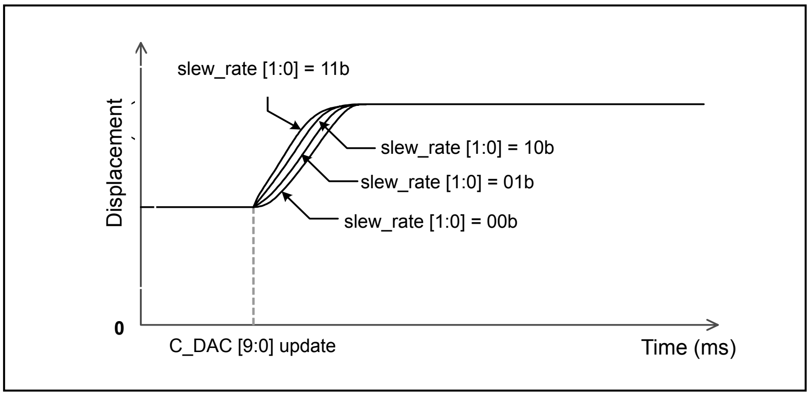


Figure 15. Displacement vs. Settling Time

Table 4. Slew Rate Speed Settings

slew_rate[1:0]	Slew Rate Speed	slew_rate[1:0]	Slew Rate Speed	slew_rate[1:0]	Slew Rate Speed	slew_rate[1:0]	Slew Rate Speed
00	Slowest	01	Slow	10	Fast	11	Fastest

・Step B6 – DAC Code Update Timing Considerations

Settling time is controlled by the resonant frequency of the actuator and the driver's slew rate speed setting. Depending on the combination of these parameters, the settling time can be such that updating point C with a new DAC code before the lens has settled at the original point C DAC code can adversely affect the settling time due to increased ringing effects. Utilize the slew rate speed parameter in order to modify the settling time so that any updates to the point C DAC code do not occur before the lens has settled.

Please review the following example based on an actuator with a resonant frequency of 100 Hz:

Table 5. Relationship Between Slew Rate Speed and Settling Time Based on a 100 Hz Actuator

f_0	slew_rate[1:0]	Settling Time
100 Hz	00	52 ms
	01	42 ms
	10	26 ms
	11	18 ms

In this example the settling time of the actuator can vary by up to ± 5 % due to the internal oscillator (MCLK) having a variance of ± 5%. The settling time has a proportionally inverse relationship to the resonant frequency and therefore the settling time can be estimated as:

Table 6. Relationship Between Slew Rate Speed and Settling Time Based on a General Resonant Frequency f_0'

f_0'	slew_rate[1:0]	Settling Time
f_0' Hz	00	52 * (100 / f_0') ms
	01	42 * (100 / f_0') ms
	10	26 * (100 / f_0') ms
	11	18 * (100 / f_0') ms

Note that the orientation of the camera module can affect the settling time due to the influence of gravity on the lens.

・Step C1 – Power Save Operation

The BU64244GWZ and BU64249GWX can be set to enter power save mode either by setting the external power save pin = VPSL (typically 0 V) or by setting the 2-wire serial PS bit = 0. It is recommended to use the external power save pin method since this will disable the internal MCLK to achieve lower power consumption while in standby mode. Please note that setting the external power save pin = VPSL will reset all 2-wire serial registers to 0.

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

Operational Notes – continued

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC’s power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Disturbance light

In a device where a portion of silicon is exposed to light such as in a WL-CSP, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

Ordering Part Number (BU64244GWZ)

B	U	6	4	2	4	4	G	W	Z	TR

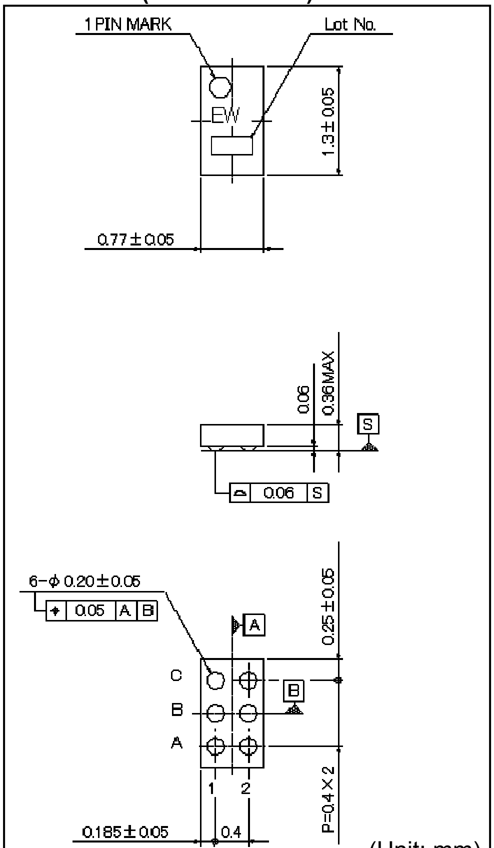
Part Number

Package
GWZ: UCSP35L1

Packaging and forming specification
TR: Embossed carrier tape

Physical Dimension Tape and Reel Information (BU64244GWZ)

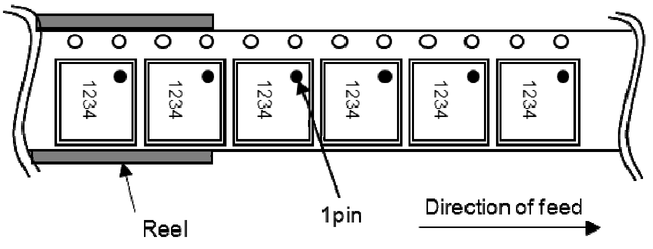
UCSP35L1 (BU64244GWZ)



(Unit: mm)

<Packing specification>

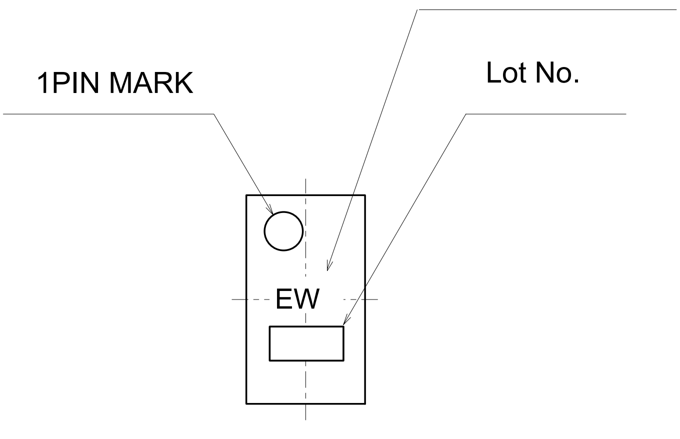
Tape	Embossed carrier tape
Quantity	6,000 pcs / reel
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Marking Diagram(TOP VIEW) (BU64244GWZ)

UCSP35L1 (BU64244GWZ)



Ordering Part Number (BU64249GWX)

B	U	6	4	2	4	9	G	W	X		E2

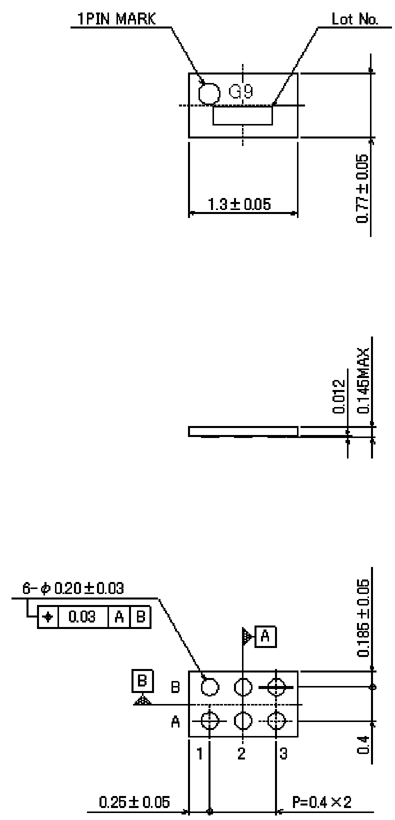
Part Number

Package
GWZ: UCSP11X1

Packaging and forming specification
E2: Embossed tape and reel

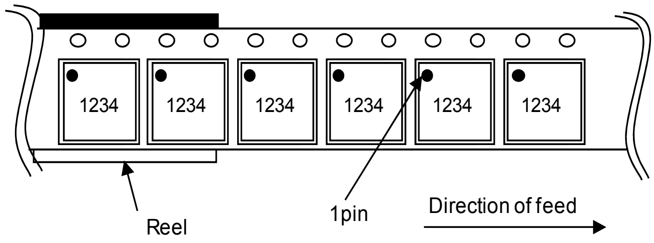
Physical Dimension Tape and Reel Information (BU64249GWX)

UCSP11X1 (BU64249GWX)



(Unit: mm)

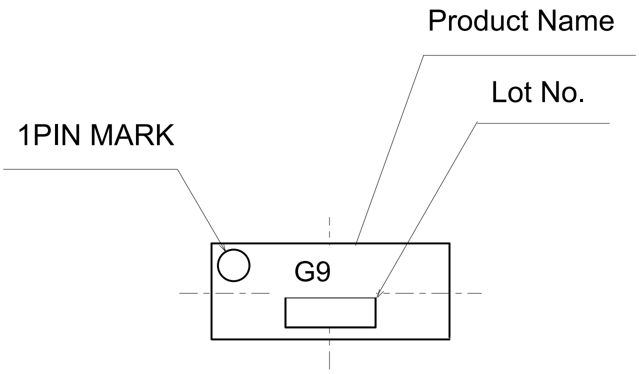
Tape	Embossed carrier tape
Quantity	3,000 pcs / reel
Direction of feed	E2 (See neighboring image)



*Order quantity needs to be multiple of the minimum quantity.

Marking Diagram(TOP VIEW) (BU64249GWX)

UCSP11X1 (BU64249GWX)



Revision History

Date	Revision	Changes
04.Nov.2014	001	New Release

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
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   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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