











#### LT1013, LT1013D, LT1013M, LT1013AM

SLOS018I-MAY 1988-REVISED JULY 2016

# LT1013x Dual Precision Operational Amplifier

#### **Features**

- Single-Supply Operation
  - Input Voltage Range Extends to Ground
  - Output Swings to Ground While Sinking Current
- Phase Reversal Protection
- Input Offset Voltage
  - 150 µV Maximum at 25°C for LT1013AM
- Offset-Voltage Temperature Coefficient
  - 2 μV/°C Maximum for LT1013AM
- Input Offset Current
  - 0.8 nA Maximum at 25°C for LT1013AM
- High Gain
  - 1.5 V/ $\mu$ V Minimum (R<sub>L</sub> = 2 k $\Omega$ ) for LT1013AM
  - 0.8 V/ $\mu$ V Minimum (R<sub>I</sub> = 600 k $\Omega$ ) for LT1013AM
- Low Supply Current
  - 0.5 mA Maximum at  $T_A = 25$ °C for LT1013AM
- Low Peak-to-Peak Noise Voltage
  - 0.55 μV Typical
- Low Current Noise
  - 0.07 pA/√Hz Typical
- For Die Only Option, See LT1013-DIE

## Applications

- Thermocouple Amplifiers
- Low-Side Current Measurement
- Instrumentation Amplifiers

## 3 Description

The LT1013x devices are dual precision operational amplifiers, featuring high gain, low supply current, low noise, and low-offset-voltage temperature coefficient.

The LT1013x devices can be operated from a single 5-V power supply; the common-mode input voltage range includes ground, and the output can also swing to within a few millivolts of ground. Crossover distortion is eliminated. The LT1013x can be operated with both dual ± 15-V and single 5-V supplies.

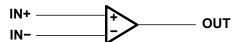
The LT1013C and LT1013D are characterized for operation from 0°C to 70°C. The LT1013DI is characterized for operation from -40°C to 105°C. The LT1013M, LT1013AM, and LT1013DM characterized for operation over the full military temperature range of -55°C to 125°C.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE (PINS)	BODY SIZE (NOM)
LT1013D LT1013DD	SOIC (8)	4.90 mm × 3.91 mm
LT1013P LT1013DP	PDIP (8)	9.81 mm × 6.35 mm
LT1013MFK LT1013AMFK	LCCC (20)	8.89 mm × 8.89 mm
LT1013MJG LT1013AMJG	CDIP (8)	9.60 mm × 6.67 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Symbol (Each Amplifier)



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## 4 Revision History

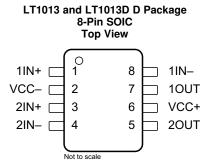
#### Changes from Revision H (November 2004) to Revision I

Page

Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.
 Removed Ordering Information table, see POA at the end of the data sheet



## 5 Pin Configuration and Functions



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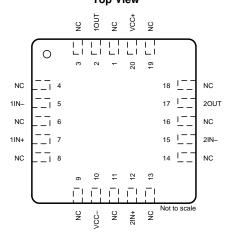
Not to scale

VCC- [

5

2IN+

#### LT1013M and LT1013AM FK Package 20-Pin LCCC Top View



#### **Pin Functions**

		PIN		1/0	DECORIDEION
NAME	SOIC	LCCC	CDIP, PDIP	I/O	DESCRIPTION
1IN+	1	7	3	I	Noninverting input for channel 1
1IN-	8	5	2	I	Inverting input for channel 1
1OUT	7	2	1	0	Output for channel 1
2IN+	3	12	5	I	Noninverting input for channel 2
2IN-	4	15	6	I	Inverting input for channel 2
2OUT	5	17	7	0	Output for channel 2
NC	_	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	_	_	No internal connection
VCC+	6	20	8	_	Positive supply Voltage
VCC-	2	10	4	_	Negative supply Voltage



## **Specifications**

#### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
$V_{CC+} - V_{CC-}$	Supply voltage <sup>(2)</sup>		-0.3	44	V
VI	Input voltage (any input)		V <sub>CC</sub> 5	$V_{CC+}$	٧
	Differential input voltage (3)			±30	٧
	Duration of short-circuit current at (or below) 25°C <sup>(4)</sup>		Unlimi	ited	
	Case temperature for 60 s	FK package		260	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 s	JG package		300	°C
$T_J$	Operating virtual junction temperature			150	°C
T <sub>stg</sub>	Storage temperature	·	-65	150	°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

			VALUE	UNIT					
LT1013	_T1013 in D and P packages								
V	V <sub>(ESD)</sub> Electrostatic Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)		±1000	V					
V(ESD)	V <sub>(ESD)</sub> discharge Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)		±500	V					
LT1013E	O in D and P packages								
Electrostatic		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V					
$V_{(ESD)}$	V(ESD) discharge Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)		±500	V					

JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

#### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC+</sub> - V <sub>CC</sub>	Supply voltage		5	30	V
		LT1013C, LT1013D	0	70	
T <sub>A</sub>	Ambient temperature	LT1013DI	-40	105	°C
		LT1013M, LT1013AM, LT1013DM	<b>-</b> 55	125	
M	lanut common mode veltage	LT1013C, LT1013D, LT1013DI	V <sub>CC</sub> -	V <sub>CC+</sub> – 2	M
V <sub>ICM</sub>	Input common-mode voltage	LT1013M, LT1013AM, LT1013DM	V <sub>CC-</sub> + 0.1	V <sub>CC+</sub> – 2	٧

Supply voltage is  $V_{CC+}$  with respect to  $V_{CC-}$ . Differential voltage is IN+ with respect to IN-.

The output may be shorted to either supply.

JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



#### 6.4 Thermal Information

			LT101	3x		
	THERMAL METRIC(1)	D (SOIC)	P (PDIP)	FK (LCCC)	JG (CDIP)	UNIT
		8 PINS	8 PINS	20 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)(3)	101.6	49.5	_	_	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.6	38.7	35.7 <sup>(4)</sup>	58.5 <sup>(4)</sup>	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42	26.7	34.8	82.9	°C/W
ΨЈТ	Junction-to-top characterization parameter	8.3	15.9	_	_	°C/W
ΨЈВ	Junction-to-board characterization parameter	41.5	26.6	_	_	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	_	_	4.0(4)	10.8(4)	°C/W

- (1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
- (2) Maximum power dissipation is a function of  $T_{J(max)}$ ,  $R_{\theta JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_{J(max)} T_A)/R_{\theta JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.
- 3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) R<sub>0JC(top)</sub> and R<sub>0JC(bot)</sub>thermal impedances are calculated in accordance with MIL-STD-883 for LCCC and CDIP

## 6.5 Electrical Characteristics: LT1013C, ±15 V

at specified free-air temperature,  $V_{CC\pm} = \pm 15 \text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T <sub>A</sub> <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
.,		D 50 0	25°C		60	300	.,
$V_{IO}$	Input offset voltage	$R_S = 50 \Omega$	Full range			400	μV
ανιο	Temperature coefficient of input offset voltage		Full range		0.4	2.5	μV/°C
	Long-term drift of input offset voltage		25°C		0.5		μV/mo
1	Input offset current		25°C		0.2	1.5	nA
I <sub>IO</sub>	input onset current		Full range			2.8	IIA
	Innut bigg gurrant		25°C		-15	-30	<b>~</b> Λ
I <sub>IB</sub>	Input bias current		Full range			-38 TIA	nA
V	Common-mode input voltage	December de diverses	25°C	-15		13.5	V
$V_{ICR}$	range	Recommended range	Full range	-15		13 V	V
V	Maximum peak output	D 2k0	25°C	±12.5	±14		V
VOM	voltage swing	$R_L = 2 k\Omega$	Full range	±12			V
		$V_{O} = \pm 10 \text{ V}, R_{L} = 600 \Omega$	25°C	0.5	0.2		
$A_{VD}$	Large-signal differential voltage amplification	V 140 V D 0140	25°C	1.2	7		$V/\mu V$
	voltage amplification	$V_O = \pm 10 \text{ V}, R_L = 2 \text{ k}\Omega$	Full range	0.7			
OMBD		V <sub>IC</sub> = −15 V to 13.5 V	25°C	97	114		-ID
CMRR	Common-mode rejection ratio	V <sub>IC</sub> = -14.9 V to 13 V	Full range	94			dB
1.	Supply-voltage rejection ratio	V 10.V/+= 140.V/	25°C	100	117		-ID
k <sub>SVR</sub>	(ΔVCC/ΔVIO)	$V_{CC+} = \pm 2 \text{ V to } \pm 18 \text{ V}$	Full range	97			dB
	Channel separation	$V_O = \pm 10 \text{ V}, R_L = 2 \text{ k}\Omega$	25°C	120	137		dB
r <sub>id</sub>	Differential input resistance		25°C	70	300		МΩ
r <sub>ic</sub>	Common-mode input resistance		25°C		4		GΩ
	Consolir someont non one PEC-		25°C		0.35	0.55	
Icc	Supply current per amplifier		Full range			0.7	mA

<sup>(1)</sup> Full range is 0°C to 70°C.

(2) All typical values are at  $T_A = 25$ °C.



## 6.6 Electrical Characteristics: LT1013C, 5 V

at specified free-air temperature,  $V_{CC_{+}} = 5 \text{ V}$ ,  $V_{CC_{-}} = 0$ ,  $V_{O} = 1.4 \text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T <sub>A</sub> <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
.,	land the standard	B 50.0	25°C		90	450	
$V_{IO}$	Input offset voltage	$R_S = 50 \Omega$	Full range			570	μV
i	least effect comment		25°C		0.3	2	0
I <sub>IO</sub>	Input offset current		Full range			6	nA
	land this a summer		25°C		-18	-50	4
I <sub>IB</sub>	Input bias current		Full range			-90	nA
.,	0	D	25°C	0		3.5	8.5 V
V <sub>ICR</sub>	Common-mode input voltage range	Recommended range	Full range	0		3	V
		Output low, No load	25°C		15	25	
		Output low, $R_1 = 600 \Omega$ to GND	25°C		5	10	
		Output low, $N_L = 800 \Omega$ to GND	Full range			13	
$V_{OM}$	Maximum peak output voltage swing	Output low, I <sub>sink</sub> = 1 mA	25°C		220	350	V
		Output high, No load	25°C	4	4.4		
		Outsit high D COO O to CND	25°C	3.4	4		
		Output high, $R_L = 600 \Omega$ to GND	Full range	3.2			
A <sub>VD</sub>	Large-signal differential voltage amplification	$V_O$ = 5 mV to 4 V, $R_L$ = 500 $\Omega$	25°C		1		V/µV
	Supply ourrent per amplifier		25°C		0.32	0.5	mΛ
cc	Supply current per ampliner	oly current per amplifier	Full range			0.55	mA

<sup>(1)</sup> 

## 6.7 Electrical Characteristics: LT1013D, ±15 V

at specified free-air temperature,  $V_{CC\pm} = \pm 15 \text{ V}, V_{IC} = 0$  (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T <sub>A</sub> <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
	langet offeet veltore	D 50.0	25°C		200	800	\/
$V_{IO}$	Input offset voltage	$R_S = 50 \Omega$	Full range			1000	μV
$\alpha_{VIO}$	Temperature coefficient of input offset voltage		Full range		0.7	5	μV/°C
	Long-term drift of input offset voltage		25°C		0.5		μV/mo
	Input offset current		25°C		0.2	1.5	nA
I <sub>IO</sub>	input onset current		Full range			2.8	IIA
	Input bigg gurrent		25°C		-15	-30	nA
I <sub>IB</sub>	Input bias current		Full range			-38	ΠA
V	Common-mode input voltage range	Recommended range	25°C	-15		13.5	٧
V <sub>ICR</sub>	Common-mode input voltage range	Recommended range	Full range	-15		13	V
V	Maximum pook autout valtage aving	$R_1 = 2 k\Omega$	25°C	±12.5	±14		V
$V_{OM}$	Maximum peak output voltage swing	$n_L = 2 \text{ K}\Omega$	Full range	±12			V
		$V_{O} = \pm 10 \text{ V}, R_{L} = 600 \Omega$	25°C	0.5	2		
$A_{VD}$	Large-signal differential voltage amplification	$V_{O} = \pm 10 \text{ V}, R_{L} = 2 \text{ k}\Omega$	25°C	1.2	7		$V/\mu V$
		$V_0 = \pm 10 \text{ V}, n_L = 2 \text{ K} \pm 2$	Full range	0.7			
CMRR	Common-mode rejection ratio	$V_{IC} = -15 \text{ V to } 13.5 \text{ V}$	25°C	97	114		dB
CIVINN	Common-mode rejection ratio	$V_{IC} = -14.9 \text{ V to } 13 \text{ V}$	Full range	94			uБ
le.	Cumply valtage valenties vatin (AVCC/AVIO)	V 10.V to 110.V	25°C	100	117		dB
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔVCC/ΔVIO)	$V_{CC+} = \pm 2 \text{ V to } \pm 18 \text{ V}$	Full range	97			uБ
	Channel separation	$V_O = \pm 10 \text{ V}, \text{ R}_L = 2 \text{ k}\Omega$	25°C	120	137		dB
r <sub>id</sub>	Differential input resistance		25°C	70	300		ΜΩ
r <sub>ic</sub>	Common-mode input resistance		25°C		4		GΩ
	Cumply surrent new amplifier		25°C		0.35	0.55	5
I <sub>CC</sub>	Supply current per amplifier	Full range			0.6	mA	

Full range is 0°C to 70°C.

Full range is 0°C to 70°C. All typical values are at  $T_A = 25$ °C.

<sup>(2)</sup> All typical values are at  $T_A = 25$ °C.



### 6.8 Electrical Characteristics: LT1013D, 5 V

at specified free-air temperature,  $V_{CC_{+}} = 5 \text{ V}$ ,  $V_{CC_{-}} = 0$ ,  $V_{O} = 1.4 \text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T <sub>A</sub> <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
.,	lance of the state of	D 50.0	25°C		250	950	
V <sub>IO</sub>	Input offset voltage	$R_S = 50 \Omega$	Full range			1200	μV
	lanut effect current		25°C		0.3	2	nA
I <sub>IO</sub>	Input offset current		Full range			6	ΠA
	Input bing aurent		25°C		-18	-50	Λ
I <sub>IB</sub>	Input bias current		Full range			-90	nA
.,	Common mode input valtage vance	Decemmended range	25°C	0		3.5	3.5 V
V <sub>ICR</sub>	Common-mode input voltage range	Recommended range	Full range	0		3 V	
		Output low, No load	25°C		15	25	
		Outrout law D COO O to CND	25°C		5	10	
		Output low, $R_L = 600 \Omega$ to GND	Full range			13	
$V_{OM}$	Maximum peak output voltage swing	Output low, I <sub>sink</sub> = 1 mA	25°C		220	350	V
		Output high, No load	25°C	4	4.4		
		Outsit high D COO O to OND	25°C	3.4	4		
		Output high, $R_L = 600 \Omega$ to GND	Full range	3.2			
A <sub>VD</sub>	Large-signal differential voltage amplification	$V_O$ = 5 mV to 4 V, $R_L$ = 500 $\Omega$	25°C		1		V/µV
	Cumply suggest now amplifier		25°C		0.32	0.5	mA
I <sub>CC</sub>	Supply current per amplifier		Full range			0.55	

## 6.9 Electrical Characteristics: LT1013DI, ±15 V

at specified free-air temperature,  $V_{\text{CC}\pm}$  = ±15 V,  $V_{\text{IC}}$  = 0 (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T <sub>A</sub> <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT	
V	Input offset voltage	B 50.0	25°C		200	800	μV	
V <sub>IO</sub>	input onset voltage	$R_S = 50 \Omega$	Full range			1000	μν	
$\alpha_{\text{VIO}}$	Temperature coefficient of input offset voltage		Full range		0.7	5	μV/°C	
	Long-term drift of input offset voltage		25°C		0.5		μV/mo	
l	Input offset current		25°C		0.2	1.5	nA	
I <sub>IO</sub>	input onset current		Full range			2.8	IIA	
l	Input bias current		25°C		-15	-30	nA	
I <sub>IB</sub>	input bias current		Full range			-38	IIA	
V	Common-mode input voltage range	Recommended range	25°C	-15		13.5 13	V	
V <sub>ICR</sub>	Common-mode input voltage range	neconinenced range	Full range	-15				
V	Maximum peak output voltage swing	$R_L = 2 k\Omega$	25°C	±12.5	±14	V	V	
$V_{OM}$	iviaximum peak output voltage swing	nL = 2 K22	Full range	±12			V	
		$V_O = \pm 10 \text{ V}, \text{ R}_L = 600 \Omega$	25°C	0.5	0.2			
$A_{VD}$	Large-signal differential voltage amplification	$V_{\Omega} = \pm 10 \text{ V}, R_{1} = 2 \text{ k}\Omega$	25°C	1.2	7		$V/\mu V$	
		$V_0 = \pm 10 \text{ V}, \text{ n}_L = 2 \text{ K} \Sigma$	Full range	0.7				
CMRR	Common-mode rejection ratio	$V_{IC} = -15 \text{ V to } 13.5 \text{ V}$	25°C	97	114		dB	
CIVINN	Common-mode rejection ratio	$V_{IC} = -14.9 \text{ V to } 13 \text{ V}$	Full range	94			uБ	
k	Supply-voltage rejection ratio (ΔVCC/ΔVIO)	$V_{CC+} = \pm 2 \text{ V to } \pm 18 \text{ V}$	25°C	100	117		dB	
k <sub>SVR</sub>	Supply-voltage rejection ratio (AVCC/AVIO)	V <sub>CC+</sub> = ±2 V (0 ±16 V	Full range	97			uБ	
	Channel separation	$V_O = \pm 10 \text{ V}, \text{ R}_L = 2 \text{ k}\Omega$	25°C	120	137		dB	
r <sub>id</sub>	Differential input resistance		25°C	70	300		$M\Omega$	
r <sub>ic</sub>	Common-mode input resistance		25°C		4		$G\Omega$	
	Supply current per amplifier		25°C		0.35	0.55	55	
I <sub>CC</sub>	Supply current per amplifier		Full range			0.6	mA	

Full range is -40°C to 105°C.

<sup>(1)</sup> Full range is 0°C to 70°C.
(2) All typical values are at T<sub>A</sub> = 25°C.

All typical values are at  $T_A = 25$ °C.



### 6.10 Electrical Characteristics: LT1013DI, 5 V

at specified free-air temperature,  $V_{CC_{+}} = 5 \text{ V}$ ,  $V_{CC_{-}} = 0$ ,  $V_{O} = 1.4 \text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T <sub>A</sub> <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT	
V	land offeet veltore	D 500	25°C		250	950	\/	
V <sub>IO</sub>	Input offset voltage	$R_S = 50 \Omega$	Full range			1200	μV	
	long it offers a company		25°C		0.3	2	Λ	
I <sub>IO</sub>	Input offset current		Full range			6	nA	
ı	Input bias current		25°C		-18	-50	nA	
IB	input bias current		Full range			-90	IIA	
V	Common-mode input voltage range	Recommended range	25°C	0		3.5	V	
V <sub>ICR</sub>	Common-mode input voitage range	necommended range	Full range	0		3	V	
		Output low, No load	25°C		15	25		
		Output low, $R_i = 600 \Omega$ to GND	25°C		5	10	1	
		Output low, R <sub>L</sub> = 600 12 to GND	Full range			13		
V <sub>OM</sub>	Maximum peak output voltage swing	Output low, I <sub>sink</sub> = 1 mA	25°C		220	350	V	
		Output high, No load	25°C	4	4.4			
		Output high, $R_L = 600 \Omega$ to GND	25°C	3.4	4			
		Output high, R <sub>L</sub> = 800 t2 to GND	Full range	3.2				
A <sub>VD</sub>	Large-signal differential voltage amplification	$V_O$ = 5 mV to 4 V, $R_L$ = 500 $\Omega$	25°C		1		V/µV	
	Cumply assured new amplifies		25°C		0.32	0.5	A	
CC	Supply current per amplifier		Full range			0.55	mA	

<sup>(1)</sup> Full range is -40°C to 105°C.

### 6.11 Electrical Characteristics: LT1013M, ±15 V

at specified free-air temperature,  $V_{CC\pm} = \pm 15 \text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T <sub>A</sub> <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V	Innut offect veltage	D 50.0	25°C		60	300	\/
$V_{IO}$	Input offset voltage	$R_S = 50 \Omega$	Full range			550	μV
ανιο	Temperature coefficient of input offset voltage		Full range		0.5	2.5 <sup>(3)</sup>	μV/°C
	Long-term drift of input offset voltage		25°C		0.5		μV/mo
1	lanut offect current		25°C		0.2	1.5	nA
I <sub>IO</sub>	Input offset current		Full range			5	ΠA
1	land the second of		25°C		-15	-30	^
IB	Input bias current		Full range			-45	nA
.,	O	December of the second	25°C	-15		13.5	V
V <sub>ICR</sub>	Common-mode input voltage range	Recommended range	Full range	-14.9		13	V
M	Manifestore	D. O.LO	25°C	±12.5	±14		V
V <sub>OM</sub>	Maximum peak output voltage swing	$R_L = 2 k\Omega$	Full range	±11.5			V
	Large-signal differential voltage amplification	$V_{O} = \pm 10 \text{ V}, R_{L} = 600 \Omega$	25°C	0.5	2		
$A_{VD}$		V 140 V D 01-0	25°C	1.2	7		$V/\mu V$
		$V_O = \pm 10 \text{ V}, R_L = 2 \text{ k}\Omega$	Full range	0.25			
CMRR	0	V <sub>IC</sub> = −15 V to 13.5 V	25°C	97	117		dB
CIVIRR	Common-mode rejection ratio	V <sub>IC</sub> = -14.9 V to 13 V	Full range	94			ав
ī.	C	V 10.V+= 140.V	25°C	100	117		-ID
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔVCC/ΔVIO)	$V_{CC+} = \pm 2 \text{ V to } \pm 18 \text{ V}$	Full range	97			dB
	Channel separation	$V_O = \pm 10 \text{ V}, R_L = 2 \text{ k}\Omega$	25°C	120	137		dB
r <sub>id</sub>	Differential input resistance		25°C	70	300		ΜΩ
r <sub>ic</sub>	Common-mode input resistance		25°C		4		GΩ
ı	Complex company and a second life or		25°C		0.35	0.55	A
I <sub>CC</sub>	Supply current per amplifier		Full range			0.7	mA

<sup>1)</sup> Full range is -55°C to 125°C.

<sup>(2)</sup> All typical values are at  $T_A = 25$ °C.

<sup>(2)</sup> All typical values are at  $T_A = 25$ °C.

<sup>3)</sup> On products compliant to MIL-PRF-38535, Class B, this parameter is not production tested.



### 6.12 Electrical Characteristics: LT1013M, 5 V

at specified free-air temperature,  $V_{CC+} = 5 \text{ V}$ ,  $V_{CC-} = 0$ ,  $V_{O} = 1.4 \text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T <sub>A</sub> <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
		B 50.0	25°C		90	450	
$V_{IO}$	Input offset voltage	$R_S = 50 \Omega$	Full range		400	1500	μV
		$R_S = 50 \Omega, V_{IC} = 0.1 V$	125°C		200	750	
	lands offers adversed		25°C		0.3	2	A
I <sub>IO</sub>	Input offset current		Full range			10	nA
	lanut biog growent		25°C		-18	-50	^
I <sub>IB</sub>	Input bias current		Full range			-120	nA
.,	Orange and investment and	December of the con-	25°C	0		3.5	V
V <sub>ICR</sub>	Common-mode input voltage range	Recommended range	Full range	0		3	V
		Output low, No load	25°C		15	25	
		Outrot law D. COO C to CND	25°C		5	10	
		Output low, $R_L = 600 \Omega$ to GND	Full range			18	
$V_{OM}$	Maximum peak output voltage swing	Output low, I <sub>sink</sub> = 1 mA	25°C		220	350	V
		Output high, No load	25°C	4	4.4		
		O OND	25°C	3.4	4		
		Output high, $R_L = 600 \Omega$ to GND	Full range	3.1			
A <sub>VD</sub>	Large-signal differential voltage amplification	$V_O$ = 5 mV to 4 V, $R_L$ = 500 $\Omega$	25°C		1		V/µV
	Owner to the second sec		25°C		0.32	0.5	4
I <sub>CC</sub>	Supply current per amplifier		Full range			0.65	mA

<sup>(1)</sup> Full range is -55°C to 125°C.

## 6.13 Electrical Characteristics: LT1013AM, ±15 V

at specified free-air temperature,  $V_{CC\pm} = \pm 15 \text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T <sub>A</sub> <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V	Innut offect valtage	D 50.0	25°C		40	150	\/
V <sub>IO</sub>	Input offset voltage	$R_S = 50 \Omega$	Full range			300	μV
$\alpha_{\text{VIO}}$	Temperature coefficient of input offset voltage		Full range		0.4	2(3)	μV/°C
	Long-term drift of input offset voltage		25°C		0.4		μV/mo
i	Input offset current		25°C		0.15	0.8	nA
I <sub>IO</sub>	input onset current		Full range			2.5	IIA
i	Input bias current		25°C		-12	-20	nA
I <sub>IB</sub>	input bias current		Full range			-30	IIA
V	Common mode input voltage range	Recommended range	25°C	-15		13.5	V
V <sub>ICR</sub>	Common-mode input voltage range	Recommended range	Full range	-14.9		13	V
M	Manifestore and the state of th	D 01:0	25°C	±13	±14		V
V <sub>OM</sub>	Maximum peak output voltage swing	$R_L = 2 k\Omega$	Full range	±12			V
		$V_{O} = \pm 10 \text{ V}, R_{L} = 600 \Omega$	25°C	0.8	2.5		
A <sub>VD</sub>	Large-signal differential voltage amplification	V 110 V D 010	25°C	1.5	8		$V/\mu V$
		$V_O = \pm 10 \text{ V}, \text{ R}_L = 2 \text{ k}\Omega$	Full range	0.5			
CMDD	Common mode rejection ratio	V <sub>IC</sub> = -15 V to 13.5 V	25°C	100	117		٩D
CMRR	Common-mode rejection ratio	V <sub>IC</sub> = -14.9 V to 13 V	Full range	97			dB
le.	Supply valtage rejection ratio (AVCC/AVIO)	V 10.V/to 110.V/	25°C	103	120		dB
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔVCC/ΔVIO)	$V_{CC+} = \pm 2 \text{ V to } \pm 18 \text{ V}$	Full range	100			uБ
	Channel separation	$V_O = \pm 10 \text{ V}, R_L = 2 \text{ k}\Omega$	25°C	123	140		dB
r <sub>id</sub>	Differential input resistance		25°C	100	400		ΜΩ
r <sub>ic</sub>	Common-mode input resistance		25°C		5		GΩ
	Supply current per amplifier		25°C		0.35	0.5	mΛ
I <sub>CC</sub>	Supply current per amplifier		Full range			0.6	mA

Full range is -55°C to 125°C.

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All typical values are at  $T_A = 25$ °C.

All typical values are at  $T_A$  = 25°C. On products compliant to MIL-PRF-38535, Class B, this parameter is not production tested.



### 6.14 Electrical Characteristics: LT1013AM, 5 V

at specified free-air temperature,  $V_{CC+} = 5 \text{ V}$ ,  $V_{CC-} = 0$ ,  $V_O = 1.4 \text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T <sub>A</sub> <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
		D 50.0	25°C		60	250	
V <sub>IO</sub>	Input offset voltage	$R_S = 50 \Omega$	Full range		250	900	μV
		$R_S = 50 \Omega$ , $V_{IC} = 0.1 V$	125°C		120	450	
	lanut affact aureat		25°C		0.2	1.3	nA
I <sub>IO</sub>	Input offset current		Full range			6	ΠA
	lanut biog growent		25°C		-15	-35	nA
I <sub>IB</sub>	Input bias current		Full range			-80	ΠA
V	Common mode input valtage vance	Decemberded serves	25°C	0		3.5	V
V <sub>ICR</sub>	CR Common-mode input voltage range	Recommended range	Full range	0		3	V
		Output low, No load	25°C		15	25	
		Output law B COO O to CND	25°C		5	10	
		Output low, $R_L = 600 \Omega$ to GND	Full range			15	
$V_{OM}$	Maximum peak output voltage swing	Output low, I <sub>sink</sub> = 1 mA	25°C		220	350	V
		Output high, No load	25°C	4	4.4		
		Output high B COO O to CND	25°C	3.4	4		
		Output high, $R_L = 600 \Omega$ to GND	Full range	3.2			
A <sub>VD</sub>	Large-signal differential voltage amplification	$V_O$ = 5 mV to 4 V, $R_L$ = 500 $\Omega$	25°C		1		V/µV
	Cumply coverent new complifier		25°C		0.31	0.45	A
I <sub>CC</sub>	Supply current per amplifier		Full range			0.55	mA

<sup>(1)</sup> Full range is -55°C to 125°C.

## 6.15 Electrical Characteristics: LT1013DM, ±15 V

at specified free-air temperature,  $V_{CC+} = \pm 15 \text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T <sub>A</sub> <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
.,	Land off and the	D 500	25°C		200	800	
$V_{IO}$	Input offset voltage	$R_S = 50 \Omega$	Full range			1000	μV
$\alpha_{VIO}$	Temperature coefficient of input offset voltage		Full range		0.5	2.5(3)	μV/°C
	Long-term drift of input offset voltage		25°C		0.5		μV/mo
	lanut offect current		25°C		0.2	1.5	Λ
I <sub>IO</sub>	Input offset current		Full range			5	nA
	lanut bion current		25°C		-15	-30	nA
I <sub>IB</sub>	Input bias current		Full range			-45	ΠA
.,	Common mode input veltage vance	Decemmended range	25°C	-15		13.5	V
V <sub>ICR</sub>	Common-mode input voltage range	Recommended range	Full range	-14.9		13	V
V <sub>OM</sub> N	Manifestore and a standard college	D. Alico	25°C	±12.5	±14		
	Maximum peak output voltage swing	$R_L = 2 k\Omega$	Full range	±11.5			V
		$V_{O} = \pm 10 \text{ V}, R_{L} = 600 \Omega$	25°C	0.5	2		
$A_{VD}$	Large-signal differential voltage amplification	V 110 V D 010	25°C	1.2	7		$V/\mu V$
		$V_O = \pm 10 \text{ V}, R_L = 2 \text{ k}\Omega$	Full range	0.25			
CMDD	Common made valentian vatio	V <sub>IC</sub> = −15 V to 13.5 V	25°C	97	114		dB
CMRR	Common-mode rejection ratio	$V_{IC} = -14.9 \text{ V to } 13 \text{ V}$	Full range	94			uБ
	Supply valtage rejection ratio (AVCC/AVIIC)	V 10.V/+o.140.V/	25°C	100	117		٩D
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔVCC/ΔVIO)	$V_{CC+} = \pm 2 \text{ V to } \pm 18 \text{ V}$	Full range	97			dB
	Channel separation	$V_O = \pm 10 \text{ V}, R_L = 2 \text{ k}\Omega$	25°C	120	137		dB
r <sub>id</sub>	Differential input resistance		25°C	70	300		МΩ
ic	Common-mode input resistance		25°C		4		GΩ
1	Comply suggest now amplifier		25°C		0.35	0.55	A
I <sub>CC</sub>	Supply current per amplifier		Full range			0.7	mA

Full range is -55°C to 125°C.

All typical values are at  $T_A = 25$ °C.

All typical values are at  $T_A$  = 25°C. On products compliant to MIL-PRF-38535, Class B, this parameter is not production tested. (3)



## 6.16 Electrical Characteristics: LT1013DM, 5 V

at specified free-air temperature,  $V_{CC+} = 5 \text{ V}$ ,  $V_{CC-} = 0$ ,  $V_{O} = 1.4 \text{ V}$ ,  $V_{IC} = 0$  (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T <sub>A</sub> <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT	
		B 50.0	25°C		250	950		
$V_{IO}$	Input offset voltage	$R_S = 50 \Omega$	Full range		800	2000	μV	
		$R_S = 50 \ \Omega, \ V_{IC} = 0.1 \ V$	125°C		560	1200		
	Input offeet gurrent		25°C		0.3	2	~ A	
I <sub>IO</sub>	Input offset current		Full range			10	nA	
	lanut biog gurrant		25°C		-18	-50	nA	
I <sub>IB</sub>	Input bias current		Full range			-120	ΠA	
V	Commence and institutions are	December and of some	25°C	0		3.5	V	
$V_{ICR}$	CR Common-mode input voltage range	Recommended range	Full range	0		3	V	
		Output low, No load	25°C		15	25		
		Output low B 600 O to CND			5	10		
		Output low, $R_L = 600 \Omega$ to GND	Full range			18		
$V_{OM}$	Maximum peak output voltage swing	Output low, I <sub>sink</sub> = 1 mA	25°C		220	350	V	
	5g	Output high, No load	25°C	4	4.4			
		Output high D 600 O to CND	25°C	3.4	4			
		Output high, $R_L = 600 \Omega$ to GND	Full range	3.1				
A <sub>VD</sub>	Large-signal differential voltage amplification	$V_{O}$ = 5 mV to 4 V, $R_{L}$ = 500 $\Omega$	25°C		1		V/µV	
	Cumbic ourrent ner amplifier		25°C		0.32	0.5	A	
I <sub>CC</sub>	Supply current per amplifier		Full range			0.65	mA	

## 6.17 Operating Characteristics

 $V_{CC\pm} = \pm 15 \ V, \ V_{IC} = 0, \ T_A = 25^{\circ}C$ 

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		0.2	0.4		V/µs
V	Facility land in a decision with a con-	f = 10 Hz		24		nV/√ <del>Hz</del>
V <sub>n</sub>	Equivalent input noise voltage	f = 1 kHz		22		Π <b>V</b> /γHZ
V <sub>N(PP)</sub>	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.55		μV
In	Equivalent input noise current	f = 10 Hz		0.07		pA/√Hz

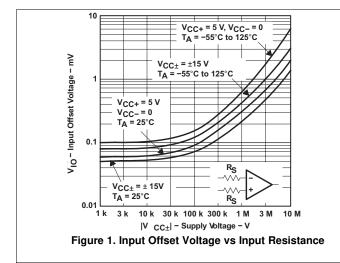
<sup>(1)</sup> Full range is  $-55^{\circ}$ C to 125°C. (2) All typical values are at  $T_A = 25^{\circ}$ C.



## 6.18 Typical Characteristics

#### Table 1. Table of Graphs

			FIGURE
V	lanut offeet voltege	vs Input Resistance	Figure 1
V <sub>IO</sub>	Input offset voltage	vs Temperature	Figure 2
$\Delta V_{IO}$	Change in input offset voltage	vs Time	Figure 3
I <sub>IO</sub>	Input offset current	vs Temperature	Figure 4
I <sub>IB</sub>	Input bias current	vs Temperature	Figure 5
V <sub>IC</sub>	Common-mode input voltage	vs Input bias current	Figure 6
	Differential valle on a constitution	vs Load resistance	Figure 7, Figure 8
A <sub>VD</sub>	Differential voltage amplification	vs Frequency	Figure 9, Figure 10
	Channel separation	vs Frequency	Figure 11
	Output saturation voltage	vs Temperature	Figure 12
CMRR	Common-mode rejection ratio	vs Frequency	Figure 13
k <sub>SVR</sub>	Supply-voltage rejection ratio	vs Frequency	Figure 14
I <sub>cc</sub>	Supply current	vs Temperature	Figure 15
los	Short-circuit output current	vs Time	Figure 16
V <sub>n</sub>	Equivalent input noise voltage	vs Frequency	Figure 17
In	Equivalent input noise current	vs Frequency	Figure 17
V <sub>N(PP)</sub>	Peak-to-peak input noise voltage	vs Time	Figure 18
	Dulas vasasas	Small signal	Figure 19, Figure 21
	Pulse response	Large signal	Figure 20, Figure 22, Figure 23
	Phase shift	vs Frequency	Figure 9



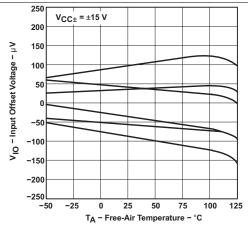
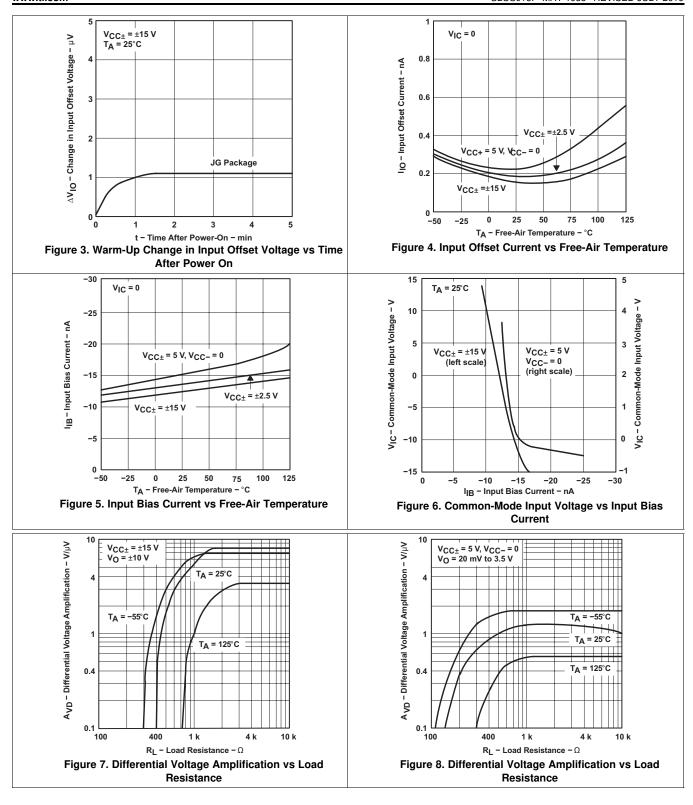
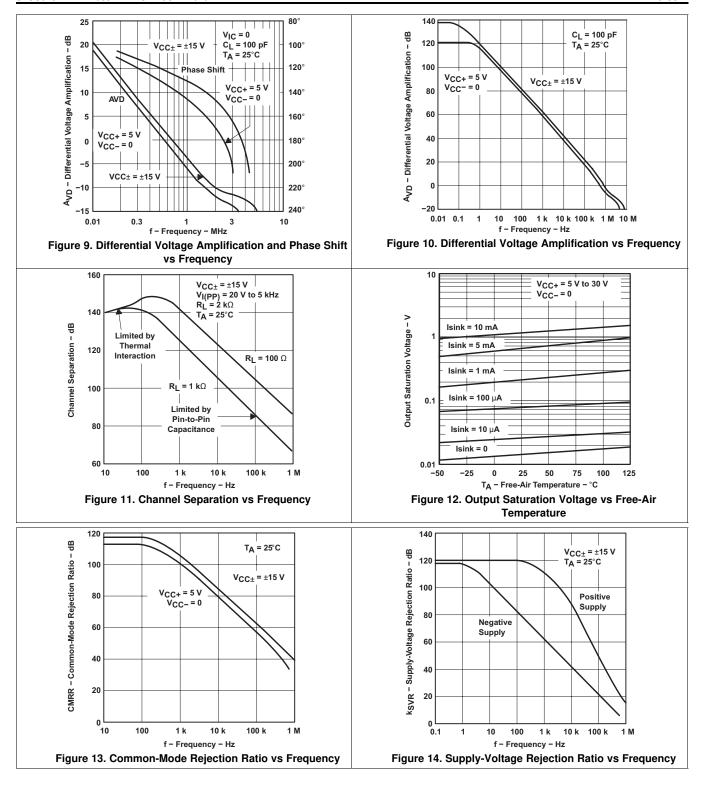


Figure 2. Input Offset Voltage of Representative Units vs Free-Air Temperature

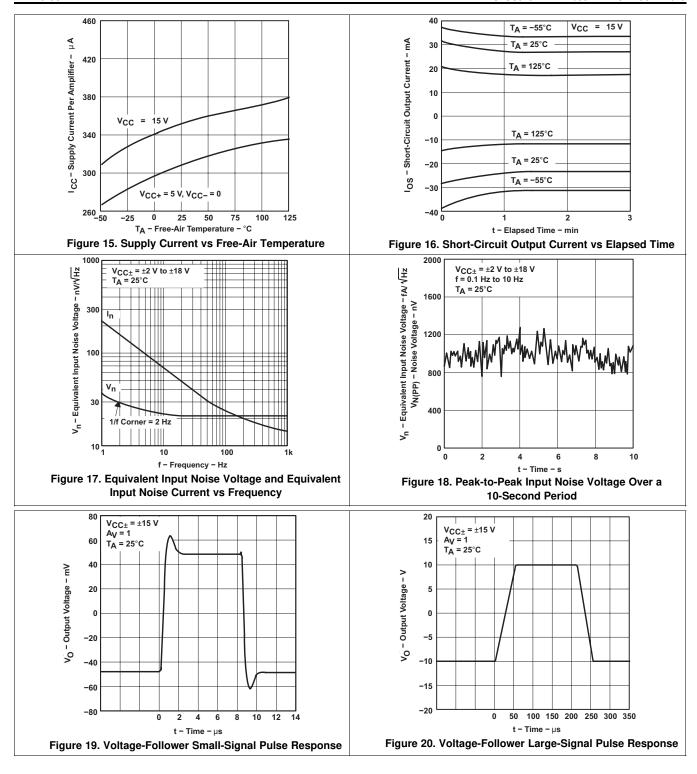




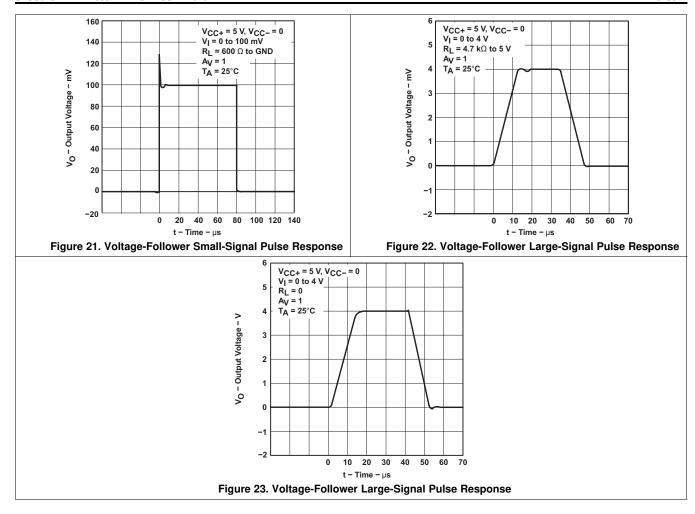












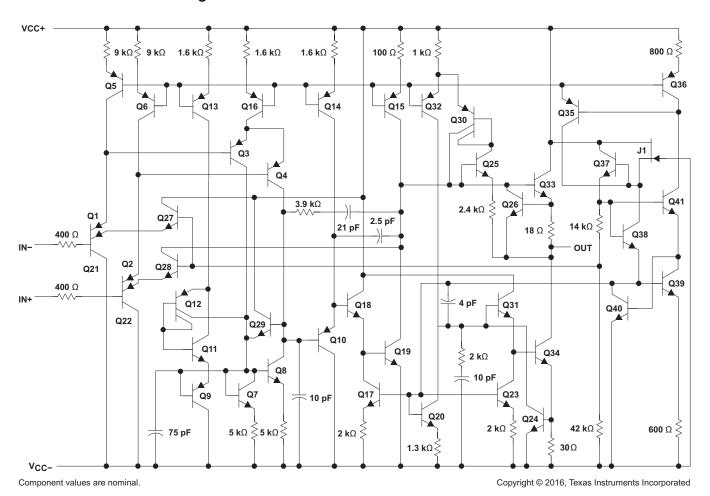


### 7 Detailed Description

#### 7.1 Overview

The LT1013x device is a dual operational amplifier with low natural  $V_{IO}$  without programming memory that can be erased. There are no side effects from active  $V_{IO}$  correction used by other op amps. The LT1013x has built-in protection for input voltage below  $V_{CC-}$ . However, an external resistance must be add to protect the LT1013x from input voltage greater than  $V_{CC+}$ .

#### 7.2 Functional Block Diagram



#### 7.3 Feature Description

#### 7.3.1 Input Resistors

For voltages less than  $V_{CC-}$ , a pair of 400- $\Omega$  resistors limit input current. These resistors have parasitic diodes to VCC+. Therefore, external series resistance is needed if input voltage exceed  $V_{CC+}$ 

#### 7.3.2 Output Stage

High output is provided by Q33 emitter for low output impedance. Q26 provides active current limiting for sourcing current.

Low output is provided by Q34 collector for lower output voltage near V<sub>CC-</sub> rail. Q24 provides active current limiting for sinking current.



#### **Feature Description (continued)**

#### 7.3.3 Low-Supply Operation

The minimum supply voltage for proper operation of the LT1013x is 3.4 V (three NiCad batteries). Typical supply current at this voltage is 290  $\mu$ A; therefore, power dissipation is only 1 mW per amplifier.

#### 7.3.4 Output Phase Reversal Protection

The LT1013x is fully specified for single-supply operation ( $V_{CC^-} = 0$ ). The common-mode input voltage range includes ground, and the output swings to within a few millivolts of ground.

Furthermore, the LT1013x has specific circuitry that addresses the difficulties of single-supply operation, both at the input and at the output. At the input, the driving signal can fall below 0 V, either inadvertently or on a transient basis. If the input is more than a few hundred millivolts below ground, the LT1013x is designed to deal with the following two problems that can occur:

- 1. On many other operational amplifiers, when the input is more than a diode drop below ground, unlimited current flows from the substrate (VCC- terminal) to the input, which can destroy the unit. On the LT1013x, the  $400-\Omega$  resistors in series with the input protect the device, even when the input is 5 V below ground.
- 2. When the input is more than 400 mV below ground (at  $T_A = 25$ °C), the input stage of similar operational amplifiers saturates, and phase reversal occurs at the output. This can cause lockup in servo systems. Because of unique phase-reversal protection circuitry (Q21, Q22, Q27, and Q28), the LT1013x outputs do not reverse, even when the inputs are at -1.5 V (see Figure 24).

This phase-reversal protection circuitry does not function when the other operational amplifier on the LT1013x is driven hard into negative saturation at the output. Phase-reversal protection does not work on amplifier 1 when amplifier 2 output is in negative saturation nor on amplifier 2 when amplifier 1 output is in negative saturation.

At the output, other single-supply designs either cannot swing to within 600 mV of ground or cannot sink more than a few micro amperes while swinging to ground. The all-npn output stage of the LT1013x maintains its low output resistance and high-gain characteristics until the output is saturated. In dual-supply operations, the output stage is free of crossover distortion.

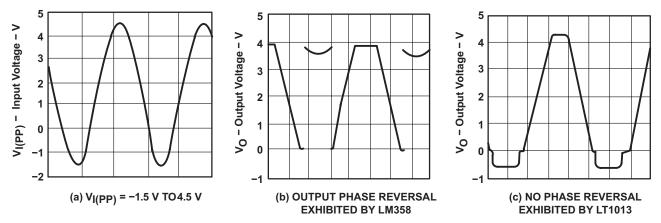


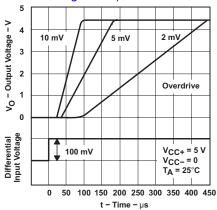
Figure 24. Voltage-Follower Response With Input Exceeding the Negative Common-Mode Input Voltage
Range

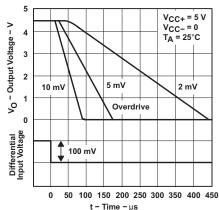


#### **Feature Description (continued)**

#### 7.3.4.1 Comparator Applications

The single-supply operation of the LT1013x is well suited for use as a precision comparator with TTL-compatible output. In systems using both operational amplifiers and comparators, the LT1013x can perform multiple duties (see Figure 25 and Figure 26).





**Various Input Overdrives** 

Figure 25. Low-to-High-Level Output Response for Figure 26. High-to-Low-Level Output Response for **Various Input Overdrives** 

#### 7.4 Device Functional Modes

The LT1013x dual operational amplifier amplifies a differential voltage applied to the inputs.



### 8 Application and Implementation

#### NOTE

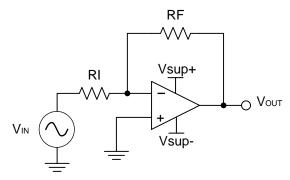
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The LT1013x operational amplifiers are useful in a wide range of signal conditioning applications where high DC accuracy is needed.

### 8.2 Typical Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.



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Figure 27. Application Schematic

#### 8.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application scales a signal of  $\pm 0.5$  V to  $\pm 1.8$  V. Setting the supply at  $\pm 12$  V is sufficient to accommodate this application.

#### 8.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using Equation 1 and Equation 2:

$$A_{v} = \frac{VOUT}{VIN} \tag{1}$$

$$A_v = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

Once the desired gain is determined, choose a value for RI or RF. Choosing a value in the  $k\Omega$  range is desirable because the amplifier circuit will use currents in the milliamp range. This ensures the part does not draw too much current. This example chooses 10  $k\Omega$  for RI, which means 36  $k\Omega$  is used for RF. This was determined by Equation 3.

$$A_v = -\frac{RF}{RI} \tag{3}$$



### **Typical Application (continued)**

#### 8.2.3 Application Curve

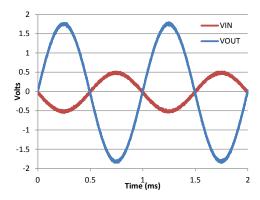


Figure 28. Input and Output Voltages of the Inverting Amplifier

### 9 Power Supply Recommendations

#### **CAUTION**

Supply voltages larger than 44 V for a single supply, or outside the range of ±22 V for a dual supply can permanently damage the device (see *Absolute Maximum Ratings*).

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout*.

#### 10 Layout

#### 10.1 Layout Guidelines

For best operational performance of the device, use quality PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the
  operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance
  power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for singlesupply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective
  methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes.
  A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital
  and analog grounds, paying attention to the flow of the ground current.
- Run the input traces as far away from the supply or output traces as possible to reduce parasitic coupling. If it
  is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed
  to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting
  input minimizes parasitic capacitance, as shown in Layout Guidelines.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.



#### 10.2 Layout Examples

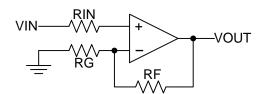


Figure 29. Operational Amplifier Schematic for Noninverting Configuration

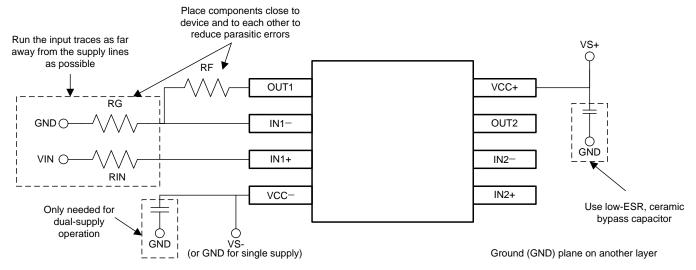


Figure 30. Operational Amplifier Board Layout for Noninverting Configuration



### 11 Device and Documentation Support

#### 11.1 Device Support

#### 11.1.1 Developmental Support

For developmental support, see the following:

LT1013-DIE

#### 11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LT1013	Click here	Click here	Click here	Click here	Click here
LT1013D	Click here	Click here	Click here	Click here	Click here
LT1013M	Click here	Click here	Click here	Click here	Click here
LT1013AM	Click here	Click here	Click here	Click here	Click here
LT1013-DIE	Click here	Click here	Click here	Click here	Click here

#### 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community T's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 11.5 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 11.7 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.



## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.





25-Oct-2016

#### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
5962-88760012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 88760012A LT1013AMFKB	Samples
5962-8876001PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8876001PA LT1013AM	Samples
5962-88760022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 88760022A LT1013MFKB	Samples
5962-8876002PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8876002PA LT1013M	Samples
LT1013AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 88760012A LT1013AMFKB	Samples
LT1013AMJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	LT1013AMJG	Samples
LT1013AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8876001PA LT1013AM	Samples
LT1013AMP	OBSOLETE	PDIP	Р	8		TBD	Call TI	Call TI	-55 to 125		
LT1013CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1013C	Samples
LT1013CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1013C	Samples
LT1013CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1013C	Samples
LT1013CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1013C	Samples
LT1013CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1013C	Samples
LT1013CP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LT1013CP	Samples
LT1013CPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LT1013CP	Samples
LT1013DD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1013D	Samples





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Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
LT1013DDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1013D	Samples
LT1013DDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1013D	Samples
LT1013DDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1013D	Samples
LT1013DDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1013D	Samples
LT1013DID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	1013DI	Samples
LT1013DIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	1013DI	Samples
LT1013DIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	1013DI	Samples
LT1013DIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	1013DI	Samples
LT1013DIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	1013DI	Samples
LT1013DIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	1013DI	Samples
LT1013DIP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 105	LT1013DIP	Samples
LT1013DIPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 105	LT1013DIP	Samples
LT1013DMD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	1013DM	Samples
LT1013DMDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	1013DM	Samples
LT1013DP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LT1013DP	Samples
LT1013DPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LT1013DP	Samples
LT1013IP	OBSOLETI	E PDIP	Р	8		TBD	Call TI	Call TI			
LT1013MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 88760022A LT1013MFKB	Samples



## PACKAGE OPTION ADDENDUM

25-Oct-2016

Orderable Device	Status	Package Type	_	Pins	_	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
LT1013MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	LT1013MJG	Samples
LT1013MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8876002PA LT1013M	Samples
LT1013MP	OBSOLETE	PDIP	Р	8		TBD	Call TI	Call TI	-55 to 125		
LT1013Y	OBSOLETE	DIESALE	Υ	0		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## **PACKAGE OPTION ADDENDUM**

25-Oct-2016

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF LT1013, LT1013M:

• Military: LT1013M

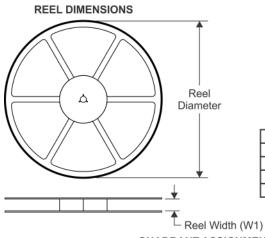
NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

## PACKAGE MATERIALS INFORMATION

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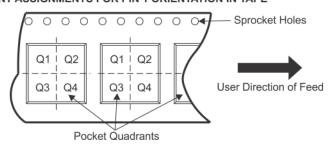
## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

All difficulties are florifical												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LT1013CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LT1013DDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LT1013DIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

www.ti.com 12-Feb-2016



\*All dimensions are nominal

7 III GITTIOTIOTOTIO GITO TIOTITITICI							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LT1013CDR	SOIC	D	8	2500	340.5	338.1	20.6
LT1013DDR	SOIC	D	8	2500	340.5	338.1	20.6
LT1013DIDR	SOIC	D	8	2500	340.5	338.1	20.6

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

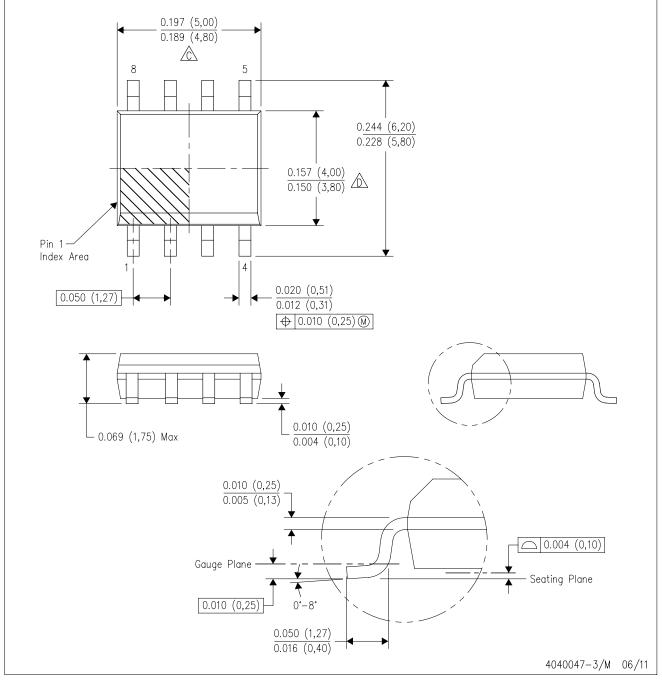


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



## D (R-PDSO-G8)

## PLASTIC SMALL OUTLINE

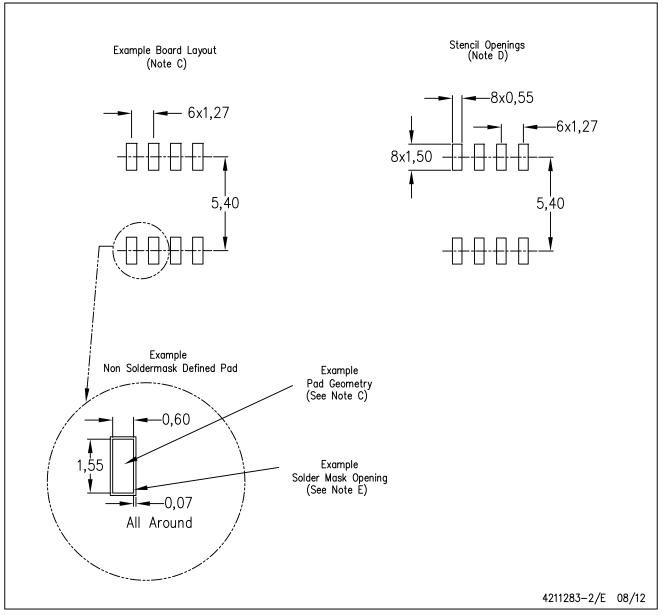


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



# D (R-PDSO-G8)

# PLASTIC SMALL OUTLINE

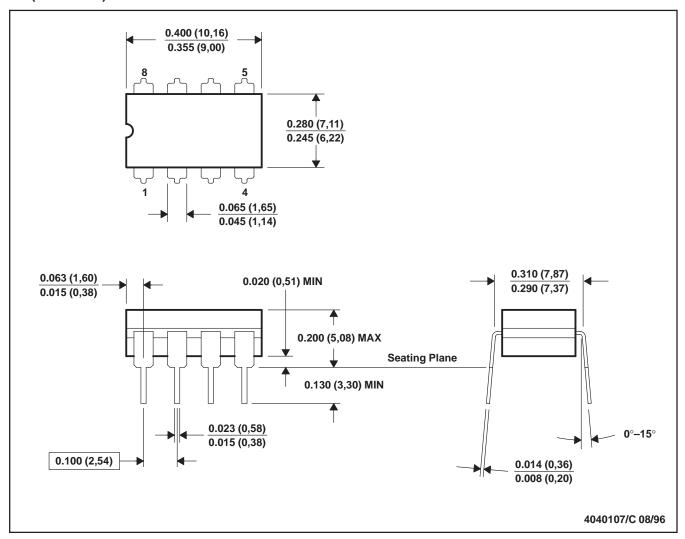


- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## JG (R-GDIP-T8)

#### **CERAMIC DUAL-IN-LINE**

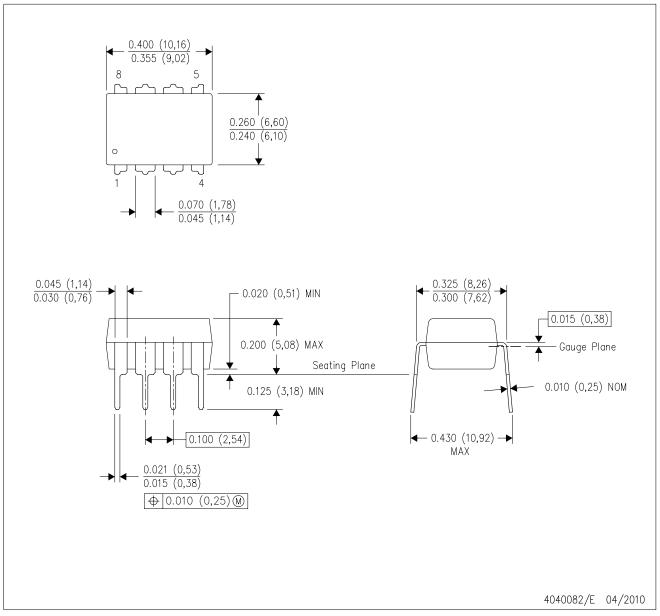


NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP1-T8

# P (R-PDIP-T8)

## PLASTIC DUAL-IN-LINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



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In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products	Applications
Products	Applications

Audio www.ti.com/audio Automotive and Transportation www.ti.com/automotive **Amplifiers** amplifier.ti.com Communications and Telecom www.ti.com/communications **Data Converters** dataconverter.ti.com Computers and Peripherals www.ti.com/computers **DLP® Products** www.dlp.com Consumer Electronics www.ti.com/consumer-apps DSP dsp.ti.com **Energy and Lighting** www.ti.com/energy Clocks and Timers www.ti.com/clocks Industrial www.ti.com/industrial Interface interface.ti.com Medical www.ti.com/medical Logic Security www.ti.com/security logic.ti.com

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