UNITRODE

bq2054

Lithium Ion Fast-Charge IC

Features

- Safe charge of Lithium Ion battery packs
- Voltage-regulated current-limited charging
- Fast charge terminated by selectable minimum current; safety backup termination on maximum time
- Charging continuously qualified by temperature and voltage limits
- Pulse-width modulation control ideal for high-efficiency switch-mode power conversion
- Direct LED control outputs display charge status and fault conditions

General Description

The bq2054 Lithium Ion Fast-Charge IC is designed to optimize charging of lithium ion (Li-Ion) chemistry batteries. A flexible pulse-width modulation regulator allows the bq2054 to control voltage and current during charging. The regulator frequency is set by an external capacitor for design flexibility. The switch-mode design keeps power dissipation to a minimum.

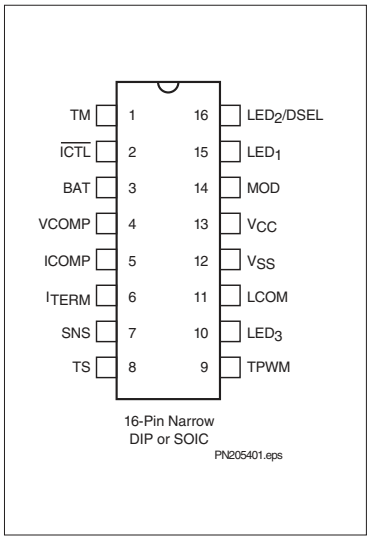
The bq2054 measures battery temperature using an external thermistor for charge qualification. Charging begins when power is applied or on battery insertion.

For safety, the bq2054 inhibits charging until the battery voltage and temperature are within configured limits. If the battery voltage is less than the low-voltage threshold, the bq2054 provides low-current conditioning of the battery.

A constant current-charging phase replenishes up to 70% of the charge capacity, and a voltage-regulated phase returns the battery to full. The charge cycle terminates when the charging current falls below a user-selectable current limit. For safety, charging terminates after maximum time and is suspended if the temperature is outside the preconfigured limits.

The bq2054 provides status indications of all charger states and faults for accurate determination of the battery and charge system conditions.

Pin Connections



16-Pin Narrow
DIP or SOIC

PN205401.eps

Pin Names

TM	Time-out programming input
$\overline{ICTL}$	Inrush current control output
BAT	Battery voltage input
VCOMP	Voltage loop comp input
ICOMP	Current loop comp input
I_{TERM}	Minimum current termination select input
SNS	Sense resistor input
TS	Temperature sense input
TPWM	Regulator timebase input
LED_3	Charge status output 3
LCOM	Common LED output
V_{SS}	System ground
V_{CC}	5.0V±10% power
MOD	Modulation control output
LED_1	Charge status output 1
LED_2/ DSEL	Charge status output 2/ Display select input

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Pin Descriptions

TM **Time-out programming input**

This input sets the maximum charge time. The resistor and capacitor values are determined using Equation 5. Figure 7 shows the resistor/capacitor connection.

$\overline{\text{ICTL}}$ **Inrush current control output**

$\overline{\text{ICTL}}$ is driven low during the fault or charge-complete states of the chip. It is used to disconnect the capacitor across the battery pack terminals, preventing inrush currents from tripping overcurrent protection features in the pack when a new battery is inserted.

BAT **Battery voltage input**

BAT is the battery voltage sense input. This potential is generally developed using a high-impedance resistor divider network connected between the positive and the negative terminals of the battery. See Figure 4 and Equation 1.

VCOMP **Voltage loop compensation input**

This input uses an external R-C network for voltage loop stability.

I_{TERM} **Minimum current termination select**

This three-state input is used to set I_{MIN} for fast charge termination. See Table 2.

ICOMP **Current loop compensation input**

This input uses an external R-C network for current loop stability.

SNS **Charging current sense input**

Battery current is sensed via the voltage developed on this pin by an external sense resistor, R_{SNS}, connected in series with the negative terminal of the battery pack. See Equation 6.

TS **Temperature sense input**

This input is used to monitor battery temperature. An external resistor divider network sets the lower and upper temperature thresholds. See Figure 6 and Equations 3 and 4.

TPWM **Regulation timebase input**

This input uses an external timing capacitor to ground to set the pulse-width modulation (PWM) frequency. See Equation 7.

LCOM **Common LED output**

Common output for $LED_{1–3}$. This output is in a high-impedance state during initialization to read programming input on DSEL.

MOD **Current-switching control output**

MOD is a pulse-width modulated push/pull output that is used to control the charging current to the battery. MOD switches high to enable current flow and low to inhibit current flow.

LED_1–LED_3 **Charger display status 1–3 outputs**

These charger status output drivers are for the direct drive of the LED display. Display modes are shown in Table 1. These outputs are tri-stated during initialization so that DSEL can be read.

DSEL **Display select input**

This three-level input controls the $LED_{1–3}$ charge display modes. See Table 1.

V_{CC} **V_{CC} supply**

5.0V, ± 10% power

V_{SS} **Ground**

Charge Algorithm

The bq2054 uses a two-phase fast charge algorithm. In phase 1, the bq2054 regulates constant current (I_{SNS} = I_{MAX}) until V_{CELL} (= V_{BAT} - V_{SNS}) rises to V_{REG}. The bq2054 then transitions to phase 2 and regulates constant voltage (V_{CELL} = V_{REG}) until the charging current falls below the programmed I_{MIN} threshold. The charging current must remain below I_{MIN} for 120 ± 40ms before a valid fast charge termination is detected. Fast charge then terminates, and the bq2054 enters the Charge Complete state. See Figures 1 and 2.

Charge Qualification

The bq2054 starts a charge cycle when power is applied while a battery is present or when a battery is inserted. Figure 2 shows the state diagram for pre-charge qualification and temperature monitoring. The bq2054 first checks that the battery temperature is within the allowed, user-configurable range. If the temperature is out of range, the bq2054 enters the Charge Pending state and waits until the battery temperature is within the allowed range. Charge Pending is enunciated by LED_3 flashing.

Thermal monitoring continues throughout the charge cycle, and the bq2054 enters the Charge Pending state when the temperature out of range. (There is one exception; if the bq2054 is in the Fault state—see below—the out-of-range temperature is not recognized until the bq2054 leaves the Fault state.) All timers are suspended (but not reset) while the bq2054 is in Charge Pending. When the temperature comes back into range, the bq2054 returns to the point in the charge cycle where the out-of-range temperature was detected.

When the temperature is valid, the bq2054 then regulates current to I_{COND} (=I_{MAX}/5). After an initial holdoff period t_{HO} (which prevents the chip from reacting to transient voltage spikes that may occur when charge current is first applied), the chip begins monitoring V_{CELL}. If V_{CELL} does not rise to at least V_{MIN} before the expiration of time-out limit t_{MTO} (e.g. the cell has failed short), the bq2054 enters the Fault state. If V_{MIN} is achieved before expiration of the time limit, the chip begins fast charging.

Once in the Fault state, the bq2054 waits until V_{CC} is cycled or a new battery insertion is detected. It then starts a new charge cycle and begins the qualification process again.

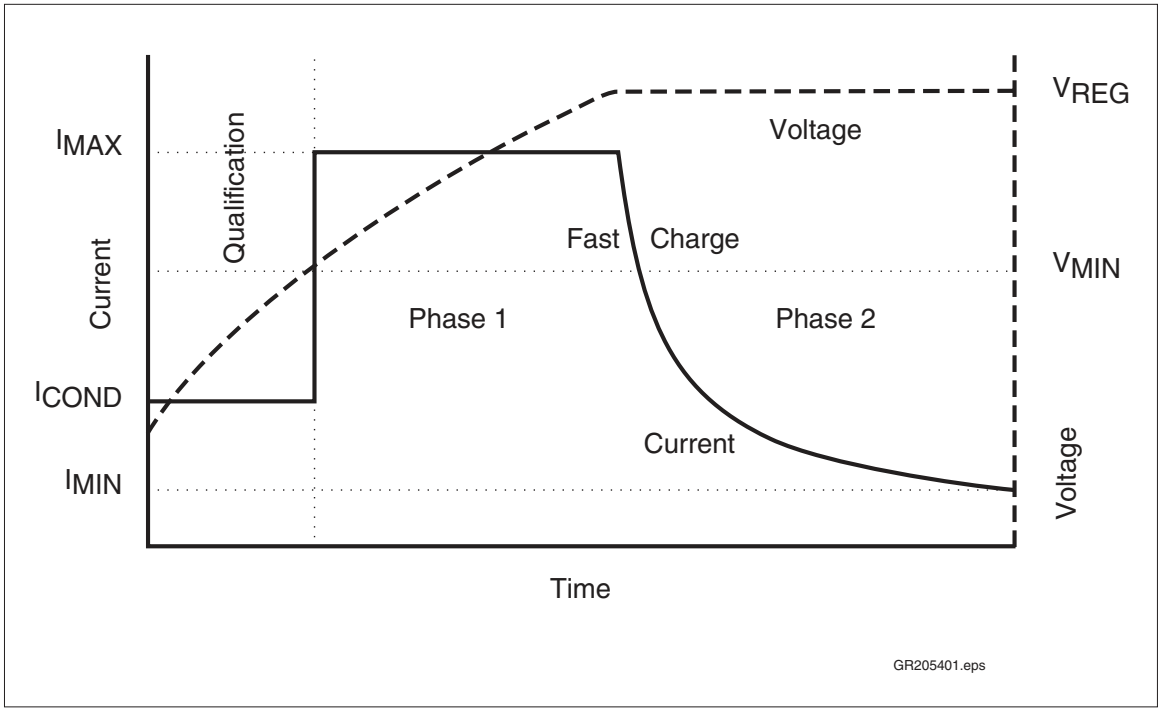


Figure 1. bq2054 Charge Algorithm

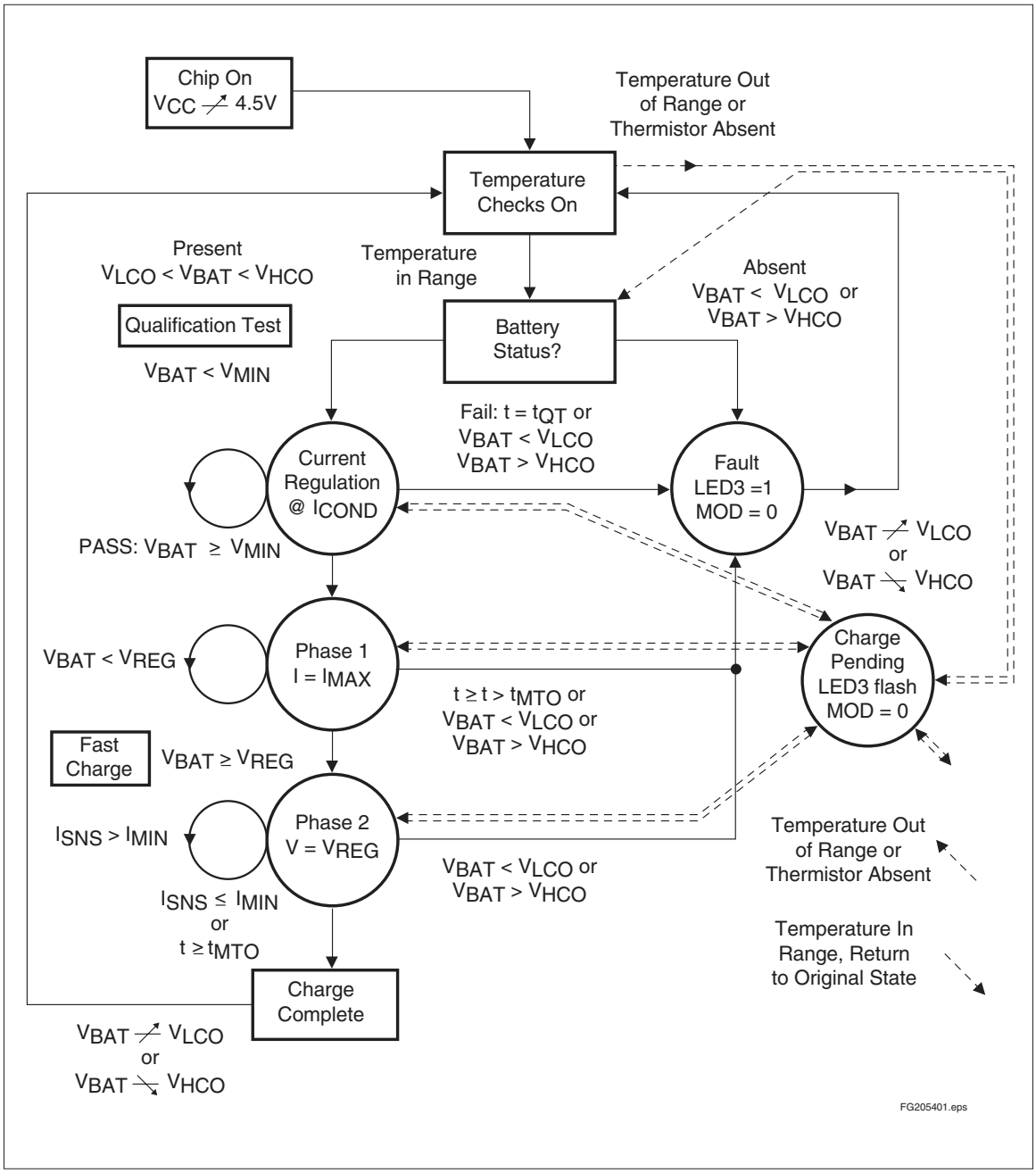


Figure 2. bq2054 State Diagram

Charge Status Display

Charge status is enunciated by the LED driver outputs LED_1–LED_3. Three display modes are available in the bq2054; the user selects a display mode by configuring pin DSEL. Table 1 shows the three display modes.

The bq2054 does not distinguish between an over-voltage fault and a "battery absent" condition. The bq2054 enters the Fault state, enunciated by turning on LED_3, whenever the battery is absent. The bq2054, therefore, gives an indication that the charger is on even when no battery is in place to be charged.

Configuring the Display Mode and I_{MIN}

$DSEL/LED_2$ is a bi-directional pin with two functions; it is an LED driver pin as an output and a programming pin as an input. The selection of pull-up, pull-down, or no pull resistor programs the display mode on DSEL per Table 1. The bq2054 latches the programming data sensed on the DSEL input when any one of the following three events occurs:

1. V_{CC} rises to a valid level.
2. The bq2054 leaves the Fault state.
3. The bq2054 detects battery insertion.

The LEDs go blank for approximately 750ms (typical) while new programming data is latched.

Table 1. bq2054 Display Output Summary

Mode	Charge Action State	LED_1	LED_2	LED_3
DSEL = 0 (Mode 1)	Battery absent or over-voltage fault	Low	Low	High
	Pre-charge qualification	Flash	Low	Low
	Fast charging	High	Low	Low
	Charge complete	Low	High	Low
	Charge pending (temperature out of range)	X	X	Flash
	Charging fault	X	X	High
DSEL = 1 (Mode 2)	Battery absent or over-voltage fault	Low	Low	High
	Pre-charge qualification	High	High	Low
	Fast charge	Low	High	Low
	Charge complete	High	Low	Low
	Charge pending (temperature out of range)	X	X	Flash
	Charging fault	X	X	High
DSEL = Float (Mode 3)	Battery absent or over-voltage fault	Low	Low	High
	Pre-charge qualification	Flash	Flash	Low
	Fast charge: current regulation	Low	High	Low
	Fast charge: voltage regulation	High	High	Low
	Charge complete	High	Low	Low
	Charge pending (temperature out of range)	X	X	Flash
	Charging fault	X	X	High

Note: 1 = V_{CC}; 0 = V_{SS}; X = LED state when fault occurred; Flash = ⅙ sec. low, ⅙ sec high.

Fast charge terminates when the charging current drops below a minimum current threshold programmed by the value of I_{TERM} (see Table 2) and remains below that level for 120 ± 40ms.

Table 2. I_{MIN} Termination Thresholds

I_{TERM}	I_{MIN}
0	$I_{MAX}/10$
1	$I_{MAX}/20$
Float	$I_{MAX}/30$

Figure 3 shows the bq2054 configured for display mode 2 and $I_{MIN} = I_{MAX}/10$.

Voltage and Current Monitoring

The bq2054 monitors battery pack voltage at the BAT pin. The user must implement a voltage divider between the positive and negative terminals of the battery pack to present a scaled battery pack voltage to the BAT pin. The bq2054 also uses the voltage across a sense resistor (R_{SNS}) between the negative terminal of the battery pack and ground to monitor the current into the pack. See Figure 4 for the configuration of this network.

The resistor values are calculated from the following:

Equation 1

$$\frac{RB1}{RB2} = \frac{N * V_{REG}}{2.05V} - 1$$

where:

- N = Number of cells in series
- V_{REG} = Desired fast-charging voltage per cell

These parameters are typically specified by the battery manufacturer. The total resistance presented across the battery pack by RB1 + RB2 should be between 150kΩ and 1MΩ. The minimum value ensures that the divider network does not drain the battery excessively when the power source is disconnected. Exceeding the maximum value increases the noise susceptibility of the BAT pin.

The current sense resistor, R_{SNS} (see Figure 5), determines the fast charge current. The value of R_{SNS} is given by the following:

Equation 2

$$I_{MAX} = \frac{0.250V}{R_{SNS}}$$

where:

- I_{MAX} = Desired maximum charge current

Hold-Off Period

Both V_{HCO} and I_{MIN} terminations are ignored during the first 1.33 ± 0.19 seconds of both the Charge Qualification and Fast Charge phases. This condition prevents premature termination due to voltage spikes that may occur when charge is first applied.

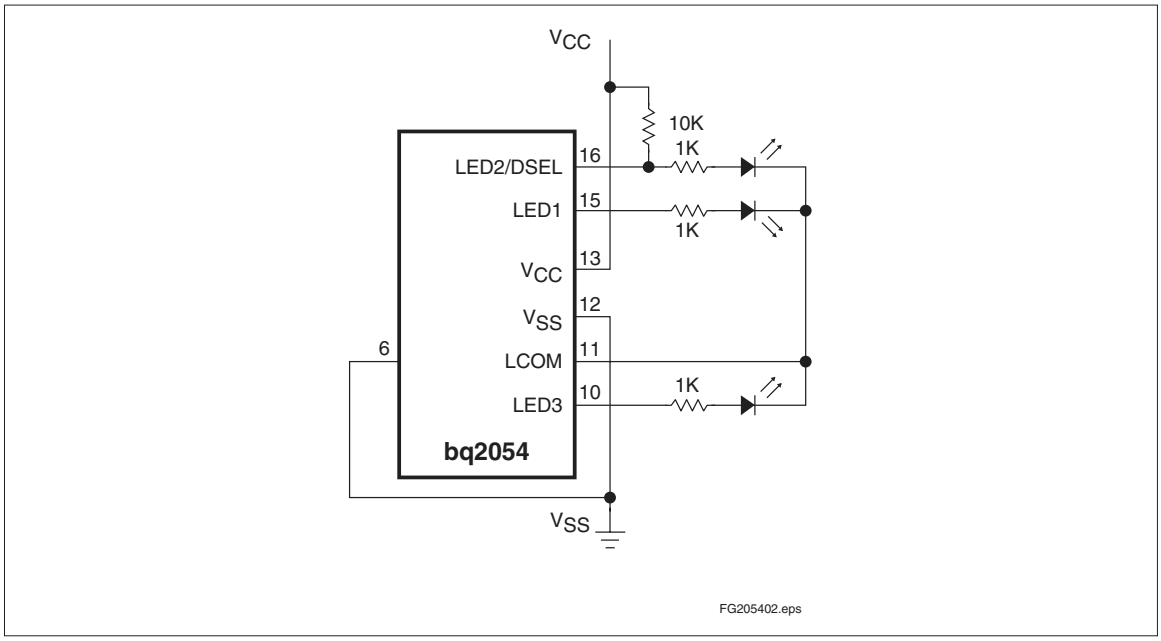


Figure 3. Configured Display Mode/IMIN Threshold

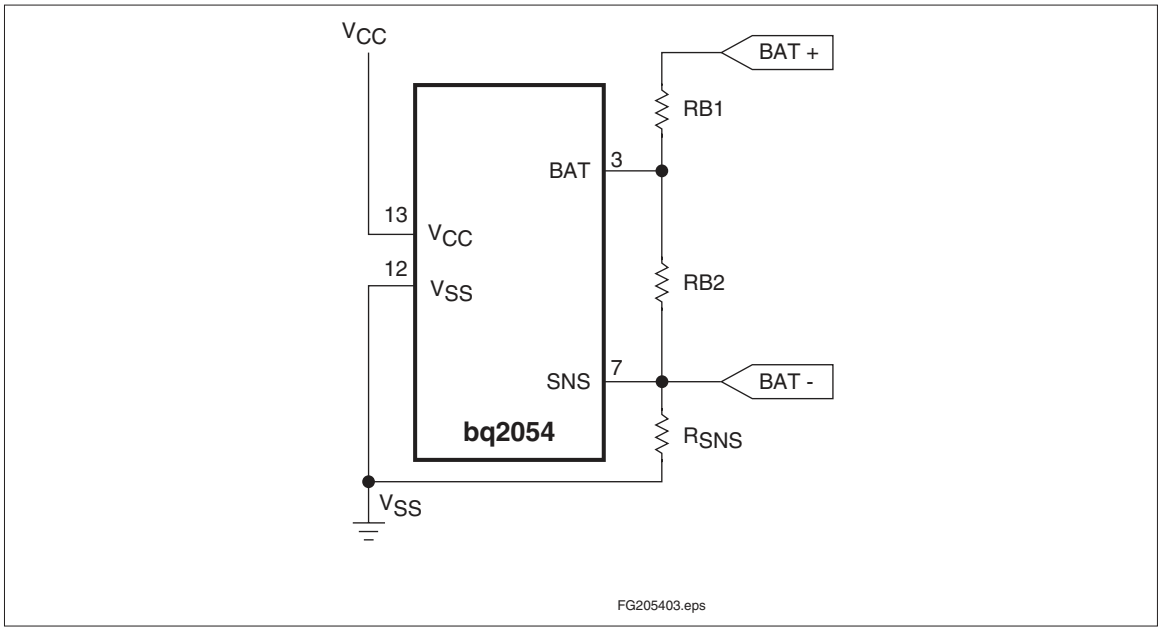


Figure 4. Configuring the Battery Divider

Battery Insertion and Removal

V_{CELL} is interpreted by the bq2054 to detect the presence or absence of a battery. The bq2054 determines that a battery is present when V_{CELL} is between the High-Voltage Cutoff (V_{HCO} = V_{REG} + 0.25V) and the Low-Voltage Cutoff (V_{LCO} = 0.8V). When V_{CELL} is outside this range, the bq2054 determines that no battery is present and transitions to the Fault state. Transitions into and out of the range between V_{LCO} and V_{HCO} are treated as battery insertions and removals, respectively. The V_{HCO} limit also implicitly serves as an overvoltage charge termination.

Inrush Current Control

Whenever the bq2054 is in the fault or charge-complete state, the $\overline{ICTL}$ output is driven low. This output can be used to disconnect the capacitor usually present in the charger across the positive and negative battery terminals, preventing the cap from supplying large inrush currents to a newly inserted battery. Such inrush currents may trip the overcurrent protection circuitry usually present in Li-Ion battery packs.

Temperature Monitoring

The bq2054 monitors temperature by examining the voltage presented between the TS and SNS pins by a resistor network that includes a Negative Temperature Coefficient (NTC) thermistor. Resistance variations around that value are interpreted as being proportional to the battery temperature (see Figure 6).

The temperature thresholds used by the bq2054 and their corresponding TS pin voltage are:

- TCO (Temperature Cutoff): Higher limit of the temperature range in which charging is allowed. V_{TCO} = 0.4 * V_{CC}
- HTF (High-Temperature Fault): Threshold to which temperature must drop after temperature cutoff is exceeded before charging can begin again. V_{HTF} = 0.44 * V_{CC}
- LTF (Low-Temperature Fault): Lower limit of the temperature range in which charging is allowed. V_{LTF} = 0.6 * V_{CC}

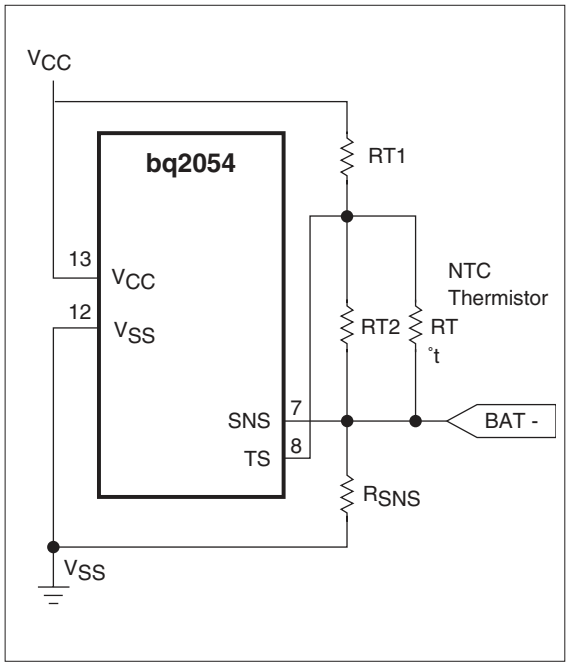


Figure 5. Configuring Temperature Sensing

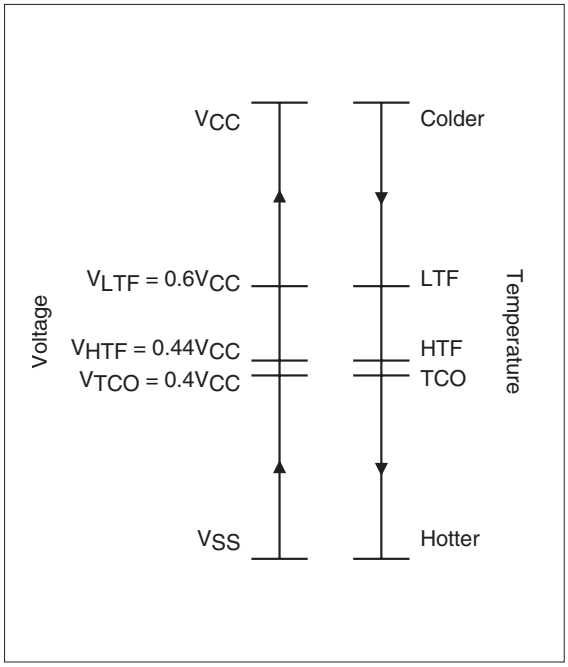


Figure 6. Voltage Equivalent of Temperature

A resistor-divider network can be implemented that presents the defined voltage levels to the TS pin at the desired temperatures (see Figure 6).

The equations for determining RT1 and RT2 are:

Equation 3

$$0.6 * V_{CC} = \frac{(V_{CC} - 0.250)}{1 + \frac{RT1 * (RT2 + R_{LTF})}{(RT2 * R_{LTF})}}$$

Equation 4

$$0.44 = \frac{1}{1 + \frac{RT1 * (RT2 + R_{HTF})}{(RT2 * R_{HTF})}}$$

where:

- R_{LTF} = thermistor resistance at LTF
- R_{HTF} = thermistor resistance at HTF

TCO is determined by the values of RT1 and RT2. 1% resistors are recommended.

Disabling Temperature Sensing

Temperature sensing can be disabled by placing 10kΩ resistors between TS and SNS and between SNS and V_{CC}.

Maximum Time-Out

MTO is programmed from 1 to 24 hours by an R-C network on the TM pin (see Figure 7) per the equation:

Equation 5

$$t_{MTO} = 0.5 * R * C$$

Where R is in kΩ and C is in µF, t_{MTO} is in hours. The maximum value for C (0.1µF) is typically used.

The MTO timer is reset at the beginning of fast charge and when fast charge transitions from the current regulated to the voltage regulated mode. If MTO expires during the current regulated phase, the bq2054 enters the Fault state and terminates charge. If the MTO timer expires during the voltage regulated phase, fast charging terminates and the bq2054 enters the Charge Complete state.

The MTO timer is suspended (but not reset) during the out-of-range temperature (Charge Pending) state.

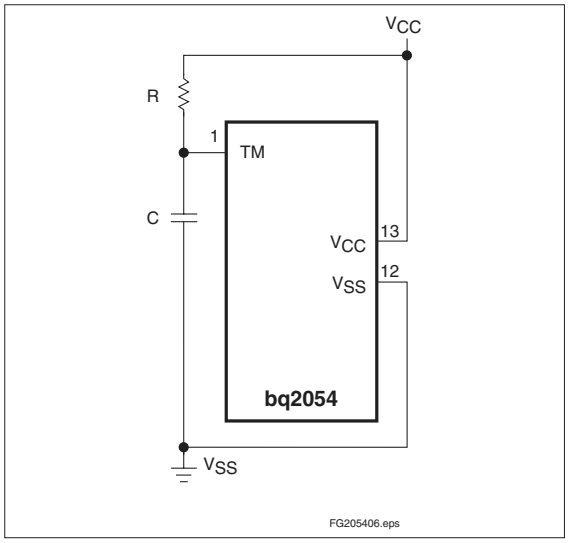


Figure 7. R-C Network for Setting MTO

Charge Regulation

The bq2054 controls charging through pulse-width modulation of the MOD output pin, supporting both constant-current and constant-voltage regulation. Charge current is monitored at the SNS pin, and charge voltage is monitored at the BAT pin. These voltages are compared to an internal reference, and the MOD output modulated to maintain the desired value.

Voltage at the SNS pin is determined by the value of resistor R_{SNS}, so nominal regulated current is set by:

Equation 6

$$I_{MAX} = 0.250V/R_{SNS}$$

The switching frequency of the MOD output is determined by an external capacitor (CPWM) between the pin TPWM and ground, per the following:

Equation 7

$$F_{PWM} = 0.1/C_{PWM}$$

Where C is in µF and F is in kHz. A typical switching rate is 100kHz, implying C_{PWM} = 0.001µF. MOD pulse width is modulated between 0 and 90% of the switching period.

To prevent oscillation in the voltage and current control loops, frequency compensation networks (C or R-C) are typically required on the V_{COMP} and I_{COMP} pins (respectively).

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec. max.

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} = 5V ±10%)

Symbol	Parameter	Rating	Unit	Tolerance	Notes
V_{REF}	Internal reference voltage	2.05	V	1%	T_A = 25°C
	Temperature coefficient	-0.5	mV/°C	10%	
V_{LTF}	TS maximum threshold	0.6 * V_{CC}	V	±0.03V	Low-temperature fault
V_{HTF}	TS hysteresis threshold	0.44 * V_{CC}	V	±0.03V	High-temperature fault
V_{TCO}	TS minimum threshold	0.4 * V_{CC}	V	±0.03V	Temperature cutoff
V_{HCO}	High cutoff voltage	2.3V	V	1%	
V_{MIN}	Under-voltage threshold at BAT	0.2 * V_{CC}	V	±0.03V	
V_{LCO}	Low cutoff voltage	0.8	V	±0.03V	
V_{SNS}	Current sense at SNS	0.250	V	10%	I_{MAX}
		0.050	V	10%	I_{COND}

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{TEMP}	Temperature sense voltage	0	-	V_{CC}	V	V_{TS} - V_{SNS}
V_{CELL}	Per cell battery voltage input	0	-	V_{CC}	V	V_{BAT} - V_{SNS}
I_{CC}	Supply current	-	2	4	mA	Outputs unloaded
I_{IZ}	DSEL tri-state open detection	-2	-	2	µA	Note 2
	I_{TERM} tri-state open detection	-2		2	µA	
V_{IH}	Logic input high	V_{CC}-0.3	-	-	V	DSEL, I_{TERM}
V_{IL}	Logic input low	-	-	V_{SS}+0.3	V	DSEL, I_{TERM}
V_{OH}	LED_{1-3}, $\overline{ICTL}$, output high	V_{CC}-0.8	-	-	V	$I_{OH} \leq 10mA$
	MOD output high	V_{CC}-0.8	-	-	V	$I_{OH} \leq 10mA$
V_{OL}	LED_{1-3}, $\overline{ICTL}$, output low	-	-	V_{SS}+0.8V	V	$I_{OL} \leq 10mA$
	MOD output low	-	-	V_{SS}+0.8V	V	$I_{OL} \leq 10mA$
	LCOM output low	-	-	V_{SS+}0.5	V	$I_{OL} \leq 30mA$
I_{OH}	LED_{1-3}, $\overline{ICTL}$, source	-10	-	-	mA	$V_{OH} = V_{CC}$-0.5V
	MOD source	-5.0	-	-	mA	$V_{OH} = V_{CC}$-0.5V
I_{OL}	LED_{1-3}, $\overline{ICTL}$, sink	10	-	-	mA	$V_{OL} = V_{SS}$+0.5V
	MOD sink	5	-	-	mA	$V_{OL} = V_{SS}$+0.8V
	LCOM sink	30	-	-	mA	$V_{OL} = V_{SS}$+0.5V
I_{IL}	DSEL logic input low source	-	-	+30	µA	V = V_{SS} to V_{SS}+ 0.3V, Note 2
	I_{TERM} logic input low source	-	-	+70	µA	V = V_{SS} to V_{SS}+ 0.3V
I_{IH}	DSEL logic input high source	-30	-	-	µA	V = V_{CC} - 0.3V to V_{CC}
	I_{TERM} logic input high source	-70	-	-	µA	V = V_{CC} - 0.3V to V_{CC}

Notes: 1. All voltages relative to V_{SS} except where noted.

2. Conditions during initialization after V_{CC} applied.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
R_{BATZ}	BAT pin input impedance	50	-	-	MΩ	
R_{SNSZ}	SNS pin input impedance	50	-	-	MΩ	
R_{TSZ}	TS pin input impedance	50	-	-	MΩ	
R_{PROG1}	Soft-programmed pull-up or pull-down resistor value (for programming)	-	-	10	kΩ	DSEL
R_{PROG2}	Pull-up or pull-down resistor value	-	-	3	kΩ	I_{TERM}
R_{MTO}	Charge timer resistor	20	-	480	kΩ	

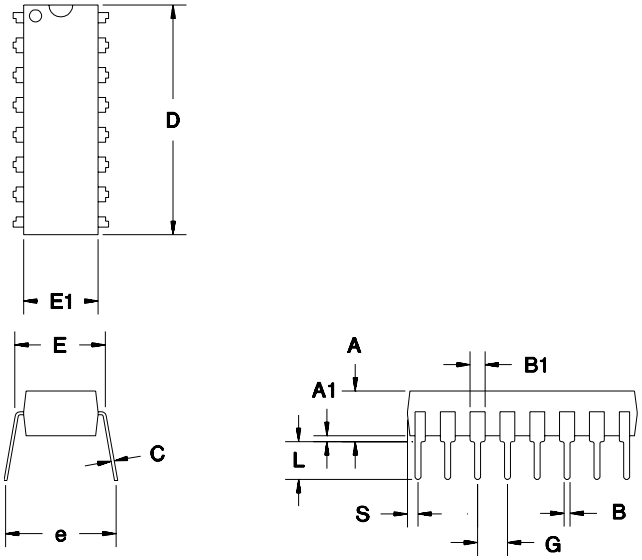
Timing (TA = TOPR; VCC = 5V ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{MTO}	Charge time-out range	1	-	24	hours	See Figure 7
t_{QT}	Pre-charge qual test time-out period	-	t_{MTO}	-	-	
t_{HO}	Termination hold-off period	1.14	-	1.52	sec.	
t_{IMIN}	Min. current detect filter period	80		160	msec.	
F_{PWM}	PWM regulator frequency range	-	100		kHz	C_{PWM} = 0.001µF (equation 7)

Capacitance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
C_{MTO}	Charge timer capacitor	-	-	0.1	µF
C_{PWM}	PWM R-C capacitance	-	0.001	-	µF

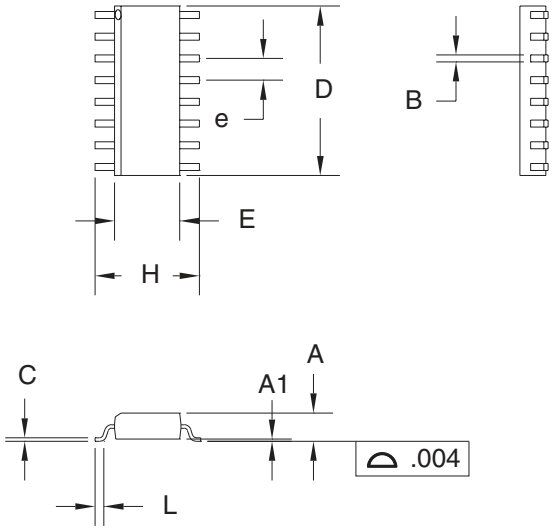
16-Pin DIP Narrow (PN)



16-Pin PN (0.300" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	0.740	0.770	18.80	19.56
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.020	0.040	0.51	1.02

16-Pin SOIC Narrow (SN)



16-Pin SN (0.150" SOIC)

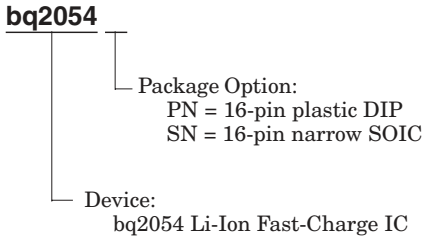
Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.385	0.400	9.78	10.16
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	5, 7, 8, 10	Value Change	Changed V_{SNS} and I_{MAX}
2	5, 10	Value Change	Changed V_{REF}
3	10	Coefficient Addition	Temperature coefficient added
4	5	New state diagram	Diagram inserted
4	1, 2, 8, 12	NC pin replaced with $\overline{ICTL}$	
4	3, 5, 13	Termination hold-off period added I_{MIN} detect filtering added	
5	11	V_{HCO} Rating changed to 2.3V V_{HCO} Tolerance changed to 1%	Changed values for V_{HCO}
6	13	t_{QT} in Timing Specifications	t_{QT} changed from (0.16 * t_{MTO}) to t_{MTO}
7	5	I_{TERM} in Table 2	Z changes to Float
7	8	Figure 6	RB1 and RB2 changed to RT1 and RT2
8	10	T_{OPR}	Deleted industrial temperature range.

Notes: Change 3 = April 1996 C changes from Dec. 1995 B.
Change 4 = Sept. 1996 D changes from April 1996 C.
Change 5 = Nov. 1996 E changes from Sept. 1996 D.
Change 6 = Oct. 1997 F changes from Nov. 1996 E.
Change 7 = Oct. 1997 G changes from Oct. 1997 F.
Change 8 = June 1999 H changes from Oct. 1997 G.

Ordering Information



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ2054PN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	0 to 0	2054PN-G	Samples
BQ2054PNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	0 to 0	2054PN-G	Samples
BQ2054SN	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 0	2054 (-G, G)	Samples
BQ2054SNTR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		2054 (-G, G)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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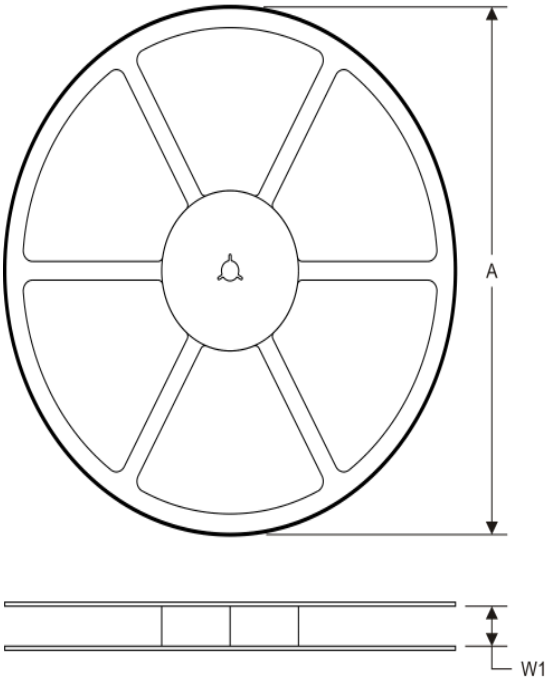
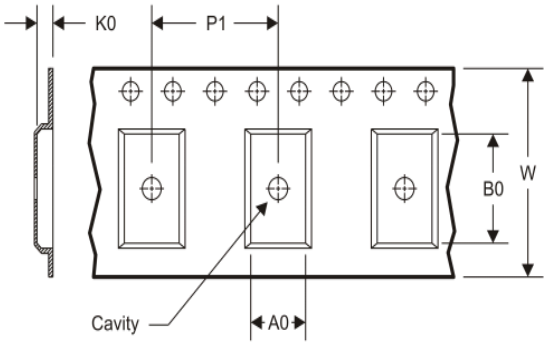
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



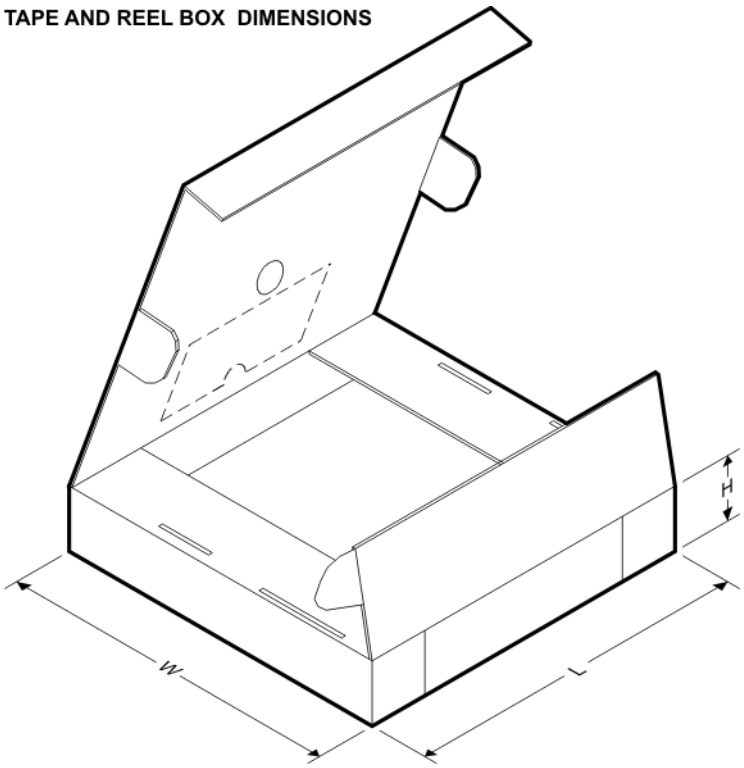
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2054SNTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

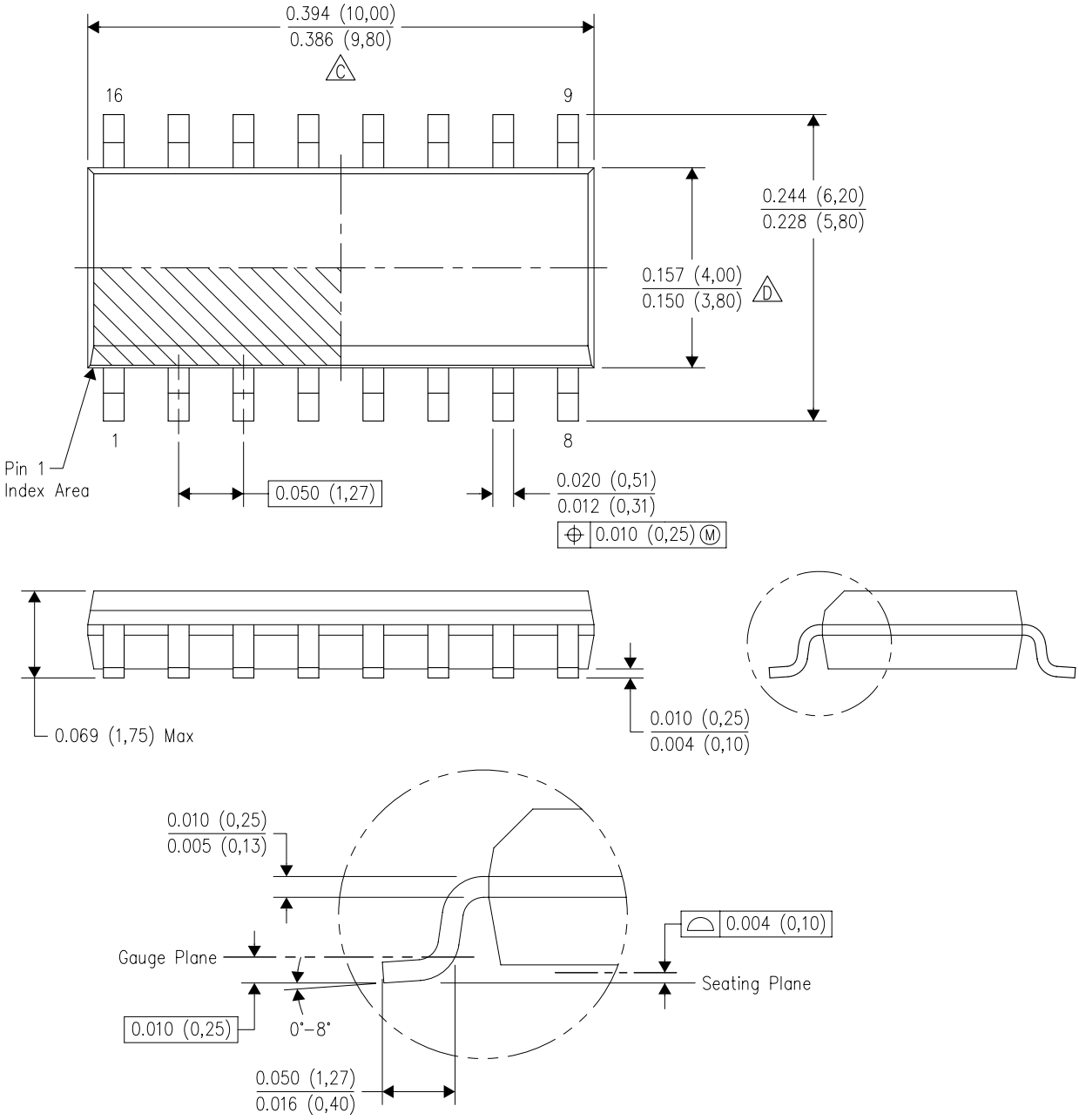
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

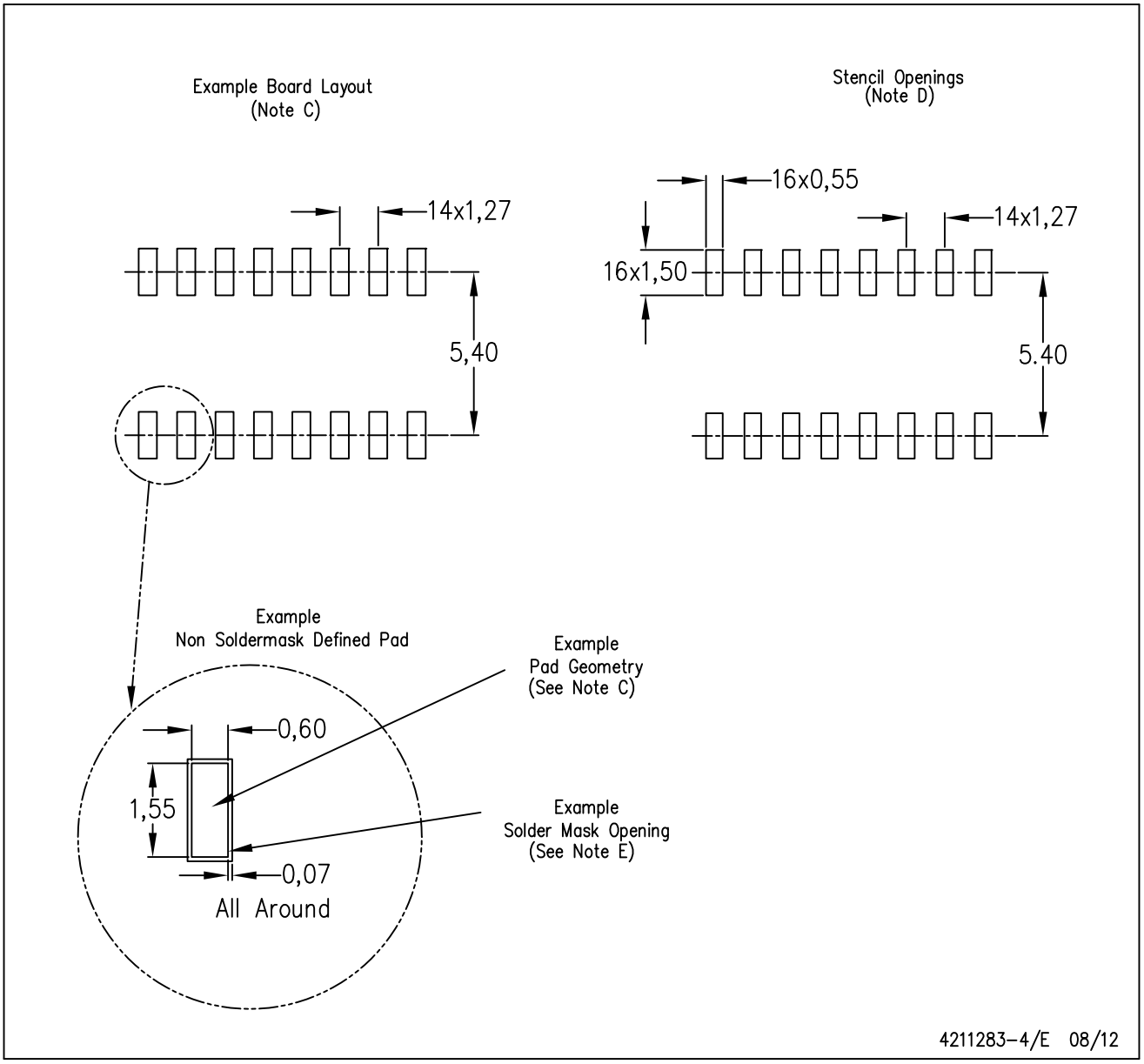
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2054SNTR	SOIC	D	16	2500	367.0	367.0	38.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

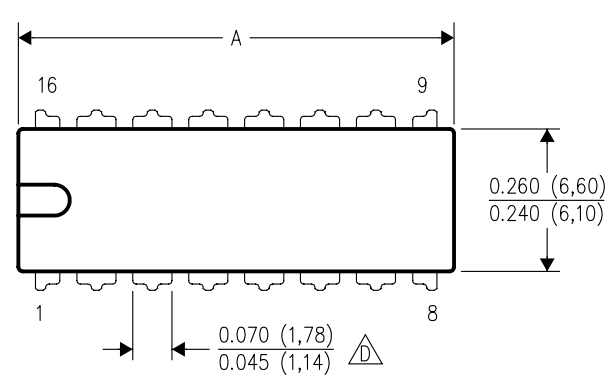


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

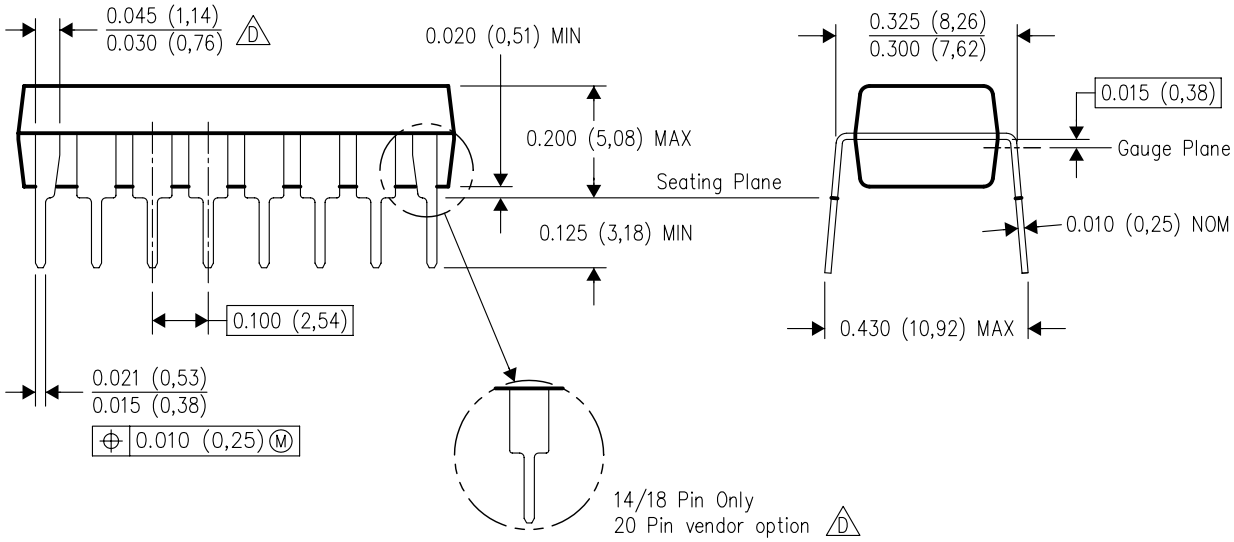
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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