## Features

- Fast Read Access Time – 55 ns
- Low Power CMOS Operation
  - 100 µA Maximum Standby
  - 35 mA Maximum Active at 5 MHz
- JEDEC Standard Packages
  - 40-lead PDIP
  - 44-lead PLCC
  - 40-lead VSOP
- Direct Upgrade from 512-Kbit and 1-Mbit (AT27C516 and AT27C1024) EPROMs
- 5V ±10% Power Supply
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid Programming Algorithm – 50 µs/Word (Typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Industrial Temperature Range

# 2-Megabit (128K x 16) OTP EPROM

# AT27C2048

## 1. Description

The AT27C2048 is a low-power, high-performance 2,097,152-bit one-time programmable read-only memory (OTP EPROM) organized 128K by 16 bits. It requires a single 5V power supply in normal read mode operation. Any word can be accessed in less than 55 ns, eliminating the need for speed-reducing WAIT states. The by-16 organization makes this part ideal for high-performance 16 and 32 bit microprocessor systems.

In read mode, the AT27C2048 typically consumes 15 mA. Standby mode supply current is typically less than 10 µA.

The AT27C2048 is available in industry-standard JEDEC-approved one-time programmable (OTP) plastic PDIP, PLCC, and VSOP packages. The device features two-line control ($\overline{CE}$, $\overline{OE}$) to eliminate bus contention in high-speed systems.

With high density 128K word storage capability, the AT27C2048 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's AT27C2048 has additional features that ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 50 µs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry-standard programming equipment to select the proper programming algorithms and voltages.

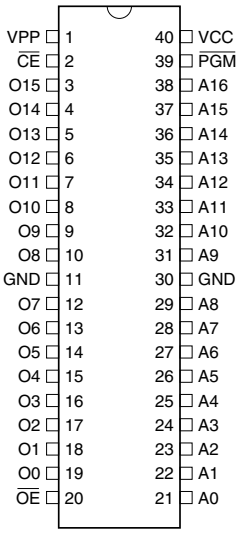
0632F–EPROM–12/07

# 2. Pin Configurations

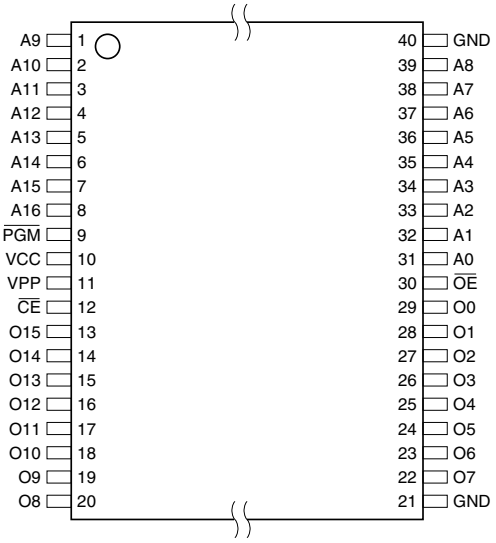
| Pin Name | Function |
|---|---|
| A0 - A16 | Addresses |
| O0 - O15 | Outputs |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $\overline{PGM}$ | Program Strobe |
| NC | No Connect |
| DC | Don't Connect |

Note: Both GND pins must be connected.

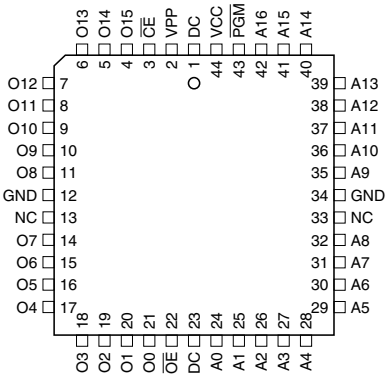
## 2.1 40-lead PDIP Top View




## 2.2 40-lead VSOP (Type 1) Top View




## 2.3 44-lead PLCC Top View

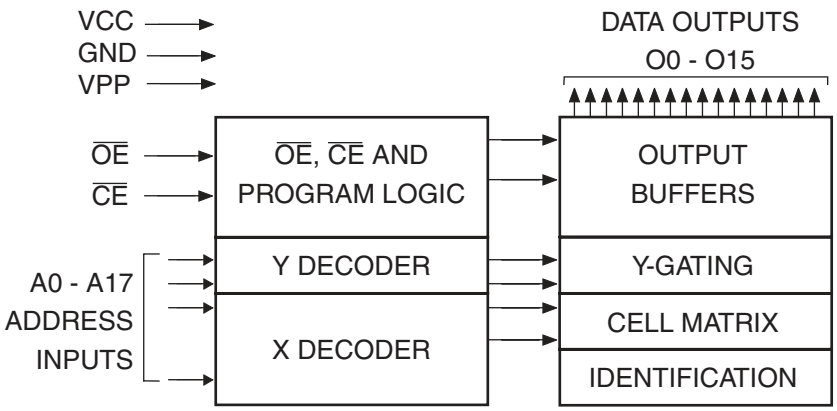



Note: Note: PLCC package pins 1 and 23 are Don't Connect.

## 3. System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the $V_{CC}$ and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the $V_{CC}$ and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

## 4. Block Diagram




## 5. Absolute Maximum Ratings*

| | |
|---|---|
| Temperature Under Bias | -55° C to +125° C |
| Storage Temperature | -65° C to +150° C |
| Voltage on Any Pin with Respect to Ground | -2.0V to +7.0V(1) |
| Voltage on A9 with Respect to Ground | -2.0V to +14.0V(1) |
| $V_{PP}$ Supply Voltage with Respect to Ground | -2.0V to +14.0V(1) |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Maximum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is $V_{CC}$ + 0.75V DC which may overshoot to +7.0V for pulses of less than 20 ns.

## 6. Operating Modes

| Mode/Pin | $\overline{CE}$ | $\overline{OE}$ | $\overline{PGM}$ | Ai | $V_{PP}$ | Outputs |
|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | X[1] | Ai | X[1] | $D_{OUT}$ |
| Output Disable | X | $V_{IH}$ | X | X | X | High Z |
| Standby | $V_{IH}$ | X | X | X | X[5] | High Z |
| Rapid Program[2] | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | Ai | $V_{PP}$ | $D_{IN}$ |
| PGM Verify | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | Ai | $V_{PP}$ | $D_{OUT}$ |
| PGM Inhibit | $V_{IH}$ | X | X | X | $V_{PP}$ | High Z |
| Product Identification[4] | $V_{IL}$ | $V_{IL}$ | X | A9 = $V_H$[3]<br>A0 = $V_{IH}$ or $V_{IL}$<br>A1 - A16 = $V_{IL}$ | $V_{CC}$ | Identification Code |

Notes:
1. X can be $V_{IL}$ or $V_{IH}$.
2. Refer to the Programming characteristics.
3. $V_H$ = 12.0 ±0.5V.
4. Two identifier words may be selected. All Ai inputs are held low ($V_{IL}$), except A9, which is set to $V_H$, and A0, which is toggled low ($V_{IL}$) to select the Manufacturer's Identification word and high ($V_{IH}$) to select the Device Code word.
5. Standby $V_{CC}$ current ($I_{SB}$) is specified with $V_{PP} = V_{CC}$. $V_{CC} > V_{PP}$ will cause a slight increase in $I_{SB}$.

## 7. DC and AC Operating Conditions for Read Operation

| | AT27C2048 | |
|---|---|---|
| | -55 | -90 |
| Industrial Operating Temperature (Case) | -40° C - 85° C | -40° C - 85° C |
| $V_{CC}$ Power Supply | 5V ± 10% | 5V ± 10% |

## 8. DC and Operating Characteristics for Read Operation

| Symbol | Parameter | Condition | Min | Max | Units |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN}$ = 0V to $V_{CC}$ | | ±1 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = 0V to $V_{CC}$ | | ±5 | µA |
| $I_{PP1}$[2] | $V_{PP}$[1] Read/Standby Current | $V_{PP} = V_{CC}$ | | 10 | µA |
| $I_{SB}$ | $V_{CC}$[1] Standby Current | $I_{SB1}$ (CMOS)<br>$\overline{CE} = V_{CC} \pm 0.3V$ | | 100 | µA |
| | | $I_{SB2}$ (TTL)<br>$\overline{CE}$ = 2.0 to $V_{CC}$ + 0.5V | | 1 | mA |
| $I_{CC}$ | $V_{CC}$ Active Current | f = 5 MHz, $I_{OUT}$ = 0 mA, $\overline{CE} = V_{IL}$ | | 35 | mA |
| $V_{IL}$ | Input Low Voltage | | -0.6 | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1 mA | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -400 µA | 2.4 | | V |

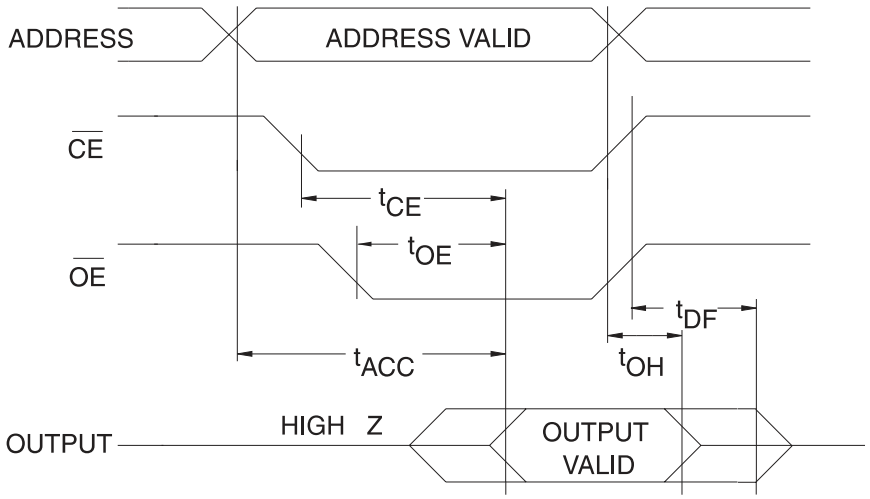
Notes:
1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$, and removed simultaneously or after $V_{PP}$
2. $V_{PP}$ may be connected directly to $V_{CC}$, except during programming. The supply current would then be the sum of $I_{CC}$ and $I_{PP}$

## 9. AC Characteristics for Read Operation

| Symbol | Parameter | Condition | AT27C2048 | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -55 | | -90 | | |
| | | | Min | Max | Min | Max | |
| $t_{ACC}$[3] | Address to Output Delay | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$ | | 55 | | 90 | ns |
| $t_{CE}$[2] | $\overline{CE}$ to Output Delay | $\overline{OE}$ = $V_{IL}$ | | 55 | | 90 | ns |
| $t_{OE}$[2][3] | $\overline{OE}$ to Output Delay | $\overline{CE}$ = $V_{IL}$ | | 20 | | 35 | ns |
| $t_{DF}$[4][5] | $\overline{OE}$ or $\overline{CE}$ High to Output Float, Whichever Occurred First | | | 20 | | 20 | ns |
| $t_{OH}$[4] | Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First | | 7 | | 0 | | ns |

Note: 2, 3, 4, 5. See the AC Waveforms for Read Operation diagram.

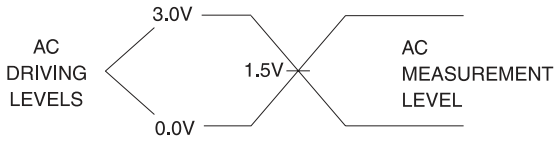
## 10. AC Waveforms for Read Operation[1]




Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to $t_{CE}$ - $t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{CE}$.
3. $\overline{OE}$ may be delayed up to $t_{ACC}$ - $t_{OE}$ after the address is valid without impact on $t_{ACC}$.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

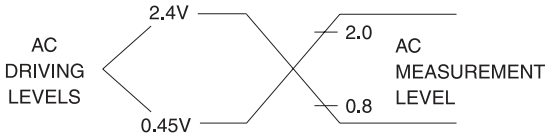
## 11. Input Test Waveforms and Measurement Levels

For -55 devices only:



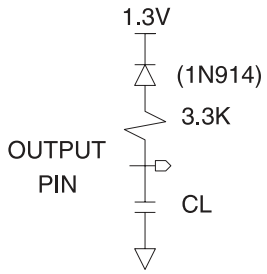

$t_R$, $t_F$ < 5 ns (10% to 90%)

For -90 devices:




$t_R$, $t_F$ < 20 ns (10% to 90%)

## 12. Output Test Load



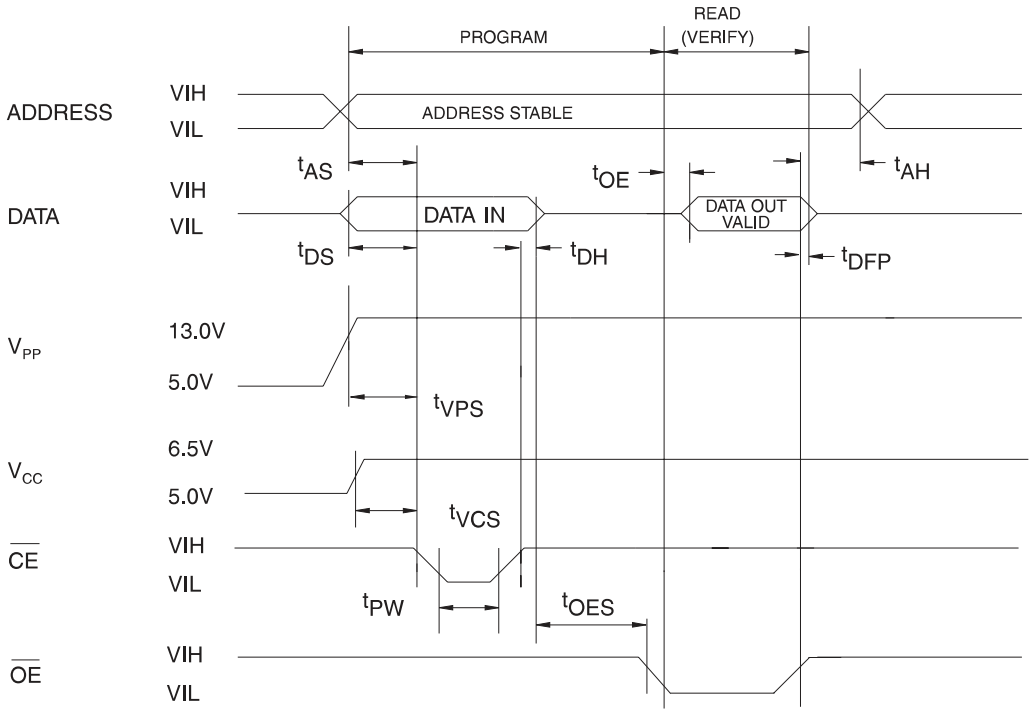

Note: CL = 100 pF including jig capacitance, except for the -55 devices, where CL = 30 pF.

## 13. Pin Capacitance

| Symbol | Typ | Max | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | 4 | 10 | pF | $V_{IN}$ = 0V |
| $C_{OUT}$ | 8 | 12 | pF | $V_{OUT}$ = 0V |

Note: Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

## 14. Programming Waveforms[1]




Notes:
1. The Input Timing Reference is 0.8V for $V_{IL}$ and 2.0V for $V_{IH}$.
2. $t_{OE}$ and $t_{DFP}$ are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C2048, a 0.1 µF capacitor is required across $V_{PP}$ and ground to suppress spurious voltage transients.

## 15. DC Programming Characteristics

$T_A$ = 25 ±5°C, $V_{CC}$ = 6.5 ±0.25V, $V_{PP}$ = 13.0 ±0.25V

| Symbol | Parameter | Test Conditions | Limits | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $I_{LI}$ | Input Load Current | $V_{IN} = V_{IL}, V_{IH}$ | | ±10 | µA |
| $V_{IL}$ | Input Low Level | | -0.6 | 0.8 | V |
| $V_{IH}$ | Input High Level | | 2.0 | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1 mA | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -400 µA | 2.4 | | V |
| $I_{CC2}$ | $V_{CC}$ Supply Current (Program and Verify) | | | 50 | mA |
| $I_{PP2}$ | $V_{PP}$ Supply Current | $\overline{CE} = V_{IL}$ | | 30 | mA |
| $V_{ID}$ | A9 Product Identification Voltage | | 11.5 | 12.5 | V |

## 16. AC Programming Characteristics

$T_A$ = 25 ± 5°C, $V_{CC}$ = 6.5 ± 0.25V, $V_{PP}$ = 13.0 ±0.25V

| Symbol | Parameter | Test Conditions[1] | Limits | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $t_{AS}$ | Address Setup Time | Input Rise and Fall Times (10% to 90%) 20 ns<br>Input Pulse Levels 0.45V to 2.4V<br>Input Timing Reference Level 0.8V to 2.0V<br>Output Timing Reference Level 0.8V to 2.0V | 2 | | µs |
| $t_{OES}$ | $\overline{OE}$ Setup Time | | 2 | | µs |
| $t_{DS}$ | Data Setup Time | | 2 | | µs |
| $t_{AH}$ | Address Hold Time | | 0 | | µs |
| $t_{DH}$ | Data Hold Time | | 2 | | µs |
| $t_{DFP}$ | $\overline{OE}$ High to Output Float Delay[2] | | 0 | 130 | ns |
| $t_{VPS}$ | $V_{PP}$ Setup Time | | 2 | | µs |
| $t_{VCS}$ | $V_{CC}$ Setup Time | | 2 | | µs |
| $t_{PW}$ | $\overline{PGM}$ Program Pulse Width[3] | | 47.5 | 52.5 | µs |
| $t_{OE}$ | Data Valid from $\overline{OE}$ | | | 150 | ns |
| $t_{PRT}$ | $V_{PP}$ Pulse Rise Time During Programming | | 50 | | ns |

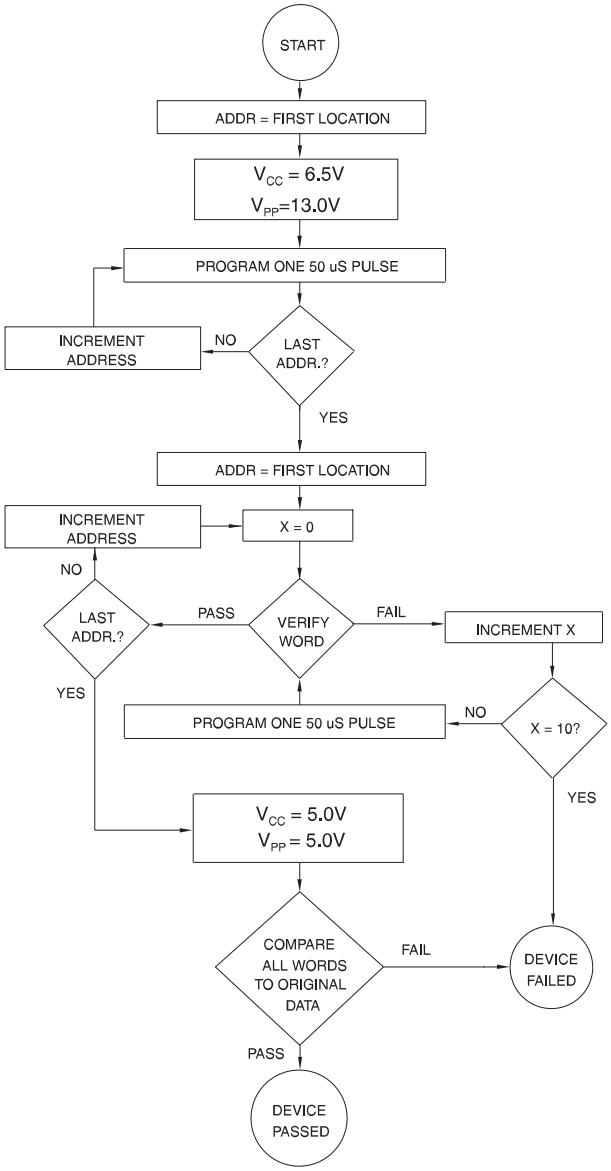
Notes:
1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.
3. Program Pulse width tolerance is 50 µsec ± 5%.

## 17. Atmel's 27C2048 Intergrated Product Identification Code

| Codes | Pins | | | | | | | | | | Hex Data |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | A0 | O15-O8 | O7 | O6 | O5 | O4 | O3 | O2 | O1 | O0 | |
| Manufacturer | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 001E |
| Device Type | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 00F7 |

## 18. Rapid Programming Algorithm

A 50 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. $V_{CC}$ is raised to 6.5V and $V_{PP}$ is raised to 13.0V. Each address is first programmed with one 50 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 50 µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. $V_{PP}$ is then lowered to 5.0V and $V_{CC}$ to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.



# 19. Ordering Information

## 19.1 Standard Package

| $t_{ACC}$ (ns) | $I_{CC}$ (mA) | | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| | Active | Standby | | | |
| 55 | 35 | 0.1 | AT27C2048-55JI<br>AT27C2048-55PI<br>AT27C2048-55VI | 44J<br>40P6<br>40V[1] | Industrial<br>(-40° C to 85° C) |
| 90 | 35 | 0.1 | AT27C2048-90JI<br>AT27C2048-90PI<br>AT27C2048-90VI | 44J<br>40P6<br>40V[1] | Industrial<br>(-40° C to 85° C) |

Note: Not recommended for new designs. Use Green package option.

## 19.2 Green Package (Pb/Halide-free)

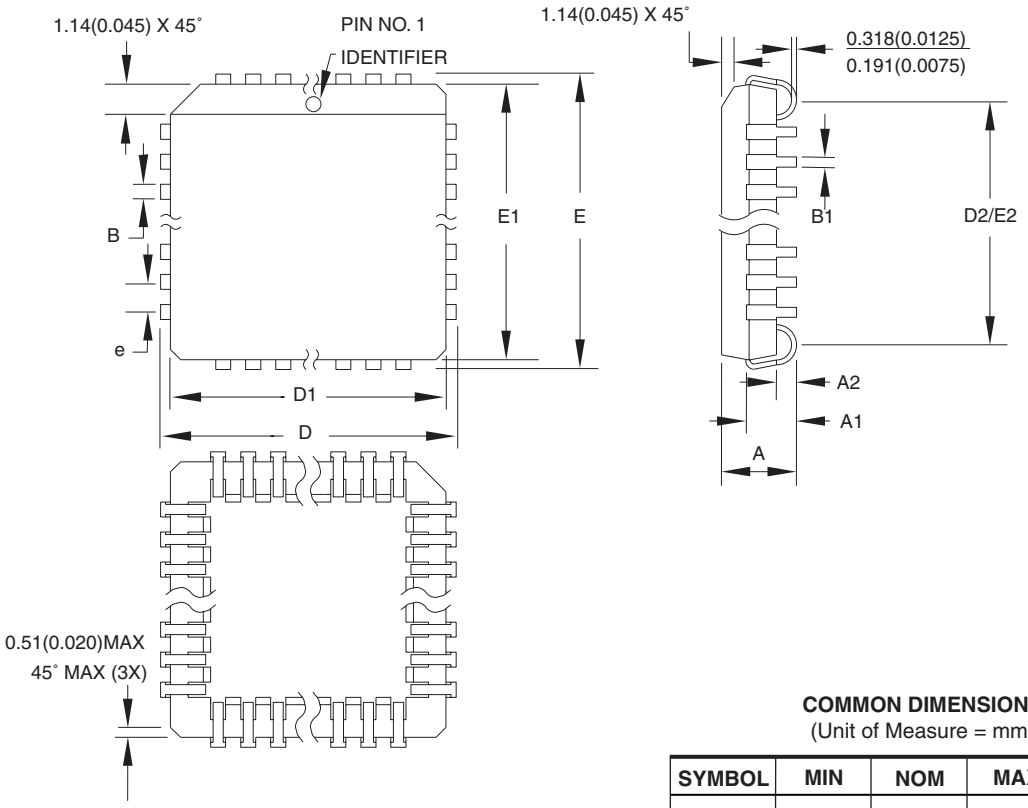
| $t_{ACC}$ (ns) | $I_{CC}$ (mA) | | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| | Active | Standby | | | |
| 55 | 35 | 0.1 | AT27C2048-55JU<br>AT27C2048-55PU | 44J<br>40P6 | Industrial<br>(-40° C to 85° C) |
| 90 | 35 | 0.1 | AT27C2048-90JU<br>AT27C2048-90PU | 44J<br>40P6 | Industrial<br>(-40° C to 85° C) |

Note: 1. The 40-lead VSOP package is not recommended for new designs.

| Package Type | |
|---|---|
| **44J** | 44-lead, Plastic J-leaded Chip Carrier (PLCC) |
| **40P6** | 40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP) |
| **40V** | 40-lead, Plastic Thin Small Outline Package (VSOP) |

# 20. Packaging Information

## 20.1 44J – PLCC




**COMMON DIMENSIONS**
(Unit of Measure = mm)

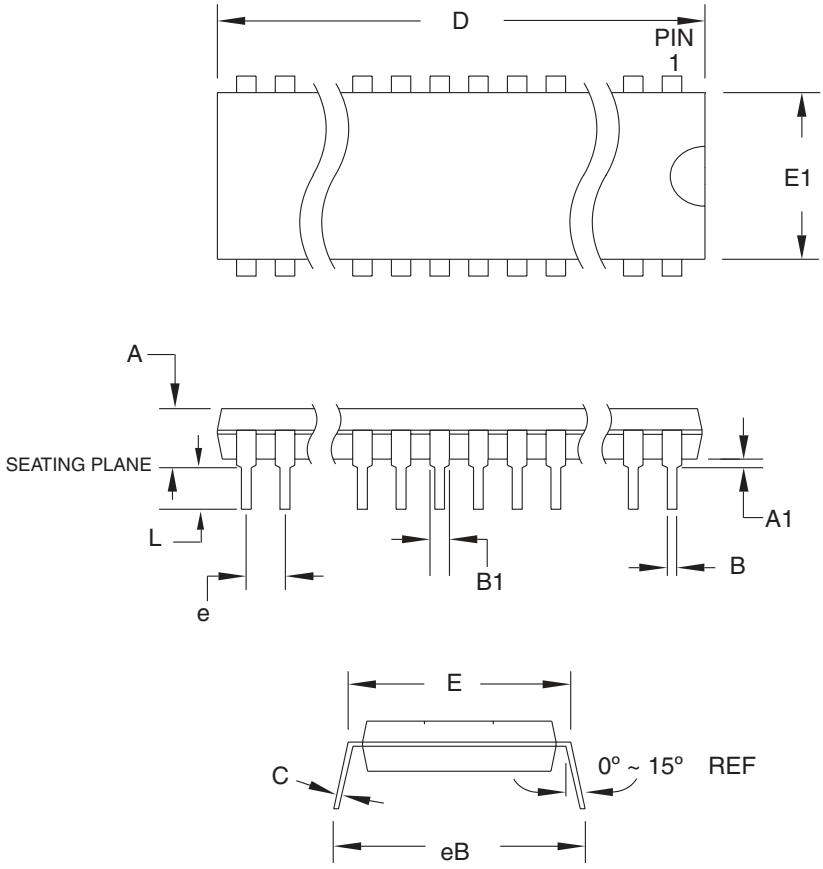
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 4.191 | – | 4.572 | |
| A1 | 2.286 | – | 3.048 | |
| A2 | 0.508 | – | – | |
| D | 17.399 | – | 17.653 | |
| D1 | 16.510 | – | 16.662 | Note 2 |
| E | 17.399 | – | 17.653 | |
| E1 | 16.510 | – | 16.662 | Note 2 |
| D2/E2 | 14.986 | – | 16.002 | |
| B | 0.660 | – | 0.813 | |
| B1 | 0.330 | – | 0.533 | |
| e | 1.270 TYP | | | |

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC) | 44J | B |

## 20.2 40P6 – PDIP




**COMMON DIMENSIONS**
(Unit of Measure = mm)

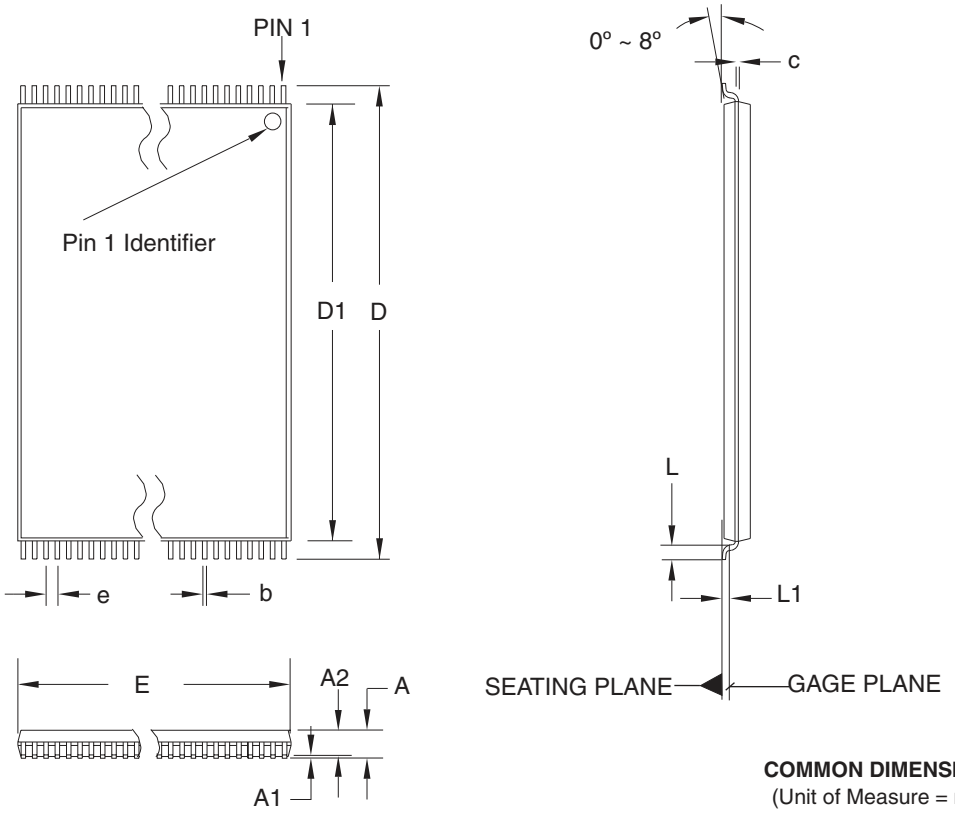
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 4.826 | |
| A1 | 0.381 | – | – | |
| D | 52.070 | – | 52.578 | Note 2 |
| E | 15.240 | – | 15.875 | |
| E1 | 13.462 | – | 13.970 | Note 2 |
| B | 0.356 | – | 0.559 | |
| B1 | 1.041 | – | 1.651 | |
| L | 3.048 | – | 3.556 | |
| C | 0.203 | – | 0.381 | |
| eB | 15.494 | – | 17.526 | |
| e | 2.540 TYP | | | |

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP) | 40P6 | B |

## 20.3 40V – VSOP




**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 13.80 | 14.00 | 14.20 | |
| D1 | 12.30 | 12.40 | 12.50 | Note 2 |
| E | 9.90 | 10.00 | 10.10 | Note 2 |
| L | 0.50 | 0.60 | 0.70 | |
| L1 | 0.25 BASIC | | | |
| b | 0.17 | 0.22 | 0.27 | |
| c | 0.10 | – | 0.21 | |
| e | 0.50 BASIC | | | |

Notes:
1. This package conforms to JEDEC reference MO-142, Variation CA.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

10/18/01

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **40V**, 40-lead (10 x 14 mm Package) Plastic Thin Small Outline Package, Type I (VSOP) | 40V | B |

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