IH6216

IH6216
8-Channel Differential CMOS Analog Multiplexer

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GENERAL DESCRIPTION

The IH6216 is a CMOS 2 of 16 multiplexer. The part is a plug-in replacement for the DG507. Three line binary decoding is used so that the 16 channels can be controlled in pairs by the binary inputs; additionally a fourth input is provided to use as a system enable. When the ENable input is high (5V) the channels are sequenced by the 3 line binary inputs, and when low (0V), all channels are off. The 3 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 3.0V. Note that the ENable input must be taken to 5V to enable the system and less than 0.8V to disable the system.

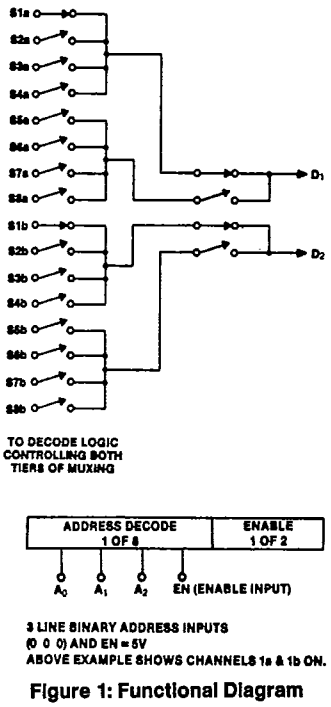
FEATURES

- Pin Compatible With HI507, DG507A & AD7507
- ±11V Analog Signal Range
- $r_{DS(on)}$ <700 Ohms Over Full Signal and Temperature Range
- Break-Before-Make Switching
- TTL and CMOS Compatible Address Control
- Binary Address Control (3 Address Inputs Control 2 Out of 16 Channels)
- Two Tier Submultiplexing to Facilitate Expandability
- Power Supply Quiescent Current Less Than 100μA
- No SCR Latchup
- Very Low Leakage $I_{D(OFF)} \leq 100pA$
- Internal Diode In Series With V^+ for Fault Protection

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH6216MJI	−55°C to +125°C	28 pin CERDIP
IH6216CJI	0°C to 70°C	28 pin CERDIP
IH6216CPI	0°C to 70°C	28 pin Plastic DIP

Ceramic package available as special order only (IH6216MDI/CDI)



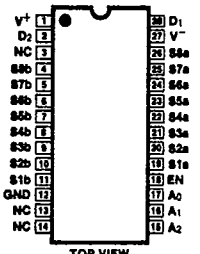
0301-1

Figure 1: Functional Diagram

DECODE TRUTH TABLE

A_2	A_1	A_0	EN	On Switch Pair
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

LOGIC "1" = V_{AH} > 3V V_{ENH} > 4.5V
LOGIC "0" = V_{AL} < 0.8V



0301-2

Figure 2: Pin Configuration

NOTE: All typical values have been characterized but are not tested.

IH6216

INTERSIL

T-51-11

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... $-15V_0-V_1$
V_S or V_D to V+ ..... 0, −36V
V_S or V_D to V− 0, 36V
V+ to Ground 16V
V− to Ground ..... −16V
Current (Any Terminal) 30mA
Current (Analog Source or Drain) 20mA
Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation (Package)* 1200mW

* All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

V+ = 15V, V− = −15V, V_{EN} = +5V (Note 1), Ground = 0V, unless otherwise specified.

Characteristic	Measured Terminal	No Tests Per Temp	Typ 25°C	Test Conditions		Max Limits M Suffix −55°C	M Suffix 25°C	M Suffix 125°C	C Suffix 0°C	C Suffix 25°C	C Suffix 70°C	Units
SWITCH												
$r_{DS(ON)}$	S to D	16	480	V_D = −10V, I_S = −1mA	Sequence each switch on	600	600	700	650	650	750	Ω
		16	300	V_D = −10V, I_S = −1mA	V_{AL} = 0.8V, V_{AH} = 3V	600	600	700	650	650	750	
$\Delta r_{DS(ON)}$			20	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$ V_S = ±10V								%
$I_{S(OFF)}$	S	16	0.01	V_S = 10V, V_D = −10V			±.5	50		±1	50	nA
		16	0.01	V_S = −10V, V_D = 10V			±.5	50		±1	50	
$I_{D(OFF)}$	D	2	0.1	V_D = 10V, V_S = −10V	V_{EN} = 0.8V		±2	100		±5	100	
		2	0.1	V_D = −10V, V_S = 10V			±2	100		±5	100	
$I_{D(ON)}$	D	16	0.1	$V_{S(ALL)}$ = V_D = 10V	Sequence each switch on		±2	100		±5	100	
		16	0.1	$V_{S(ALL)}$ = V_D = −10V	V_{AL} = 0.8V, V_{AH} = 3V		±2	100		±5	100	
INPUT												
$I_{A(on)}$ or		3	0.01	V_A = 3.0V			−10	−30		−10	−30	µA
$I_{A(off)}$		3	0.01	V_A = 14V			10	30		10	30	
I_A	A_0 A_1 A_2 A_3	3		V_{EN} = 5V	All V_A = 0		−10	−30		−10	−30	
	EN	1		V_{EN} = 0			−10	−30		−10	−30	
DYNAMIC												
t_{trans}	D		0.6	See Fig. 3			1					µs
t_{open}	D		0.2	See Fig. 4								
$t_{on(EN)}$	D		0.8	See Fig. 5			1.5					
$t_{off(EN)}$	D		0.3				1					
"OFF" Isolation	D		60	V_{EN} = 0, R_L = 200Ω, C_L = 3pF, V_S = 3VRMS, f = 500kHz								dB
C_s	S		5	V_S = 0	V_{EN} = 0, f = 140kHz to 1MHz							pF
$C_{d(off)}$	D		20	V_D = 0								
C_{ds}	D to S		1	V_S = 0, V_D = 0								
SUPPLY												
Supply +	V+	1	55				200			1000		µA
Current −	V−	1	2	V_{EN} = 5V			100			1000		
Standby +	V+	1	1		All V_A = 0 or 5V		100			1000		
Current −	V−	1	1	V_{EN} = 0			100			1000		

NOTE 1: See Enable Input Strobing Levels, Section 1.

NOTE: All typical values have been characterized but are not tested.

IH6216

IH6216

INTERSIL

T-51-11

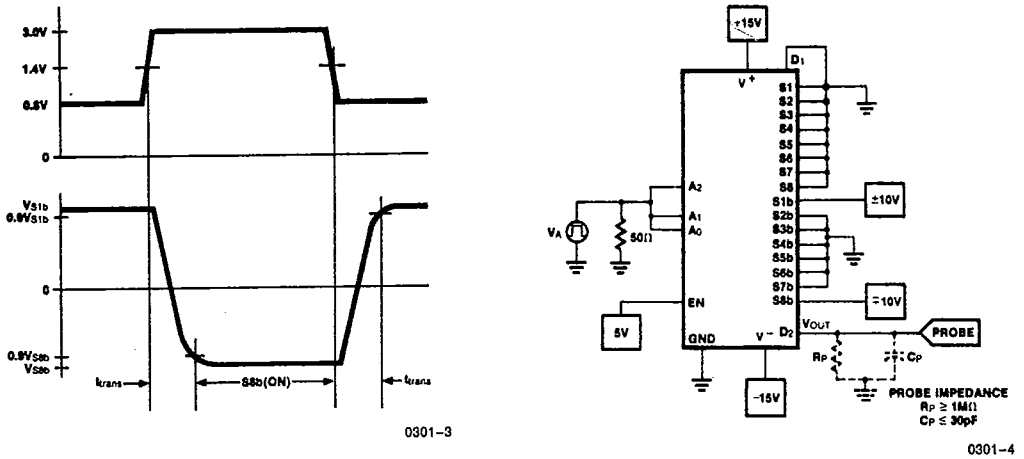


Figure 3: Switching Information

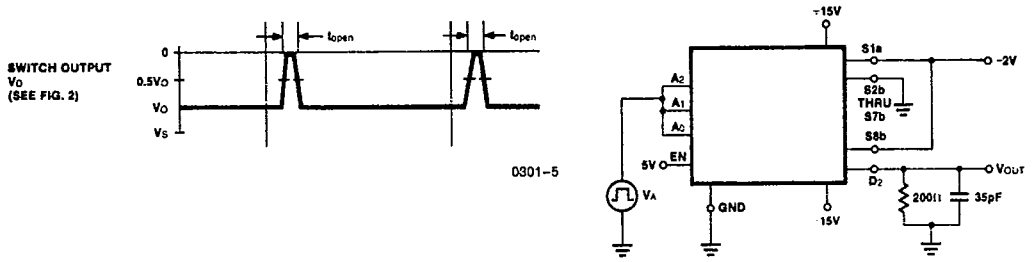


Figure 4: Switching Information

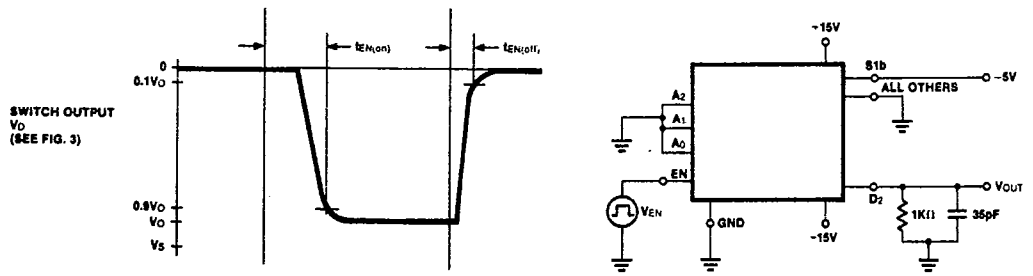


Figure 5: Switching Information

NOTE: All typical values have been characterized but are not tested.

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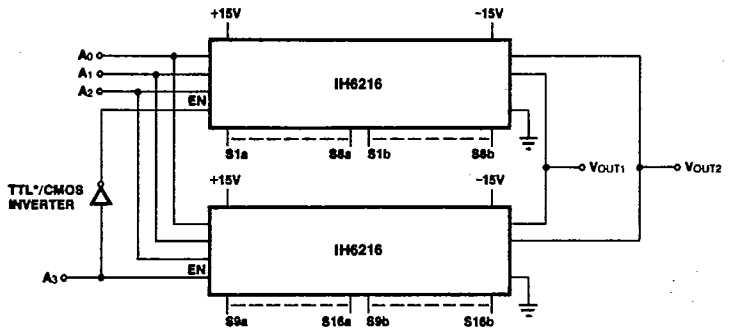
T-51-11

IH6216 APPLICATIONS



*TTL gate must have pullup to drive EN input

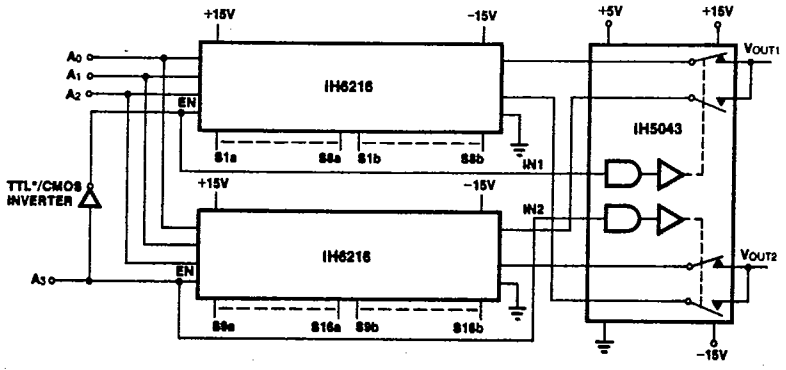
Figure 6: 2 Out of 32 Channel Multiplexer Using 2 IH6216s

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	On Switch	
0	0	0	0	S1a	
0	0	0	1	S2a	
0	0	1	0	S3a	
0	0	1	1	S4a	
0	1	0	0	S5a	
0	1	0	1	S6a	
0	1	1	0	S7a	
0	1	1	1	S8a	V_{OUT1}
1	0	0	0	S9a	
1	0	0	1	S10a	
1	0	1	0	S11a	
1	0	1	1	S12a	
1	1	0	0	S13a	
1	1	0	1	S14a	
1	1	1	0	S15a	
1	1	1	1	S16a	

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	On Switch	
0	0	0	0	S1b	
0	0	0	1	S2b	
0	0	1	0	S3b	
0	0	1	1	S4b	
0	1	0	0	S5b	
0	1	0	1	S6b	
0	1	1	0	S7b	
0	1	1	1	S8b	V_{OUT2}
1	0	0	0	S9b	
1	0	0	1	S10b	
1	0	1	0	S11b	
1	0	1	1	S12b	
1	1	0	0	S13b	
1	1	0	1	S14b	
1	1	1	0	S15b	
1	1	1	1	S16b	



*TTL inverter must have resistor pullup to drive EN input

Figure 7: 2 One of 32 Multiplexer Using Two IH6216s, and An IH5043 for Submultiplexing

NOTE: All typical values have been characterized but are not tested.

IH6216

IH6216

INTERSIL

T-51-11

General note on expandability of IH6216

The IH6216 is a two tier multiplexer, where 8 pairs of input channels are routed to a pair of outputs in blocks of 4. Each block of 4 input channels is routed to one common output channel, and thus the submultiplexed system looks like 4 blocks of 4 inputs routed to 4 different outputs with the 4 outputs tied in pairs. Thus 20 switches are needed to handle the 16 channels of information. The advantages of this are lower output capacitance and leakage than would be possible using a system with all 8 channels tied to one common output. Also the expandability into 2 out of 32, 64, 128, etc. is facilitated. Figures 6, 7, and 8 show how the IH6216 is expanded.

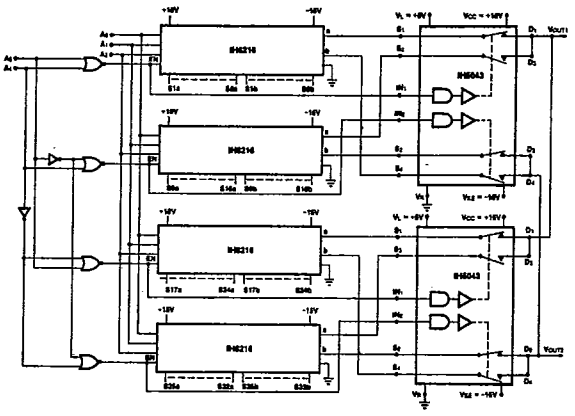
Figure 6 shows a 2 of 32 multiplexer, using 2 IH6216s. Since the 6216 is itself a 2 tier MUX, the system as shown is basically a 2 tier system. Corresponding output points of each of the 6216 are connected together, and the ENable input strobe is used as the A_3 input. Since each output (pins 2 and 28) corresponds to an "ON" FET and an "OFF" FET, the overall system looks like 1 "ON" FET and 3 "OFF" FETs for each of the V_{out1} and V_{out2} outputs. Thus the output leakage will be 1 $I_{D(on)}$ plus 3 $I_{D(off)}$s or about 0.4nA at room temperature. Throughput speed will be typically 0.8μs for t_{on} and 0.3μs for t_{off}, with throughput channel resistance in the 500Ω area.

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	On Switch	
0	0	0	0	S1a	
0	0	0	1	S2a	
0	0	1	0	S3a	
0	0	1	1	S4a	
0	1	0	0	S5a	
0	1	0	1	S6a	
0	1	1	0	S7a	
0	1	1	1	S8a	V_{OUT1}
1	0	0	0	S9a	
1	0	0	1	S10a	
1	0	1	0	S11a	
1	0	1	1	S12a	
1	1	0	0	S13a	
1	1	0	1	S14a	
1	1	1	0	S15a	
1	1	1	1	S16a	

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	On Switch	
0	0	0	0	S1b	
0	0	0	1	S2b	
0	0	1	0	S3b	
0	0	1	1	S4b	
0	1	0	0	S5b	
0	1	0	1	S6b	
0	1	1	0	S7b	
0	1	1	1	S8b	V_{OUT2}
1	0	0	0	S9b	
1	0	0	1	S10b	
1	0	1	0	S11b	
1	0	1	1	S12b	
1	1	0	0	S13b	
1	1	0	1	S14b	
1	1	1	0	S15b	
1	1	1	1	S16b	



0301-11

Figure 8: 2 One of 64 Multiplexer Using 4 IH6216s and 2 IH5043s as Submultiplexers

NOTE: All typical values have been characterized but are not tested.

IH6216

T-51-11

Figure 7 shows the 2 of 32 MUX of Figure 6, with a third tier of submultiplexing added to further reduce leakage and output capacitance. The IH5043 has typical ON resistance of 50Ω (max. is 75Ω) so it only increases throughput channel resistance from the 500 ohms of Figure 6 to about 550 ohms for Figure 7. Throughput channel speed is a little slower by about 0.5μs for both ON and OFF time, and output leakage is about 0.2nA.

Figure 8 shows a 2 of 64 MUX using 3 tier MUXing (similar to Figure 7). The Intersil IH5043 is used for the third tier of MUXing. Each V_{out} point will see 3 OFF channels and 1 ON channel at anytime, so that the typical leakages will be about 0.4nA. Throughput channel resistance will be in the 550Ω area and throughput switching speeds about 1.3μs for ON time and 0.8μs for OFF time.

The IH5043 was chosen as the third tier of the MUX because it will switch the same AC signals as the IH6216 (typically plus and minus 15V) and uses break before make switching. Also power supply quiescent currents are typically 1-2μA so that no excessive system power is generated. Note that the logic of the 5043 is such that it can be tied directly to the ENable input (as shown in the figures) with no extra logic being required.

Enable input strobing levels

The ENable input acts as an enabling or disabling pin for the IH6216 when used as a 2 out of 16 channel MUX, however when expanding the MUX to more than 16 channels, the EN pin acts as another address input. Figures 6 and 7 show the EN pin used as the A_3 input.

For the system to function properly the EN input (pin 18) must go to 5V ±5% for the high state and less than 0.8V for the low state. When using TTL logic, a pull-up of 1kΩ or less resistor should be used to pull the output voltage up to 5V. When using CMOS logic, the high state goes to the power supply so no pull-up is required.

If used on high voltage logic supplies, EN should be at least 0.7V below V^+ at all times. See IH6208 data sheet for details.

APPLICATION NOTES

Further information may be found in:

A003 "Understanding and Applying the Analog Switch"

A006 "A New CMOS Analog Gate Technology"

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing"

R009 "Reduce CMOS Multiplexer Troubles Through Proper Device Selection"

NOTE: This multiplexer does not require external resistors and/or diodes to eliminate what is commonly known as a latch up or SCR action. Because of this fact, the $r_{DS(ON)}$ of the switch is maintained at specified values.

NOTE: All typical values have been characterized but are not tested.