19-5477; Rev 0; 8/10

MAX98400A Evaluation Kit

Evaluates: MAX98400A

General Description

The MAX98400A evaluation kit (EV kit) configures the MAX98400A Class D amplifier to drive 2x20W into a pair of 8Ω speakers in stereo mode, or 1x40W into a 4Ω speaker in mono mode, for audio applications. The EV kit operates from an 8V to 28V DC power supply. The EV kit is configured for +20.1dB gain. The EV kit accepts a pair of single-ended or differential input signals and provides two sets of differential outputs for speakers.

The EV kit has two independent MAX98400A circuits, demonstrating direct speaker driving (for low component count) and filtered output driving (for ease of evaluation). The EV kit comes with two MAX98400AETX+ devices installed.

The EV kit provides an option to control the limiter, thermal foldback, input configuration, gain, shutdown, and mono mode of the MAX98400A. The EV kit also provides an input pad to accept an optional external power supply for powering the device's preamplifiers. The EV kit includes convenient audio input and output connectors.

Features

- **8V to 28V Single DC Power-Supply Operation**
- **Fully Differential Inputs and Outputs**
- **Drives 2x20W into 8Ω Speakers in Stereo Mode**
- **Drives 1x40W into 4Ω Speaker in Mono Mode**
- **Limiter Control**
- **Thermal Foldback**
- **Shutdown Control**
- **Evaluates the MAX98400A in a 36-Pin TQFN Package with an Exposed Pad**
- **U1 Configured for Filterless Output**
- **U2 Configured for Filtered Output**
- **Fully Assembled and Tested**

Ordering Information

PART	TYPE
MAX98400AEVKIT+	EV Kit

+Denotes lead(Pb)-free and RoHS compliant.

Component List

DESIGNATION	QTY	DESCRIPTION
FILTERLESS EVALUATION (U1)		
C101	1	220µF ±20%, 35V electrolytic capacitor (radial leaded, 5mm spacing), 10mm diameter x 12.5mm high Panasonic EEU-FM1V221
C102A, C102B	2	1µF ±10%, 50V X7R ceramic capacitors (0805) TDK C2012X7R1H105K
C103, C104	2	1µF ±10%, 10V X7R ceramic capacitors (0603) Murata GRM188R71A105K
C105–C108	4	1µF ±10%, 25V X7R ceramic capacitors (0805) Murata GRM21BR71E105K
C111–C114	0	Not installed, ceramic capacitors (0603)
FB1	1	22Ω at 100MHz ferrite bead (0805) Murata BLM21PG220SN1D

DESIGNATION	QTY	DESCRIPTION
GAIN1_1, GAIN2_1, LIM_1	3	3-pin headers
INL1	1	White phono jack
INR1	1	Red phono jack
JU104, JU105, $\overline{SHDN\_1}$, TEMP_1	4	2-pin headers
L1+, L1-, R1+, R1-	0	Not installed, multipurpose test points
MONO_1	0	Not installed, 2-pin header
R101, R103, R104, R105	0	Not installed, resistors (0603)
R102, R107	2	100kΩ ±5% resistors (0603)
R106	0	Not installed, potentiometer (3/8in)
R111–R114	4	0Ω ±5% resistors
SPKL1+, SPKL1-, SPKR1+, SPRK1-	4	Binding posts

Component List (continued)

DESIGNATION	QTY	DESCRIPTION
U1	1	Stereo Class D audio amplifier (36 TQFN-EP*) Maxim MAX98400AETX+
—	10	600Ω at 100MHz, 150mΩ DCR, 2A ferrite beads (0805) Würth Elektronik 742792040
—	10	330pF ±10%, 50V X7R ceramic capacitors (0603) TDK C1608X7R1H331K
FILTERED EVALUATION (U2)		
C201	1	220µF ±20%, 35V electrolytic capacitor (radial leaded, 5mm spacing), 10mm diameter x 12.5mm high Panasonic EEU-FM1V221
C202A, C202B	2	1µF ±10%, 50V X7R ceramic capacitors (0805) TDK C2012X7R1H105K
C203, C204	2	1µF ±10%, 10V X7R ceramic capacitors (0603) Murata GRM188R71A105K
C205–C208	4	1µF ±10%, 25V X7R ceramic capacitors (0805) Murata GRM21BR71E105K
C220–C223, C226–C229	8	0.15µF ±10%, 50V X7R ceramic capacitors (0805) Murata GRM21BR71H154K
C224, C225	2	0.68µF ±10%, 50V X7R ceramic capacitors (1206) Murata GRM31MR71H684K
FB2	1	22Ω ferrite bead (0805) Murata BLM21PG220SN1D
FOUTL2+, FOUTL2-, FOUTR2+, FOUTR2-	4	Binding posts

DESIGNATION	QTY	DESCRIPTION
GAIN1_2, GAIN2_2, LIM_2	3	3-pin headers
INL2	1	White phono jack
INR2	1	Red phono jack
JU204, JU205, $\overline{SHDN\_2}$, TEMP_2	4	2-pin headers
L20–L23	4	33µH ±20%, 3.0A inductors (12.3mm x 12.3mm) Sumida CDRH127NP-330NC
MONO_2	0	Not installed, 2-pin header
R201, R203, R204, R205	0	Not installed, resistors (0603)
R202, R207	2	100kΩ ±5% resistors (0603)
R206	0	Not installed, potentiometer (3/8in)
R226–R229	4	15Ω ±5% resistors (1206)
U2	1	Stereo Class D audio amplifier (36 TQFN-EP*) Maxim MAX98400AETX+
COMMON TO BOTH SIDES		
C1	1	0.1µF ±10%, 50V X7R ceramic capacitor (0603) Murata GRM188R71H104K
C2	1	1µF ±10%, 10V X7R ceramic capacitor (0603) Murata GRM188R71A105K
D1	1	4.3V, 20mA zener diode (SOT23) Central Semi CMPZ5229B
JU1	1	3-pin header
PGND, PVDD	2	Binding posts
R1	1	10kΩ ±5% resistor (0603)
—	13	Shunts
—	1	PCB: MAX98400A EVALUATION KIT+

**EP = Exposed pad.*

Component Suppliers

SUPPLIER	PHONE	WEBSITE
Central Semiconductor Corp.	631-435-1110	www.centralsemi.com
Murata Electronics North America, Inc.	770-436-1300	www.murata-northamerica.com
Panasonic Corp.	800-344-2112	www.panasonic.com
Sumida Corp.	847-545-6700	www.sumida.com
TDK Corp.	847-803-6100	www.component.tdk.com
Würth Electronik GmbH & Co. KG	201-785-8800	www.we-online.com

Note: *Indicate that you are using the MAX98400A when contacting these component suppliers.*

Quick Start

Required Equipment

- MAX98400A EV kit
- 8V to 28V, 5A DC power supply
- Audio source with volume control (e.g., CD player)
- Two speakers

Procedure—Filterless Evaluation (U1)

The EV kit is fully assembled and tested. Follow the steps below to verify board operation. **Caution: Do not turn on the power supply until all connections are completed.**

1) Verify that all jumpers are in their default positions, as shown in Table 1.
2) If not using the filtered evaluation side, remove the shunt on $\overline{\text{SHDN\_2}}$ (disable).
3) Connect the first speaker across the SPKL1- and SPKL1+ PCB binding posts.
4) Connect the second speaker across the SPKR1- and SPKR1+ PCB binding posts.
5) Connect the positive terminal of the power supply to the PVDD binding post and the power-supply ground terminal to the PGND binding post.
6) Connect the left output terminal of the audio source to the INL1 RCA phono jack.
7) Connect the right output terminal of the audio source to the INR1 RCA phono jack.
8) Turn on the audio source at minimum volume.
9) Turn on the power supply.
10) Gradually increase the audio source volume until audio is heard through the loud speakers.

Procedure—Filtered Evaluation (U2)

The EV kit is fully assembled and tested. Follow the steps below to verify board operation. **Caution: Do not turn on the power supply until all connections are completed.**

1) Verify that all jumpers are in their default positions, as shown in Table 2.
2) If not using the filterless evaluation side, remove the shunt on $\overline{\text{SHDN\_1}}$ (disable).
3) Connect the first speaker across the FOUTL2- and FOUTL2+ PCB binding posts.
4) Connect the second speaker across the FOUTR2- and FOUTR2+ PCB binding posts.
5) Connect the positive terminal of the power supply to the PVDD binding post and the power-supply ground terminal to the PGND binding post.
6) Connect the left output terminal of the audio source to the INL2 RCA phono jack.
7) Connect the right output terminal of the audio source to the INR2 RCA phono jack.
8) Turn on the audio source at minimum volume.
9) Turn on the power supply.
10) Gradually increase the audio source volume until audio is heard through the loud speakers.

_Detailed Description of Hardware

The MAX98400A EV kit provides a proven layout for evaluating the MAX98400A. The EV kit is designed to evaluate the device in a 36-pin TQFN package with an exposed pad. The device is a Class D amplifier that can be configured to drive 2x20W into a pair of 8Ω speakers, or 1x40W into a 4Ω speaker. The EV kit operates from a DC power supply that provides 8V to 28V and 5A of current. The EV kit PCB is designed with two layers and has 2oz copper for optimized power dissipation. Each side of the EV kit accepts a pair of differential or single-ended input signals and provides two sets of amplified differential audio outputs.

Optional External Preamplifier Power Supply (VS)

The EV kit provides input pads (VS1 for U1 and VS2 for U2) to accept an optional 5V external power supply for powering the device's preamplifiers when the internal regulator is disabled. The external power supply for the preamplifiers must be in the 4.5V to 5.5V range.

Filterless Output (U1)

The EV kit's filterless outputs (SPKL1+/SPKL1- and SPKR1+/SPKR1-) can be connected directly to a pair of speaker loads without any filtering.

Output Filtering Requirements (U1)

The device can pass CE EN55022B regulations with only ferrite-bead filters, especially when speaker-wire lengths are less than or equal to 1m. To install the ferrite-bead filters, first remove the 0Ω resistors (R111–R114). Next, replace resistors R111–R114 with ferrite beads listed in Table 3 (provided with the EV kit), and install filter capacitors on the C111–C114 pads. The speaker wire should be connected to the L1+/L1- and R1+/R1- test points. Although component selection for the output filter is dependent on speaker-wire length, the components in Table 3 are provided with the EV kit as a starting point. Final component selection should be determined during EMC testing. Contact the factory, if required. Note that an inductive load is required at this terminal. If using an 8Ω power resistor, add a 68µH series inductor. If using a 4Ω power resistor, add a 33µH series inductor.

Filtered Output (U2)

Audio analyzers typically cannot accept pulse-width modulated (PWM) signals at their inputs. Therefore, the EV kit features a pair of lowpass filters at each of the outputs to ease evaluation. Use the filtering output posts (FOUTL2+/FOUTL2- and FOUTR2+/FOUTR2-) to connect the filtered PWM outputs to the audio analyzer. The default lowpass filters at the EV kit outputs are optimized for a pair of 8Ω power resistors or 8Ω speakers.

Mono Mode (MONO)

The EV kit is preconfigured for stereo mode at the factory. To change the EV kit to operate in mono mode, short jumper MONO_1 (U1) or MONO_2 (U2) with a shorting wire, connect SPKL1- to SPKR1- (U1) or FOUTL2- to FOUTR2- (U2) with a short banana-lead cable, and connect SPKL1+ to SPKR1+ (U1) or FOUTL2+ to FOUTR+2 (U2) with a short banana-lead cable. Connect the audio input source to the INL1 or INL2 RCA jack.

Thermal Foldback

As shipped from the factory, the thermal-foldback feature is enabled (TEMP_1 and TEMP_2 jumpers open). To disable thermal foldback, install a shunt across the TEMP_1 and TEMP_2 jumpers. Refer to the MAX98400A/MAX98400B IC data sheet.

Limiter

As shipped from the factory, the limiter-threshold control is disabled. To enable the limiter in PVDD tracking mode, move the LIM_1 or LIM_2 shunt to the 2-3 position. To enable the limiter in programmable mode, leave the LIM_1 or LIM_2 jumper open and select appropriate values for R103, R104, and R105 or R203, R204, and R205. Refer to the MAX98400A/MAX98400B IC data sheet for information on selecting these component values.

Table 1. Jumper Descriptions (U1)

JUMPER	SHUNT POSITION	DESCRIPTION
$\overline{\text{SHDN\_1}}$	1-2*	Normal operation; U1 $\overline{\text{SHDN}}$ = DVDD (external logic-high)
	Open	Shutdown; U1 $\overline{\text{SHDN}}$ = GND
TEMP_1	Open*	Thermal foldback enabled; U1 TEMPLOCK = unconnected
	1-2	Thermal foldback disabled; U1 TEMPLOCK = GND
MONO_1	Open*	Stereo mode; U1 MONO is pulled to GND by R102
	1-2	Mono mode; U1 MONO is pulled to VS1
LIM_1	1-2*	Limiter disabled; U1 LIM_TH = VS1
	2-3	Limiter enabled in PVDD tracking mode; U1 LIM_TH = GND
	Open	Limiter programmable mode; U1 LIM_TH is determined by R103, R104, and R105
JU104	1-2*	Single-ended input mode; U1 INL- = GND
	Open	Differential input mode; U1 INL- is not connected to GND
JU105	1-2*	Single-ended input mode; U1 INR- = GND
	Open	Differential input mode; U1 INR- is not connected to GND
GAIN1_1	1-2	U1 G1 = VS1
	2-3*	U1 G1 = GND
	Open	U1 G1 is not driven
GAIN2_1	1-2	U1 G2 = VS1
	2-3	U1 G2 = GND
	Open*	U1 G2 is not driven

**Default position.*

Table 2. Jumper Descriptions (U2)

JUMPER	SHUNT POSITION	DESCRIPTION
$\overline{\text{SHDN\_2}}$	1-2*	Normal operation; U2 $\overline{\text{SHDN}}$ = DVDD (external logic-high)
	Open	Shutdown; U2 $\overline{\text{SHDN}}$ = GND
TEMP_2	Open*	Thermal foldback enabled; U2 TEMPLOCK = unconnected
	1-2	Thermal foldback disabled; U2 TEMPLOCK = GND
MONO_2	Open*	Stereo mode; U2 MONO is pulled to GND by R202
	1-2	Mono mode; U2 MONO is pulled to VS2
LIM_2	1-2*	Limiter disabled; U2 LIM_TH = VS2
	2-3	Limiter enabled in PVDD tracking; U2 LIM_TH = GND
	Open	Limiter programmable mode; U2 LIM_TH is determined by R203, R204, and R205
JU204	1-2*	Single-ended input mode; U2 INL- = GND
	Open	Differential input mode; U2 INL- is not connected to GND
JU205	1-2*	Single-ended input mode; U2 INR- = GND
	Open	Differential input mode; U2 INR- is not connected to GND
GAIN1_2	1-2	U2 G1 = VS2
	2-3*	U2 G1 = GND
	Open	U2 G1 is not driven
GAIN2_2	1-2	U2 G2 = VS2
	2-3	U2 G2 = GND
	Open*	U2 G2 is not driven

**Default position.*

Table 3. Recommended EMI Filter Components for 8Ω Loads

DESIGNATION	DESCRIPTION
R111–R114	600Ω at 100MHz, 150mΩ DCR, 2A ferrite beads (0805) Würth Elektronik 742792040
C111–C114	330pF ±10%, 50V X7R ceramic capacitors (0603) Murata GRM188R71H331K or TDK C1608X7R1H331K

Note: *3A current-rating ferrite beads are recommended for 4Ω load drive.*

Table 4. Gain Jumper Descriptions*

SHUNT POSITION		GAIN (dB)
GAIN1_1, GAIN1_2	GAIN2_1, GAIN2_2	
2-3	2-3	9.0
Open		13.0
1-2		16.7
2-3	Open	20.1
Open		23.3
1-2		26.4
2-3	1-2	29.8
Open		32.9
1-2		Reserved

**GAIN1_1 and GAIN2_1 set the gain for U1. GAIN1_2 and GAIN2_2 set the gain for U2.*

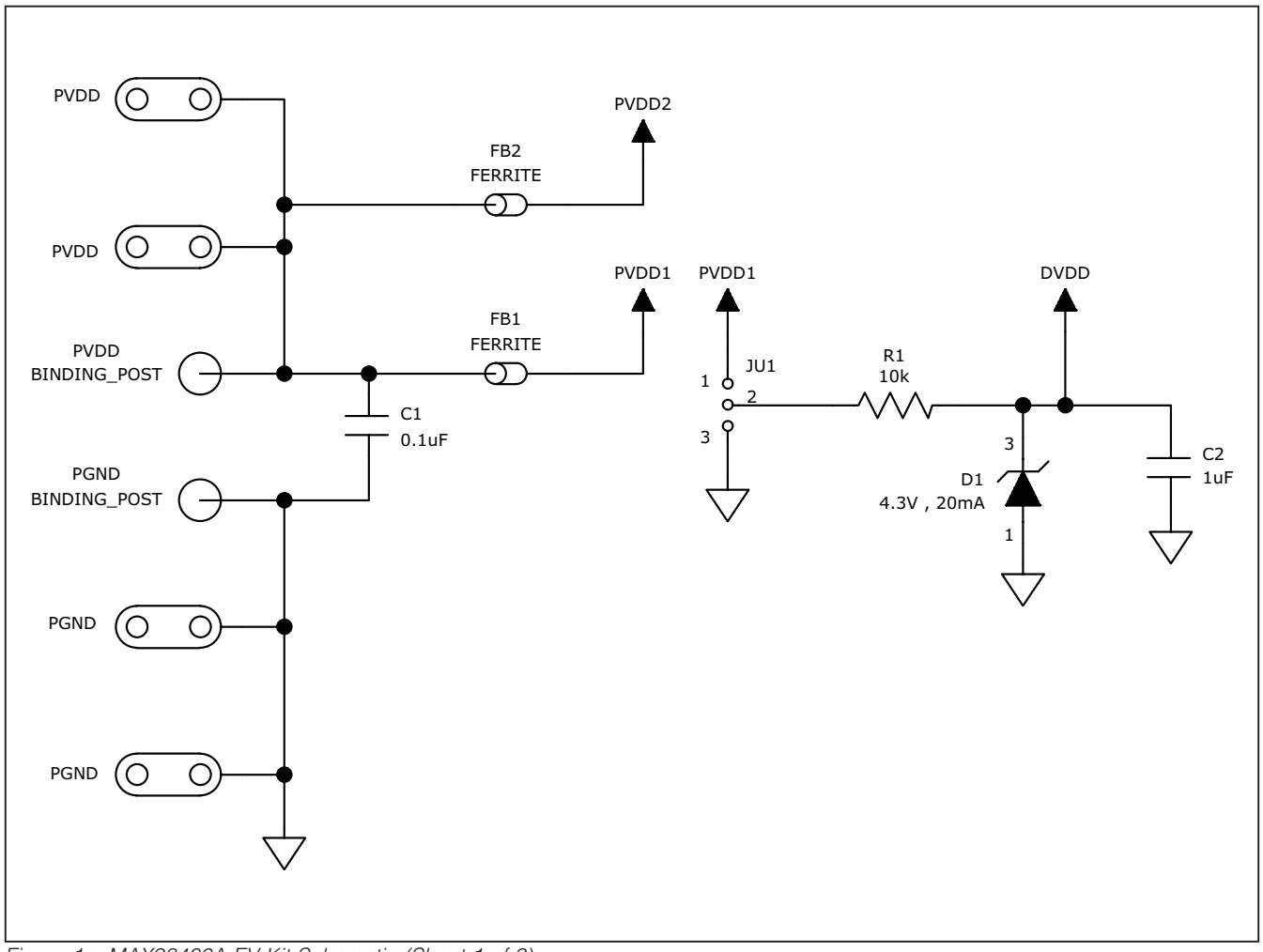


Figure 1a. MAX98400A EV Kit Schematic (Sheet 1 of 3)

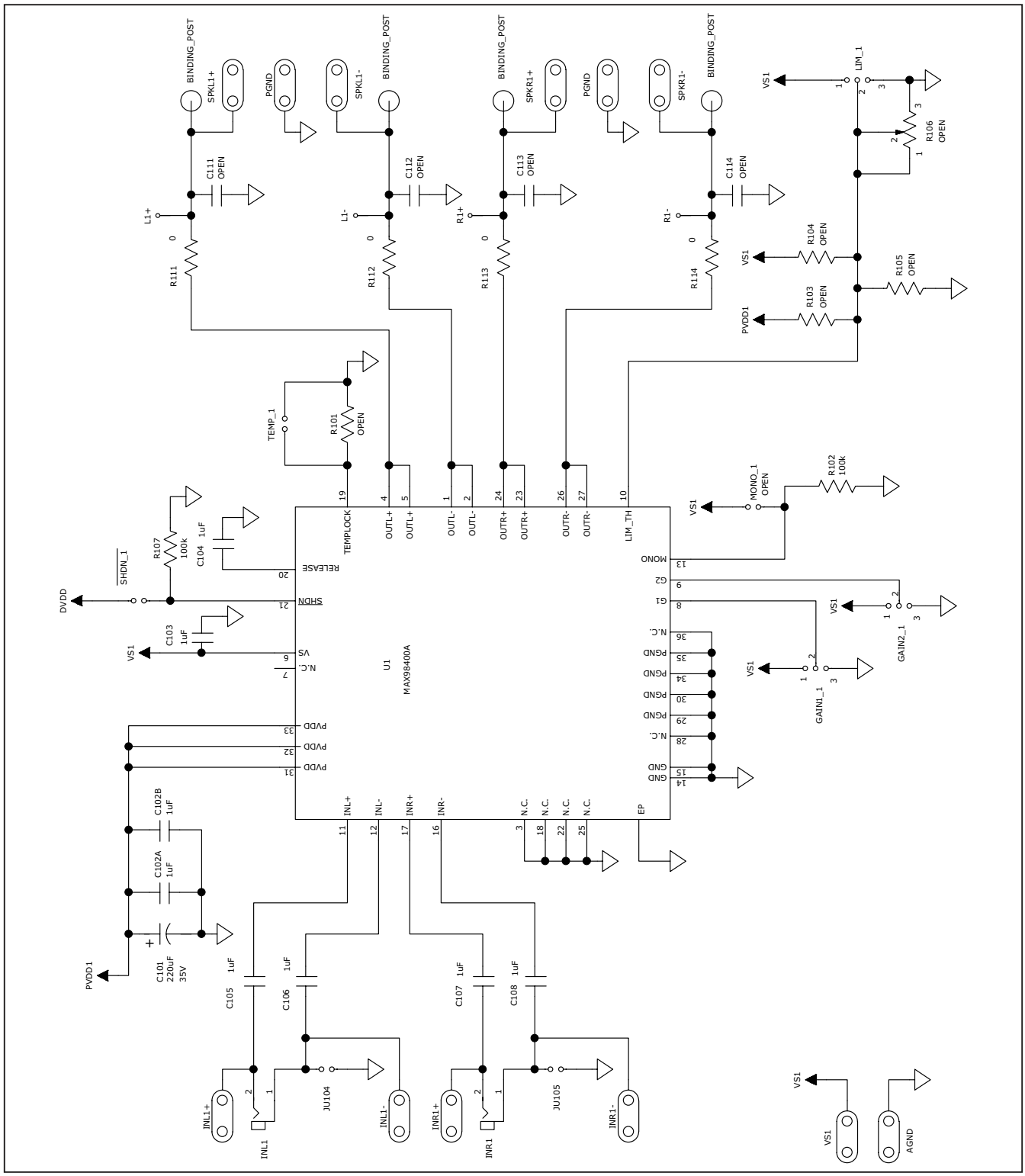


Figure 1b. MAX98400A EV Kit Schematic (Sheet 2 of 3)

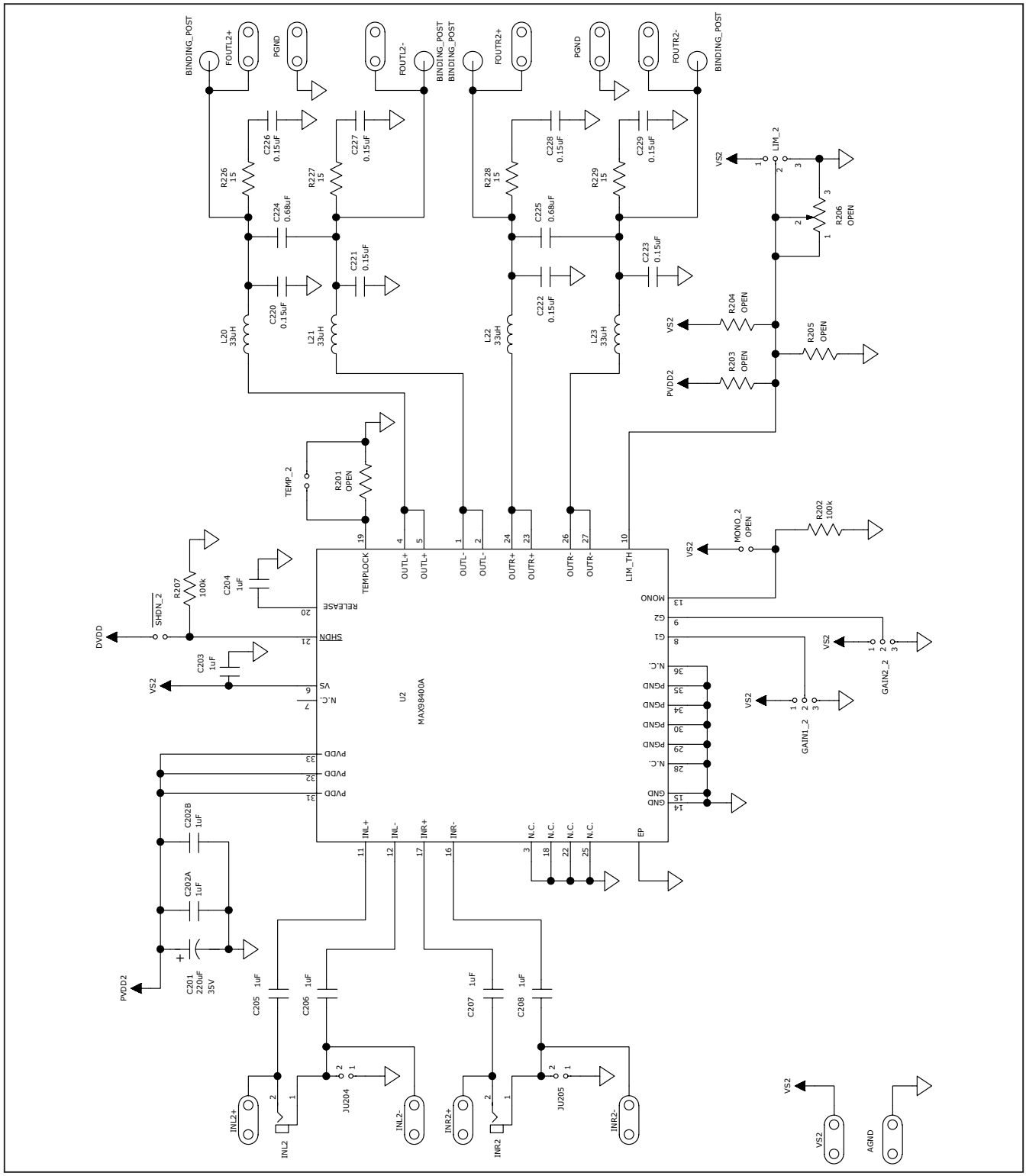
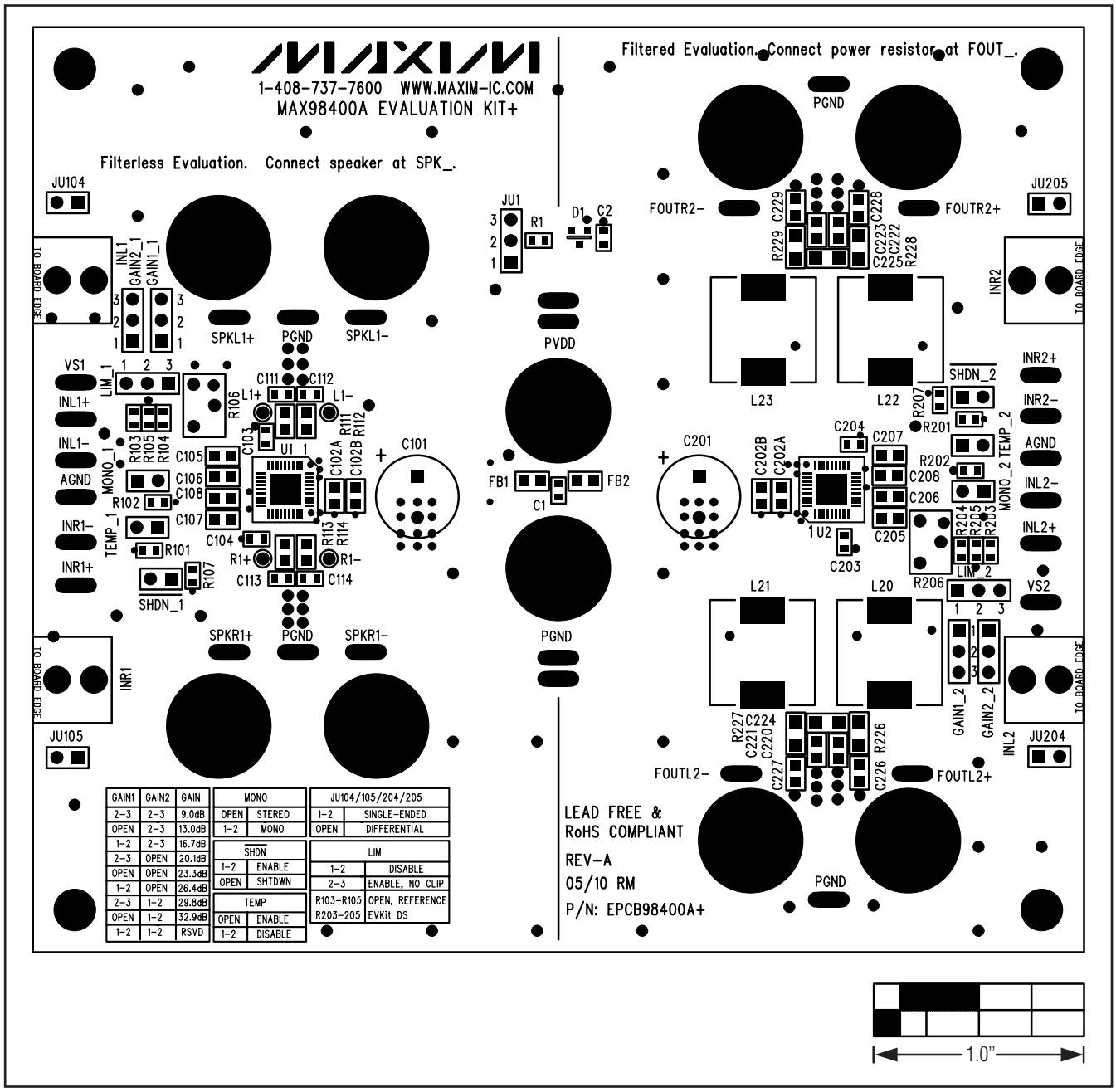


Figure 1c. MAX98400A EV Kit Schematic (Sheet 3 of 3)



GAIN1	GAIN2	GAIN
2-3	2-3	9.0dB
OPEN	2-3	13.0dB
1-2	2-3	16.7dB
2-3	OPEN	20.1dB
OPEN	OPEN	23.3dB
1-2	OPEN	26.4dB
2-3	1-2	29.8dB
OPEN	1-2	32.9dB
1-2	1-2	RSVD

MONO	
OPEN	STEREO
1-2	MONO

SHDN	
1-2	ENABLE
OPEN	SHTDWN

TEMP	
OPEN	ENABLE
1-2	DISABLE

JU104/105/204/205	
1-2	SINGLE-ENDED
OPEN	DIFFERENTIAL

LIM	
1-2	DISABLE
2-3	ENABLE, NO CLIP
R103–R105	OPEN, REFERENCE
R203–205	EVKit DS

Figure 2. MAX98400A EV Kit Component Placement Guide—Component Side

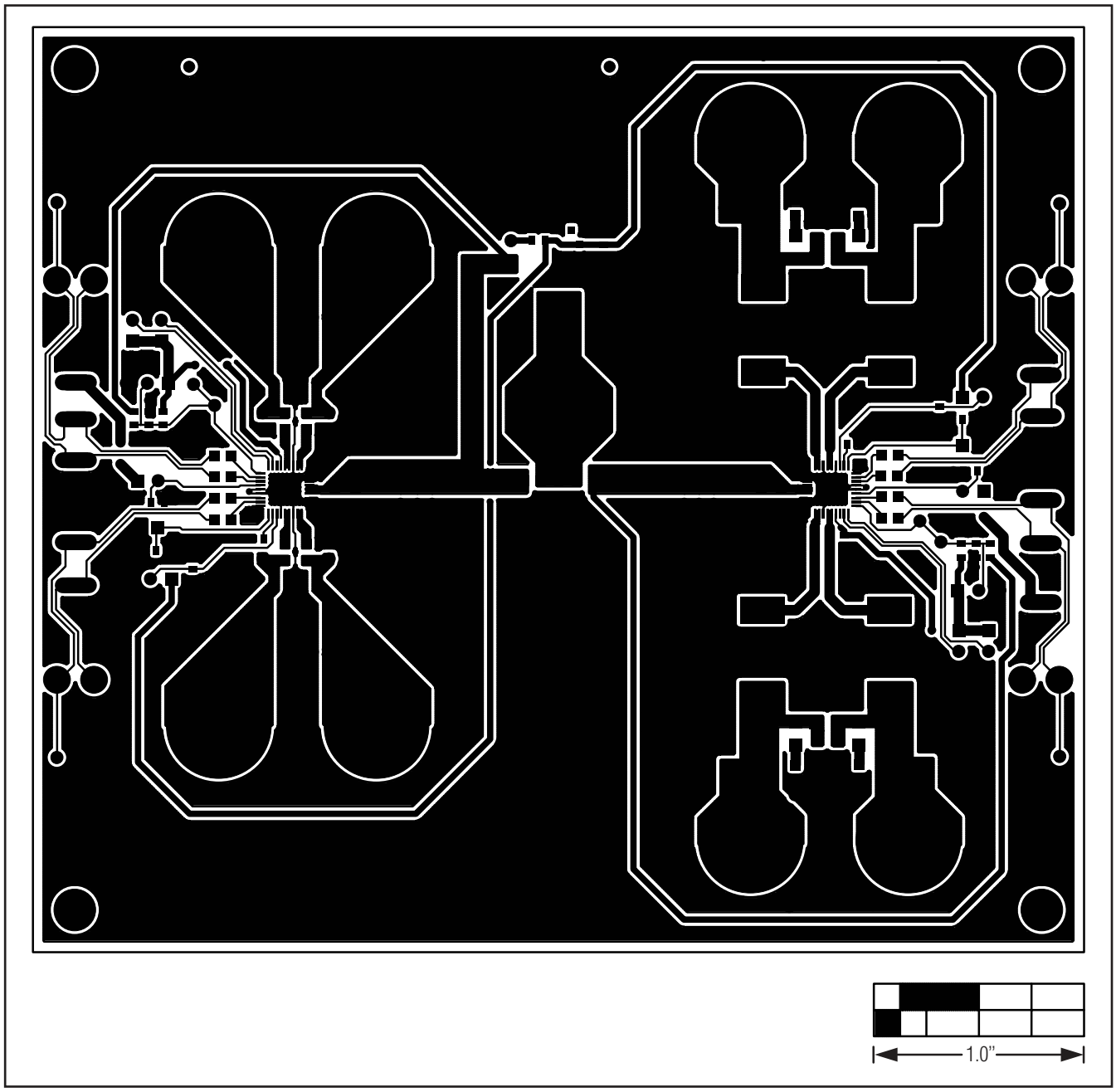


Figure 3. MAX98400A EV Kit PCB Layout—Component Side

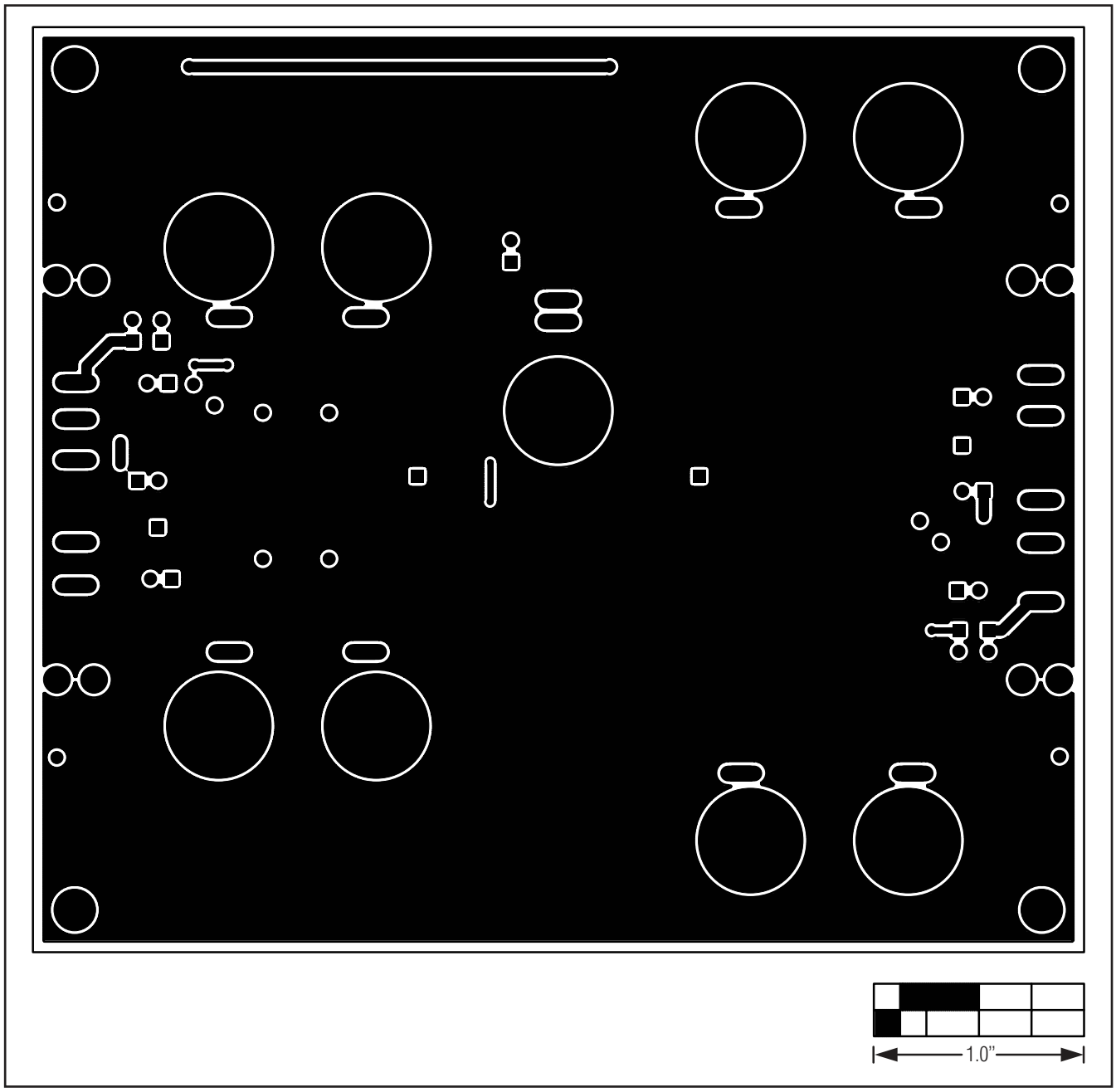


Figure 4. MAX98400A EV Kit PCB Layout—Solder Side

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/10	Initial release	—