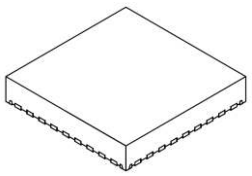
TOSHIBA Bi-CD Integrated Circuit Silicon Monolithic

TB67B001FTG, TB67B001AFTG

Sensorless PWM Driver for 3-Phase Brushless Motors

The TB67B001FTG (Later omitted TB67B001), TB67B001AFTG (Later omitted TB67B001A) is a three-phase PWM chopper driver for sensorless brushless motors. It controls motor rotation speed by changing the PWM duty cycle, based on the speed control input.
The difference of both products is the level of lock detecting signal (LD_OUT) pin. It is shown below.

TB67B001: Normal state: High, Abnormal state: Low
TB67B001A: Normal state: Low, Abnormal state: High



P-VQFN36-0505-0.50-001

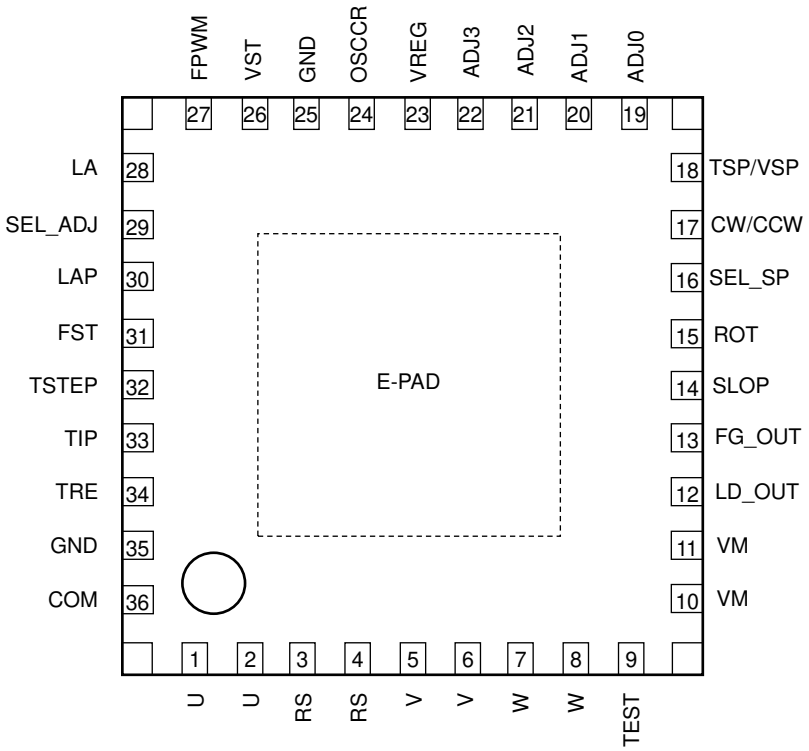
Weight: 0.05 g (typ.)

Features

- Sensorless drive in three-phase full-wave
- PWM chopper control
- Control based on the PWM duty cycle input or analog voltage input is selectable
- Output current: Absolute maximum rating: 3 A
- Power supply: Absolute maximum rating: 25 V
- Adjustable output PMW duty cycle
- Selectable lead angle control function
- Selectable overlapping commutation (120°, 135°, and 150°)
- Selectable soft switching
- Rotation speed detecting signal (FG_OUT)
- Lock detecting signal (LD_OUT)
  TB67B001: Normal state: High, Abnormal state: Low
  TB67B001A: Normal state: Low, Abnormal state: High
- Adjustable startup settings
- Selectable forced commutation frequency control function
- Selectable PWM frequency
- Restart function
- Overcurrent protection circuit (ISD)
- Thermal shutdown circuit (TSD)
- Under voltage lockout circuit (UVLO)
- Current limiter circuit

Pin Assignment

<Top View>



Note 1: Design the pattern in consideration of the heat design because a metal on the back side of a package E-PAD (3.4 mm × 3.4 mm) and the four corner PADs of a package have the role of heat radiation.
(A metal on the back side of a package (E-PAD) and the four corner PADs of a package are connected each other. And they should be connected to GND because they are connected to the back of the chip electrically.)

Note 2: Because each U, V, W, RS, and VM signal has two pins, short out these two pins at the external pattern respectively.

Pin Description

Pin No.	Symbol	I/O	Description
1	U	O	U-phase output pin
2	U	O	U-phase output pin
3	RS	—	Connection pin for output current detecting resistance
4	RS	—	Connection pin for output current detecting resistance
5	V	O	V-phase output pin
6	V	O	V-phase output pin
7	W	O	W-phase output pin
8	W	O	W-phase output pin
9	TEST	—	Test pin (Connect to ground)
10	VM	—	Motor power supply pin
11	VM	—	Motor power supply pin
12	LD_OUT	O	Lock detecting signal output pin (open-drain)
13	FG_OUT	O	Rotation speed detecting signal output pin (open-drain)
14	SLOP	I	Soft switching select input pin
15	ROT	I	Rotation speed of lead angle switching select input pin
16	SEL_SP	I	Control signal to TSP/VSP pin select input pin
17	CW/CCW	I	Forward/Reverse rotation direction select input pin
18	TSP/VSP	I	Speed command input pin (PWM duty cycle control or analog voltage control) in sensorless drive mode
19	ADJ0	I	Adjusting pin for characteristics of speed command input
20	ADJ1	I	Adjusting pin 1 for characteristics of output PWM duty cycle
21	ADJ2	I	Adjusting pin 2 for characteristics of output PWM duty cycle
22	ADJ3	I	Adjusting pin 3 for characteristics of output PWM duty cycle
23	VREG	—	Reference voltage output
24	OSCCR	—	Internal OSC setting pin
25	GND	—	Ground connection pin
26	VST	I	Output PWM duty cycle setting pin in DC excitation and forced commutation modes
27	FPWM	I	Output PWM frequency select input pin
28	LA	I	Lead angle setting input pin
29	SEL_ADJ	I	Output PWM duty cycle function setting input pin
30	LAP	I	Overlapping commutation select pin
31	FST	I	Forced commutation frequency select input pin
32	TSTEP	—	Connection pin for a capacitor to set the Output PWM duty cycle increasing time
33	TIP	—	Connection pin for a capacitor to set the DC excitation time
34	TRE	—	Connection pin for a capacitor to set the restart time
35	GND	—	Ground connection pin
36	COM	I	Connection pin for the center tap of the motor

Functional Description

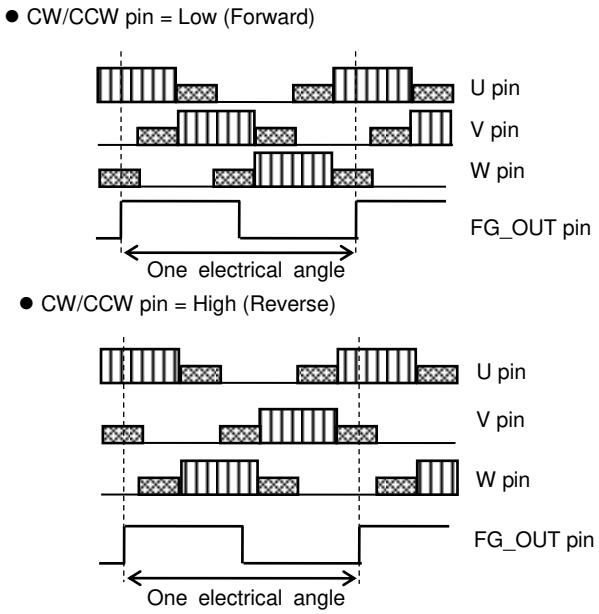
In this chapter, the equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.
Timing charts may be simplified for explanatory purposes.

1. Sensorless Drive mode

Based on a command for a startup operation, the position of the rotor is fixed in DC excitation mode.
Then, the forced commutation signal is generated to start the motor rotation. As the motor rotates, the induced voltage occurs in each phase of the coil.
When a signal indicating the polarity of each phase voltage which includes the induced voltage is detected as a position signal, the motor driving signal is automatically switched from the forced commutation signal to the normal commutation signal that is based on the position signal (induced voltage). Then, a brushless motor starts running in sensorless commutation mode.

1.1 Forward /Reverse rotation direction select input pin: CW/CCW pin

When CW/CCW pin = Low, a motor rotates in forward direction. When CW/CCW pin = High, a motor rotates in reverse direction.
Switch the rotation direction after a motor is stopped to avoid stepping out.



1.2 Rotation speed detection signal output pin: FG_OUT pin

A two-polar motor outputs a signal of 1 ppr (1 pulse/electrical angle) according to the induced voltage.
A four-polar motor outputs signals of 2 ppr similarly.

2. Startup Operation

At startup, no induced voltage is generated due to the stationary motor, and the rotor position cannot be detected for sensorless drive.
Therefore, first, this IC fixes a rotor position of motor in DC excitation mode for an appropriate period of time. And then it has a motor make starting up in forced commutation mode.
The DC excitation time is determined by the TIP pin.
The forced commutation frequency is determined by the FST pin.
The output PWM duty cycles in DC excitation and forced commutation modes are determined by the voltage of VST pin.
For sensorless drive mode, the output PWM duty cycle is determined by the speed command input to TSP/VSP pin to start and stop the motor operation, and to control the motor speed.
Since the time and startup torques (output PWM duty cycle) in DC excitation and forced commutation vary depending on the motor type and load, they should be adjusted experimentally.

2.1 DC Excitation Mode

The DC excitation time is determined by the value of capacitor (C2) connected to the TIP pin.

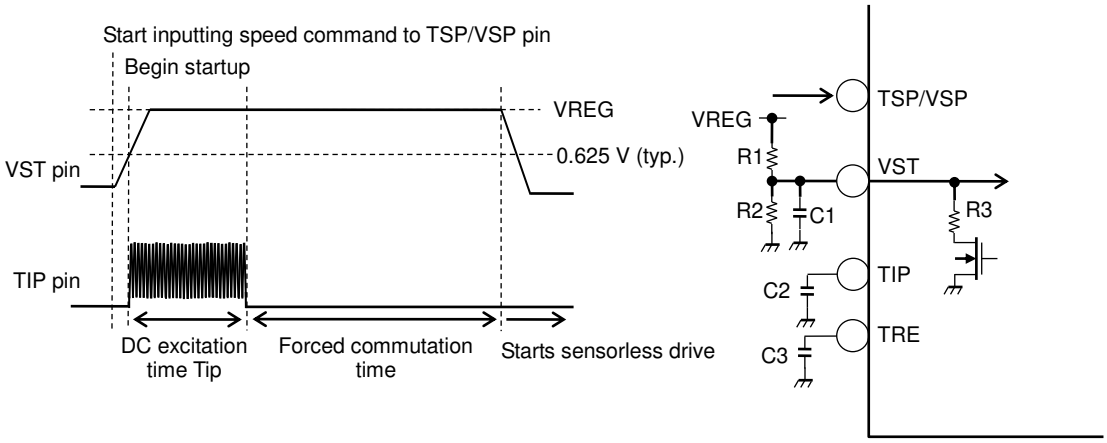
DC excitation time: Tip (s) = 0.313 × 31.5 times × C2 (F) × 10^6

When C2 = 0.01 µF, Tip = 0.0986 s

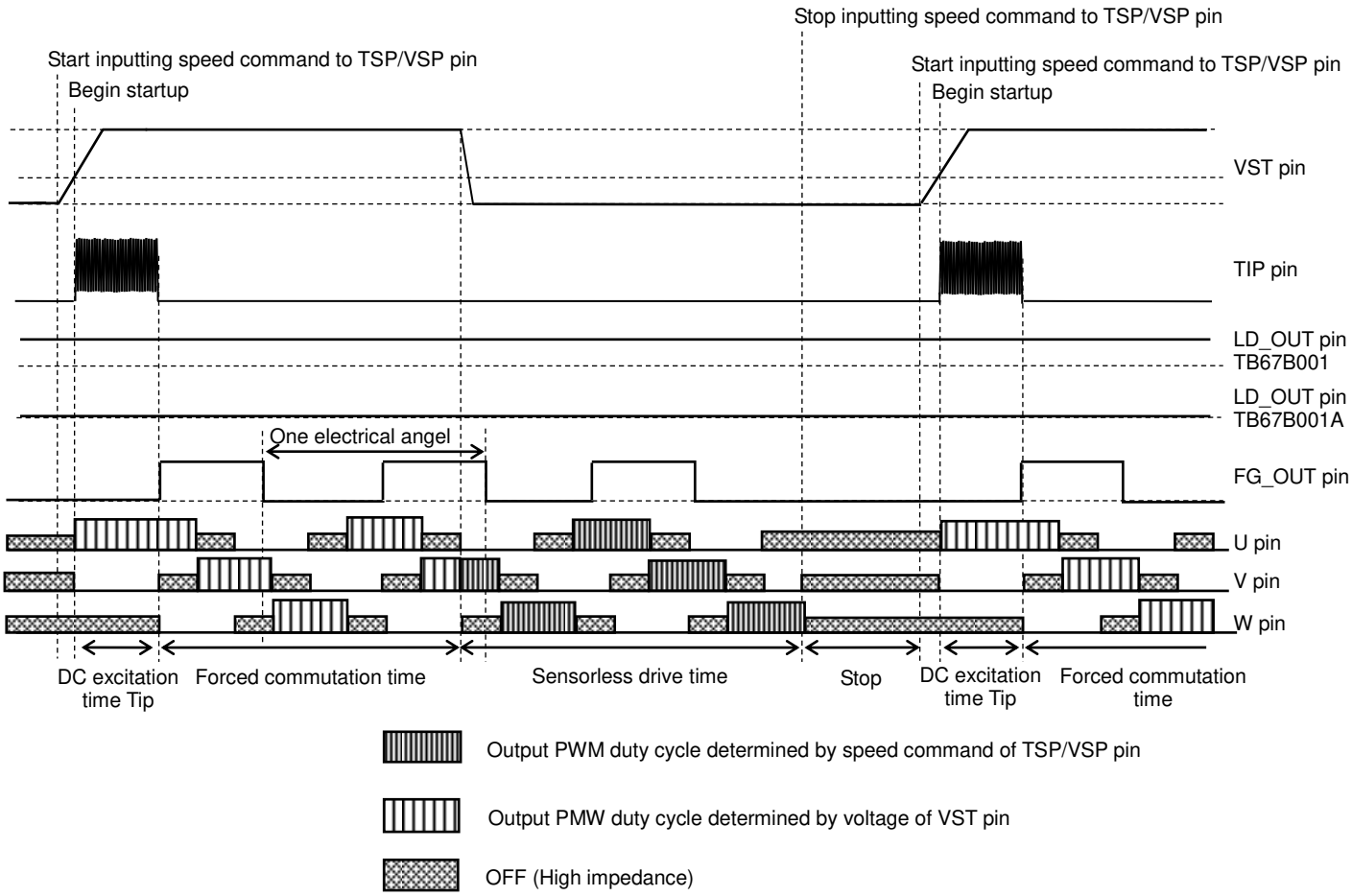
2.2 Forced Commutation Mode

The forced commutation frequency is determined by the voltage of the FST pin.

FST = High: Forced commutation frequency f_{ST} ≈ 6.4 Hz
FST = Middle or Open: Forced commutation frequency f_{ST} ≈ 3.2 Hz
FST = Low: Forced commutation frequency f_{ST} ≈ 1.6 Hz



2.3 Timing Chart of the Startup Operation



3. Operation in Abnormality Detection

When the following events are detected, the operation in abnormality detection is done.

1. The forced commutation frequency exceeds four electrical-degree period.
2. The overcurrent protection circuit (ISD) is activated.
3. The thermal shutdown circuit (TSD) is activated.
4. The rotation frequency in sensorless drive mode is the forced commutation frequency or less.
5. The rotation frequency (commutation frequency) is the maximum rotation frequency (FMAX) or more.

   FMAX depend on the state of FST pin is shown below.

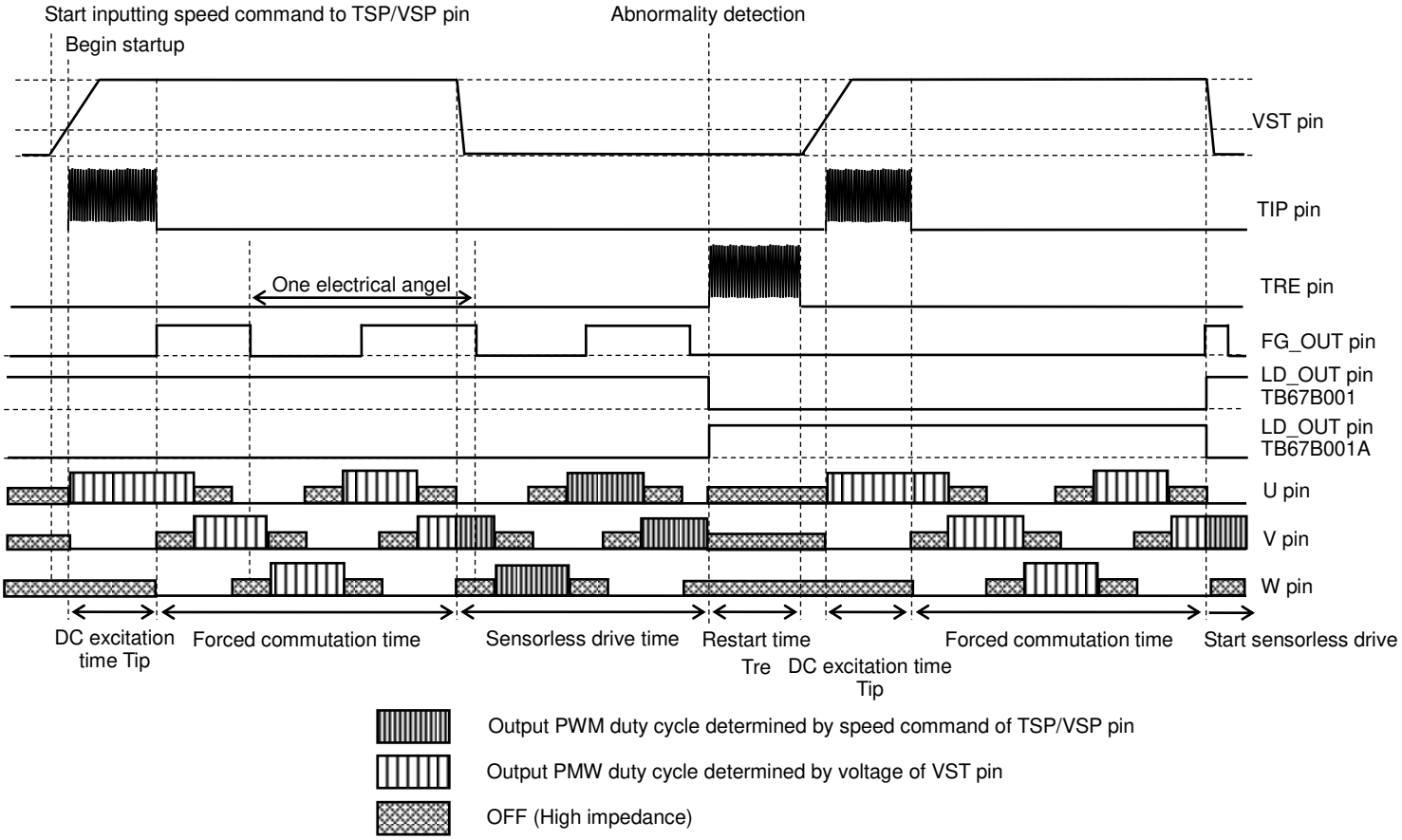
   FST pin = High: FMAX = 1.5 kHz / 1 electrical angle frequency
   FST pin = Middle or open: FMAX = 1.5 kHz / 1 electrical angle frequency
   FST pin = Low: FMAX = 750 Hz / 1 electrical angle frequency

When any abnormality is detected, output pins are turned off (high impedance) during the operation restart time (Tre).
The restart time is determined by the value of a capacitor (C3) connected to TRE pin.

Restart time: Tre (s) = 0.313 × 31.5 times × C3 (F) × 10^6

When C3 = 1 µF, Tre = 9.86 s.

3.1 Timing Chart of Abnormality Detection



3.2 Operation in Lock Detection

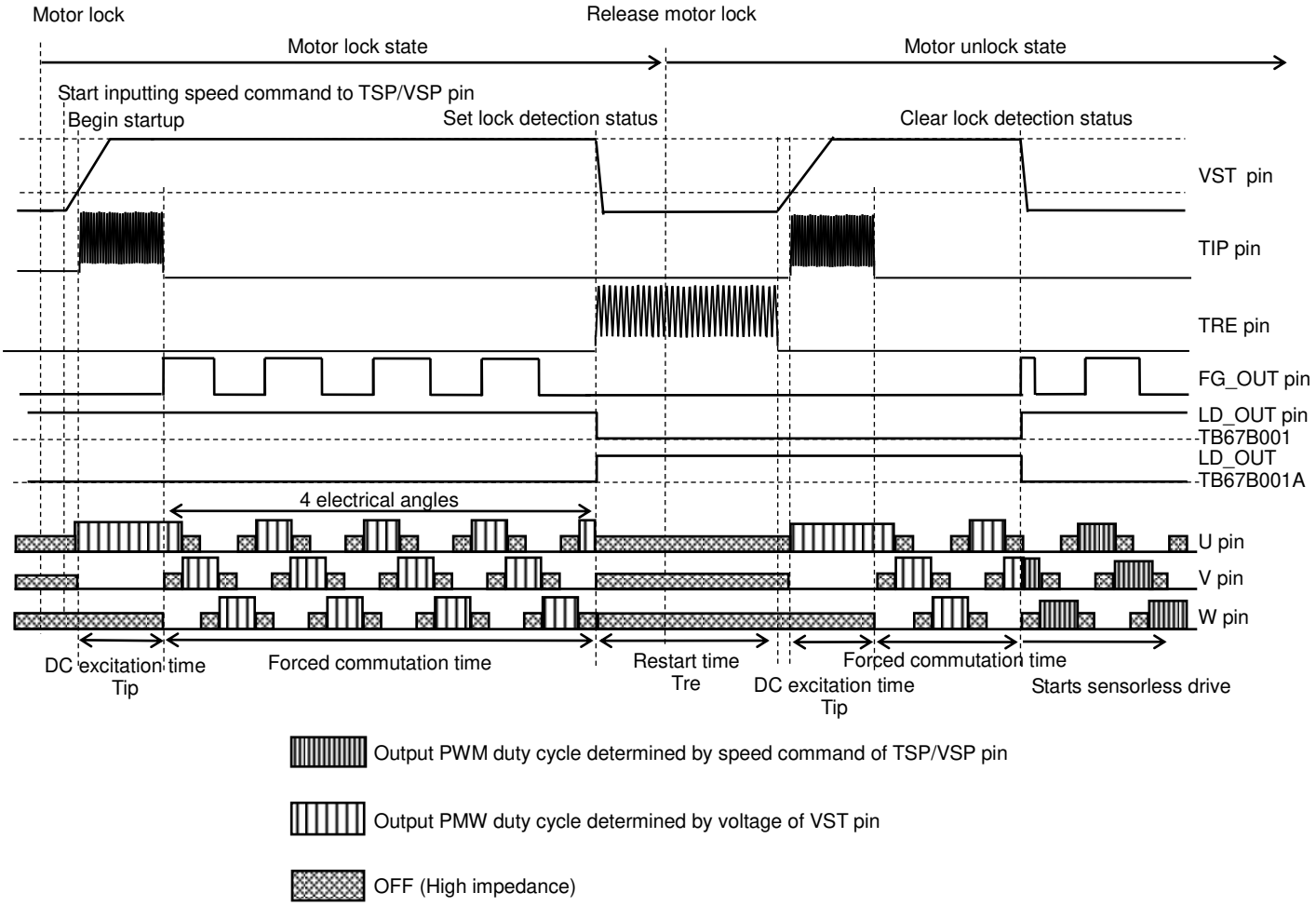
When the operation mode does not change from the forced commutation mode to the senseless drive mode by the motor rotation lock and so on, the LD_OUT pin outputs low (In case of TB67B001, the LD_OUT pin outputs high in case of TB67B001A.) from starting the restart.

Then, the following operations are repeated and the LD_OUT pin keeps low (In case of TB67B001, the LD_OUT pin outputs high in case of TB67B001A) until the sensorless drive mode starts normally.

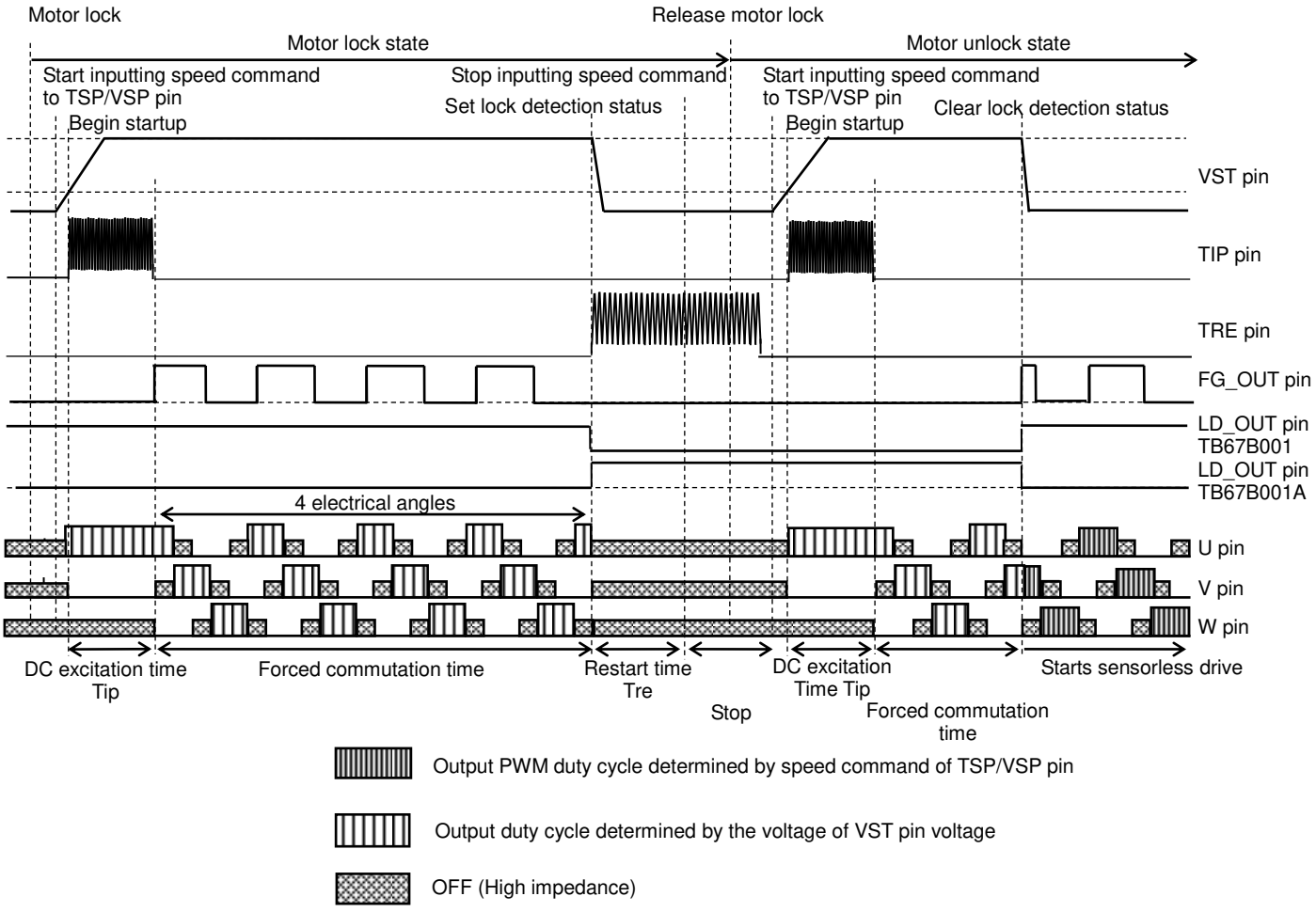
Restart time → DC excitation time → forced commutation time (during 4-electrical angles) → Restart time → DC excitation time…

When the inputting speed command to TSP/VSP pin is stopped in the lock detection, the LD_OUT pin keeps low (In case of TB67B001, the LD_OUT pin keeps high in case of TB67B001A) until the sensorless drive mode starts.

3.3 Timing Chart of Lock Detection



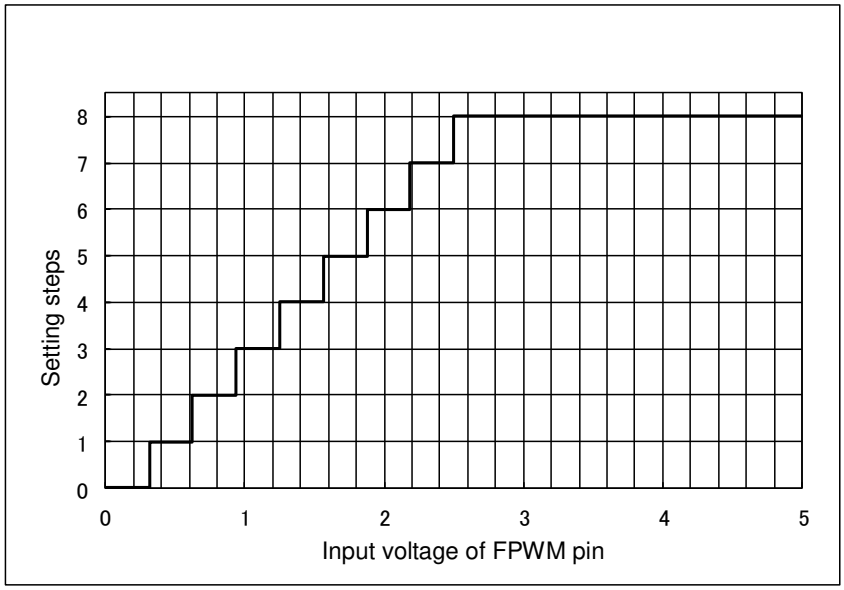
3.4 Timing Chart of Stopping Speed Command of TSP/VSP pin during Lock Detection

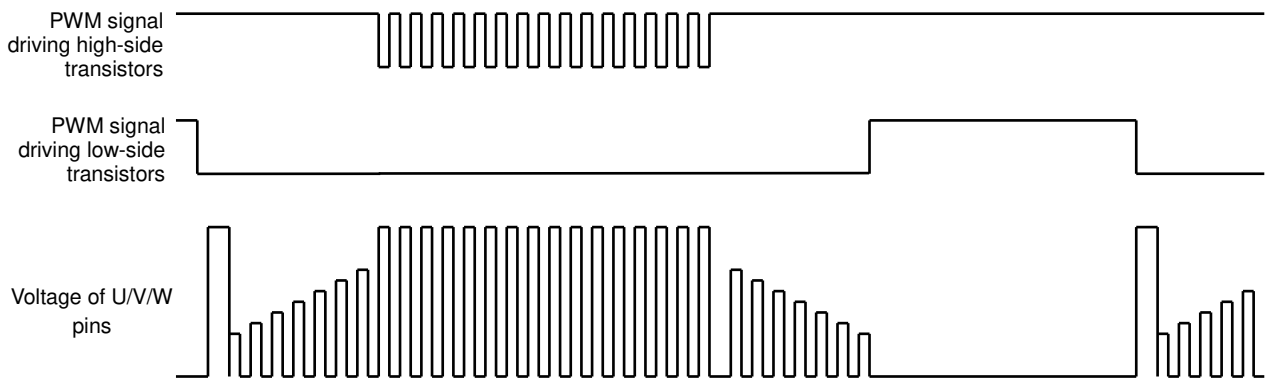


4. PWM frequency

Output PWM frequency determined by the input voltage of FPWM pin.
Depending on the set value, the PWM frequency changes according to the rotation speed.
The PWM frequency must be sufficiently high relative to the electrical frequency of the motor and within the range permitted by the switching characteristics of the driver circuit.

Setting steps	FPWM pin voltage (V)	Rotation speed (Electrical angle)					
		0 Hz to less than 200 Hz	200 Hz to less than 400 Hz	400 Hz to less than 600 Hz	600 Hz to less than 800 Hz	800 Hz to less than 1 kHz	1 kHz to 1.5 kHz
8	2.5	23.8 kHz	47.7 kHz	95.3 kHz	95.3 kHz	190.6 kHz	190.6 kHz
7	2.1875	23.8 kHz	23.8 kHz	47.7 kHz	47.7 kHz	95.3 kHz	95.3 kHz
6	1.875	23.8 kHz	47.7 kHz	95.3 kHz	95.3 kHz	95.3 kHz	95.3 kHz
5	1.5625	47.7 kHz	47.7 kHz	95.3 kHz	95.3 kHz	95.3 kHz	190.6 kHz
4	1.25	47.7 kHz	95.3 kHz	95.3 kHz	95.3 kHz	95.3 kHz	190.6 kHz
3	0.9375	190.6 kHz					
2	0.625	95.3 kHz					
1	0.3125	47.7 kHz					
0	0	23.8 kHz					





5. Motor Speed Control

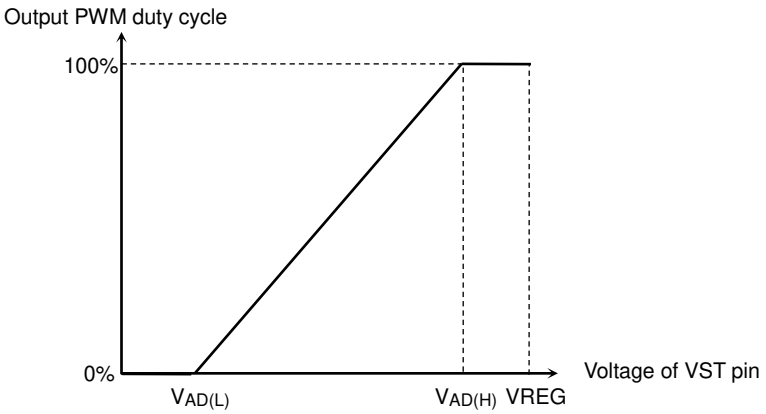
Control signal to TSP/VSP pin can make on/off the motor and control the output PWM duty cycle to control the rotation speed of the motor.
It can also select the analog voltage control or the PWM duty cycle control by the level of SEL_SP pin.
As other functions, the control signal to TSP/VSP pin can adjust the variation of the output PWM duty cycle by the voltage level of ADJ0 pin, ADJ1 pin, ADJ2 pin, and ADJ3 pin.

Level of SEL_SP pin	Control signal to TSP/VSP pin
High	An analog voltage
Low	A PWM duty cycle

5.1 Relation between the Voltage of a VST Pin and Output PWM Duty Cycle in DC Excitation and the Forced Commutation Modes.

Output PWM duty cycle in the DC excitation and the forced commutation modes are determined by the voltage of VST pin.

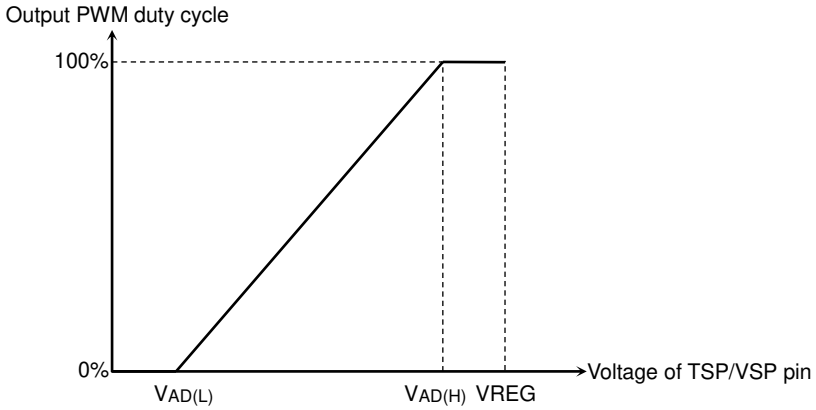
0 ≤ Voltage of VST pin ≤ $V_{AD(L)}$: 0.625 V (typ.)
→ Output PWM duty cycle = 0%
$V_{AD(L)}$ ≤ Voltage of VST pin ≤ $V_{AD(H)}$: 3.125 V (typ.)
→ Output PWM duty cycle = 0% to 100% (0/128 to 128/128)
$V_{AD(H)}$ ≤ Voltage of VST pin ≤ VREG
→ Output PWM duty cycle = 100% (128/128)



5.2 Relation between a Voltage of TSP/VSP Pin and Output PWM Duty Cycle in Sensorless Drive Mode (SEL_SP pin = High)

This section describes in case of the control signal is an analog voltage.
The startup operation begins when a voltage of TSP/VSP pin is 0.625 V (typ.) or above. And the startup operation is reset when it is less than 0.625 V.

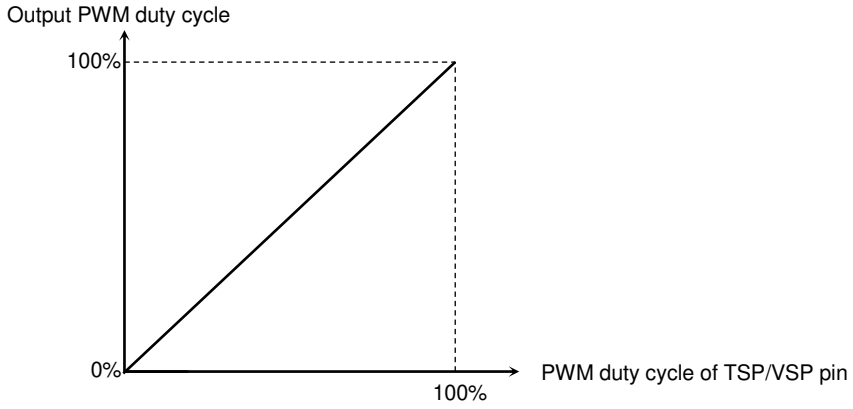
0 ≤ Voltage of TSP/VSP pin ≤ $V_{AD(L)}$: 0.625 V (typ.)
→ Output PWM duty cycle = 0% (0/128)
$V_{AD(L)}$ ≤ Voltage of TSP/VSP pin ≤ $V_{AD(H)}$: 3.125 V (typ.)
→ Output PWM duty cycle = 0% to 100% (0/128 to 128/128)
$V_{AD(H)}$ ≤ Voltage of TSP/VSP pin ≤ VREG
→ Output PWM duty cycle = 100% (128/128)



Note: The relation when ADJ1 pin, ADJ2 pin, and ADJ3 pin are connect to ground is shown above. For details of ADJ1 pin, ADJ2 pin and ADJ3 pin, refer to 5.4.

5.3 Relation between PWM Duty Cycle of TSP/VSP Pin and Output PWM Duty Cycle in Sensorless Drive Mode (SEL_SP pin = Low)

This section describes in case of the control signal is the PWM duty cycle.
The startup operation begins when the PWM signal is inputted to TSP/VSP pin.
The ON time of the PWM signal may be not detected when it is 0.2 µs or less. Also, the PWM signal is decided as no signal when the OFF time of the PWM signal is 2.5 ms or above.
The frequency of the PWM signal to TSP/VSP pin should be in the range from 400 Hz to 100 kHz.
In changing Duty, it should be changed within 510 ms because Duty is kept for 510 ms. When it exceeds 510 ms, the operation is judged stop. When signal of stop is inputted, the operation stops after 510 ms passes because Duty is kept for 510 ms.



Note: The relation when ADJ1 pin, ADJ2 pin, and ADJ3 pin are connect to ground is shown above. For details of ADJ1 pin, ADJ2 pin and ADJ3 pin, refer to 5.4.

5.4 Adjustment of the Relation between the Control Signal to TSP/VSP Pin and Output PWM Duty Cycle

Three points of output PWM duty cycles can be adjusted by the voltages of ADJ1 pin, ADJ2 pin and ADJ3 pin.

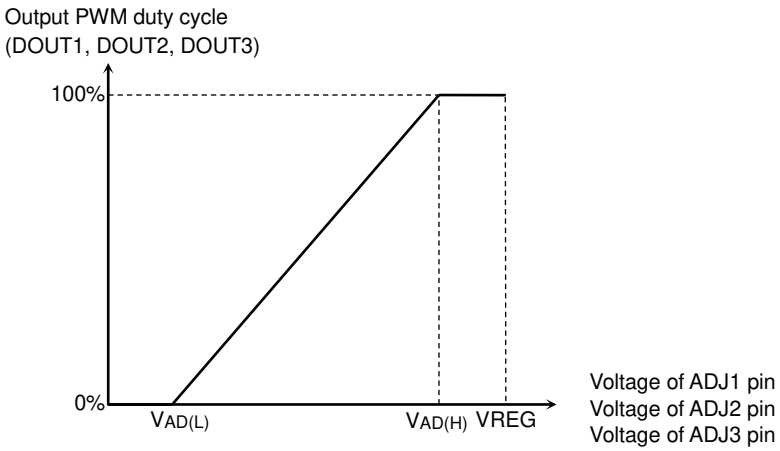
Voltage input pin for adjustment	Adjusted output PWM duty cycle
ADJ1 pin	DOUT1
ADJ2 pin	DOUT2
ADJ3 pin	DOUT3

The DOUT2 is the output PWM duty when the percent value of the control signal of TSP/VSP pin is 50% (typ.).
And also, the DOUT3 is the output PWM duty when the percent value of the control signal of TSP/VSP pin is 90% (typ.).
The DOUT1's percent of the control signal can be adjusted by the voltage of ADJ0

Percent value of the control signal of TSP/VSP pin	Output PWM duty cycle
Value specified by the voltage of ADJ0 pin (DIN1)	DOUT1
50% (typ.) (DIN2)	DOUT2
90% (typ.) (DIN3)	DOUT3

1) Relation between the voltages of ADJ1, ADJ2 and ADJ3 pins and the output PWM duty cycles (DOUT1, DOUT2, DOUT3)

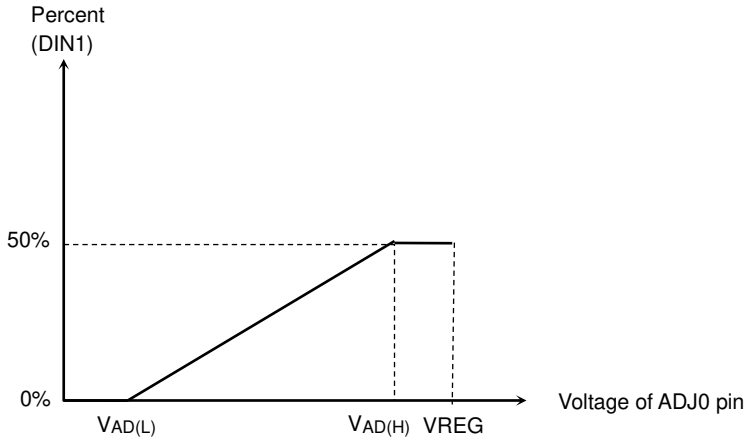
0 ≤ Voltages of ADJ1, ADJ2 and ADJ3 pins ≤ $V_{AD(L)}$: 0.625 V (typ.)
→ The output PWM duty cycle (DOUT1, DOUT2, DOUT3) = 0% (0/128)
$V_{AD(L)}$ ≤ Voltages of ADJ1, ADJ2 and ADJ3 pins ≤ $V_{AD(H)}$: 3.125 V (typ.)
→ The output PWM duty cycle (DOUT1, DOUT2, DOUT3) = 0% to 100% (0/128 to 128/128)
$V_{AD(H)}$ ≤ Voltages of ADJ1, ADJ2 and ADJ3 pins ≤ VREG
→ The output PWM duty cycle (DOUT1, DOUT2, DOUT3) = 100% (128/128)



Note: Voltage setting of ADJ1 pin, ADJ2 pin and ADJ3 pin should be set as follows; voltage of ADJ1 pin ≤ voltage of ADJ2 pin ≤ voltage of ADJ3 pin. If it is set as follows; voltage of ADJ1 pin > voltage of ADJ2 pin > voltage of ADJ3 pin, this function may not operate correctly.

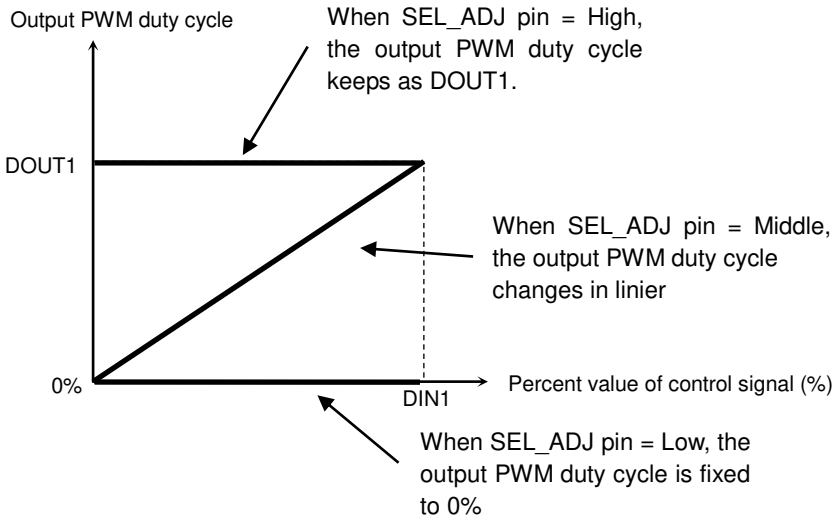
2) Relation between a voltage of ADJ0 pin and the DIN1 which makes the output PWM duty cycle as the DOUT1 is shown bellows ;

0 ≤ Voltages of ADJ0 pin ≤ $V_{AD(L)}$: 0.625 V (typ.)
→ The percent of the control signal (DIN1) = 0% (0/128)
$V_{AD(L)}$ ≤ Voltages of ADJ0 pin ≤ $V_{AD(H)}$: 3.125 V (typ.)
→ The percent of the control signal (DIN1) = 0% to 50% (0/128 to 128/128)
$V_{AD(H)}$ ≤ Voltages of ADJ0 pin ≤ VREG
→ The percent of the control signal (DIN1) = 50% (128/128)



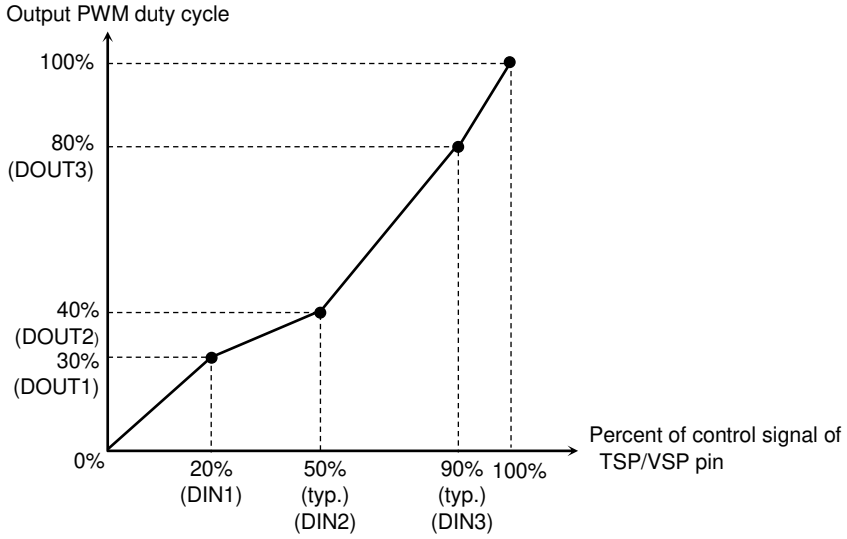
3) When the percent value of the control signal is equal or less than the duty cycle (DIN1) specified by a voltage of ADJ0 pin, the relation between the percent value of the control signal and output PWM duty cycle according to the state of SEL_ADJ pin is shown in the below table.

SEL_ADJ	Operation state
High	When the percent value of the control signal is DIN1 or less, the output PWM duty cycle is kept as DOUT1.
Middle	When the percent value of the control signal is DIN1 or less, the output PWM duty cycle changes in linier from the output PWM duty cycle of DIN1 to 0%.
Low	When the percent value of the control signal is DIN1 or less, the output PWM duty cycle is fixed to 0%.



4) Setting example

Percent of control signal of TSP/VSP pin	Output PWM duty cycle
Up to 20%	From 0% to 30% in linier
20% (DIN1)	30% (DOUT1)
50% (typ.) (DIN2)	40% (DOUT2)
90% (typ.) (DIN3)	80% (DOUT3)



To set the above relation between the percent of control signal of TSP/VSP pin and the output PWM duty cycle, set the level of SEL_ADJ pin and the voltage of ADJ0 pin, ADJ1 pin, ADJ2 pin and ADJ3 pin shown below.

- SEL_ADJ pin = MIDDLE
- Voltage of ADJ0 pin: (20% / 50% × (3.125-0.65V))+ 0.625V = 1.625V
- Voltage of ADJ1 pin: (30% / 100% × (3.125-0.65V)) + 0.625V = 1.375V
- Voltage of ADJ2 pin: (40% / 100% × (3.125-0.65V)) + 0.625V = 1.625V
- Voltage of ADJ3 pin: (80% / 100% × (3.125-0.65V)) + 0.625V = 2.625V

6. Commutation Control

In forced commutation mode at startup, this IC is configured for 120° commutation with a lead angle of 0°, and without soft switching.
Then, when the operation mode enters sensorless driving mode, its commutation waveform automatically changes to the one specified by the LA, the LAP, and the SLOP pins.
When SLOP pin is Low, the soft switching function operates. The output PWM duty cycle in output commutation switching changes in stages.
The soft switching pattern is three depend on the state of LAP pin. And the soft switching pattern of 150° commutation has the Pattern A and Pattern B. They have difference of the output duty cycle changes in stages.
When SLOP pin is High, the soft switching function does not operate.

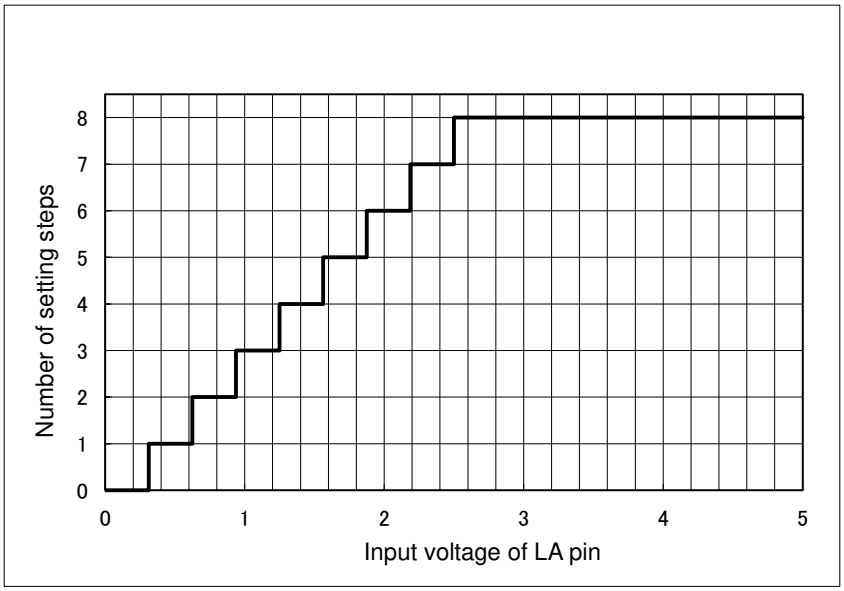
SLOP pin	LAP pin	Soft switching	Commutation angle
High	High	N/A	120° commutation
	Middle	N/A	135° commutation
	Low	N/A	150° commutation
Low	High	Available (With pattern B)	150° commutation
	Middle	Available	135° commutation
	Low	Available (With pattern A)	150° commutation

6.1 Setting lead angle

When ROT pin is High, the lead angle is determined by the voltage of LA pin regardless of the rotation speed.
When ROT pin is Low, the lead angle changes depending on the rotation speed.
At this time, in case of FST pin is Low, the lead angle changes whenever the rotation speed increases 100 Hz.
In case of FST pin is Middle or High, the lead angle changes whenever it increases 200 Hz.

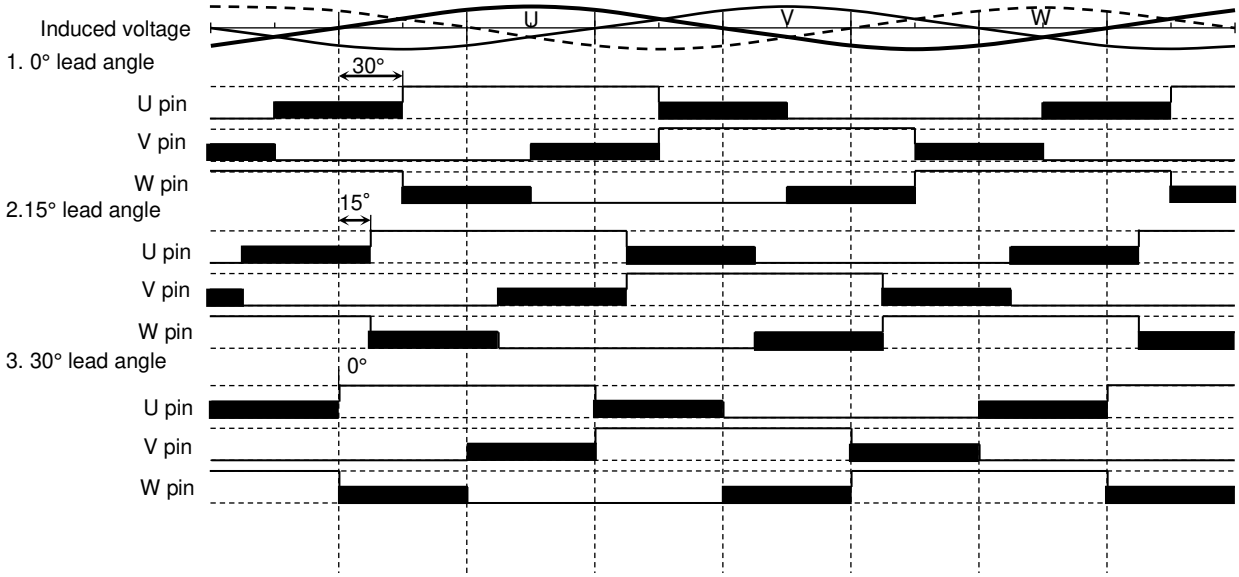
Note: When 135° commutation is selected, upper limit of the lead angle is 22.5°. And more than 22.5° cannot be configured. Likewise, when 150° commutation is selected, upper limit of the lead angle is 15° and more than 15° cannot be configured.

ROT pin	Steps of LA setting	Voltage of LA pin (V)	Rotation speed (electrical angle) When FST pin is Low, upper (0 to 750 Hz) / When FST pin is High or Middle, lower (0 to 1.5 kHz)					
			0 Hz to less than 100 Hz	100 Hz to less than 200 Hz	200 Hz to less than 300 Hz	300 Hz to less than 400 Hz	400 Hz to less than 500 Hz	500Hz to 750 Hz
			0 Hz to less than 200 Hz	200 Hz to less than 400 Hz	400 Hz to less than 600 Hz	600 Hz to less than 800 Hz	800 Hz to less than 1 kHz	1 kHz to 1.5 kHz
High	8	2.5	30°					
	7	2.1875	26.25°					
	6	1.875	22.5°					
	5	1.5625	18.75°					
	4	1.25	15°					
	3	0.9375	11.25°					
	2	0.625	7.5°					
	1	0.3125	3.75°					
	0	0	0°					
Low	8	2.5	3.75°	11.25°	18.75°	26.25°	30°	30°
	7	2.1875	11.25°	15°	18.75°	22.5°	26.25°	30°
	6	1.875	7.5°	11.25°	15°	18.75°	22.5°	26.25°
	5	1.5625	3.75°	7.5°	11.25°	15°	18.75°	22.5°
	4	1.25	0°	3.75°	7.5°	11.25°	15°	18.75°
	3	0.9375	0°	15°	15°	15°	18.75°	22.5°
	2	0.625	7.5°	7.5°	15°	15°	18.75°	22.5°
	1	0.3125	0°	7.5°	15°	15°	18.75°	22.5°
	0	0	7.5°	15°	15°	15°	18.75°	22.5°

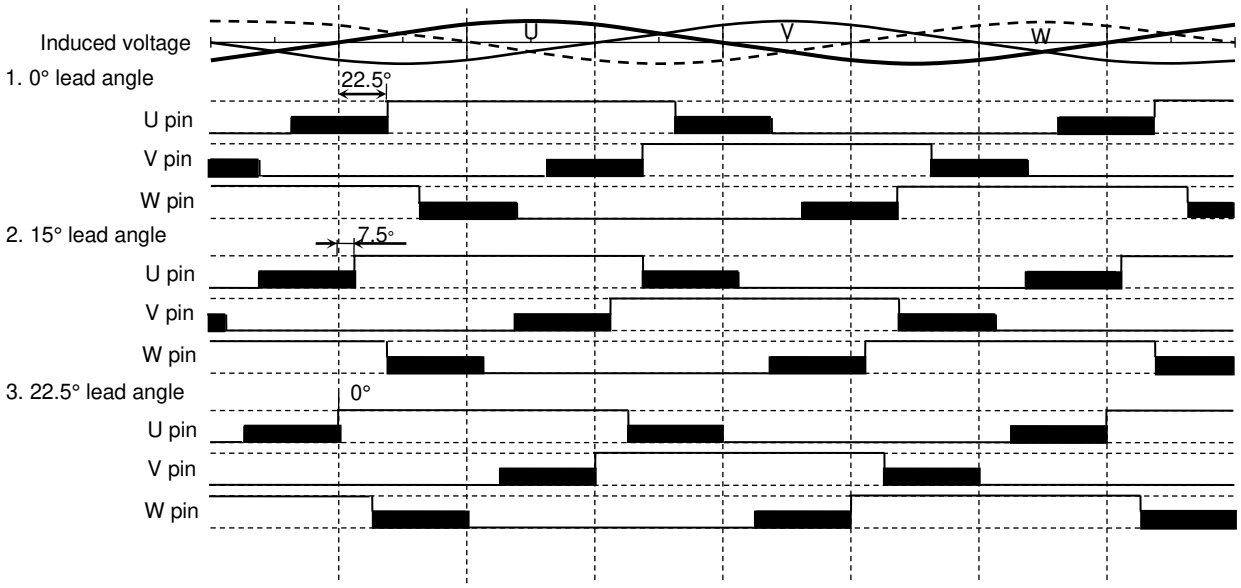


6.2 Waveform of commutation timing (CW/CCW pin = Low)

- SLOP pin = High, LAP pin = High (120° commutation)

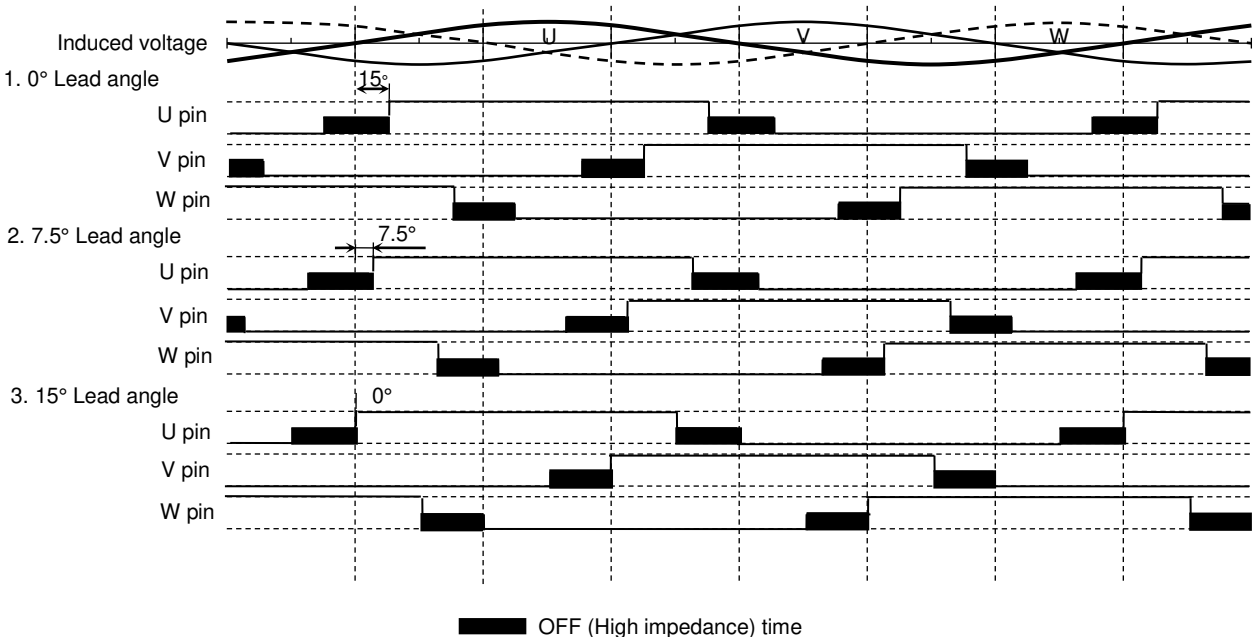


- SLOP pin = High, LAP pin = Middle (135° commutation)

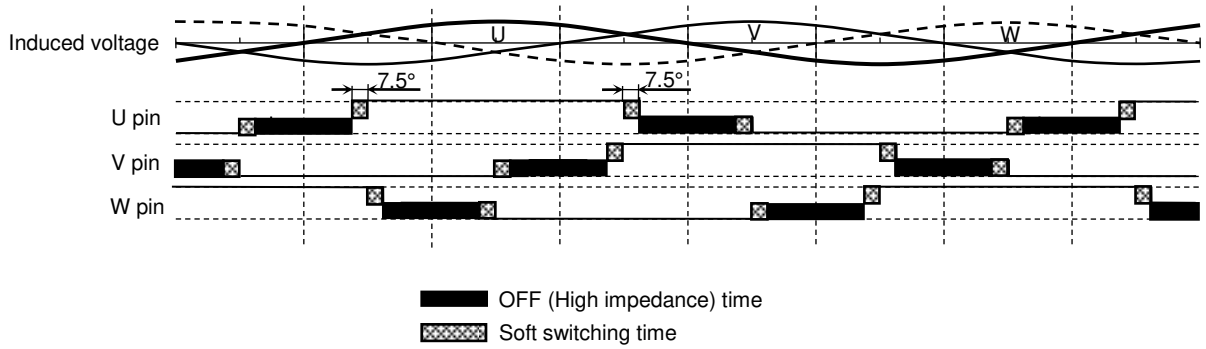


OFF (High impedance) time

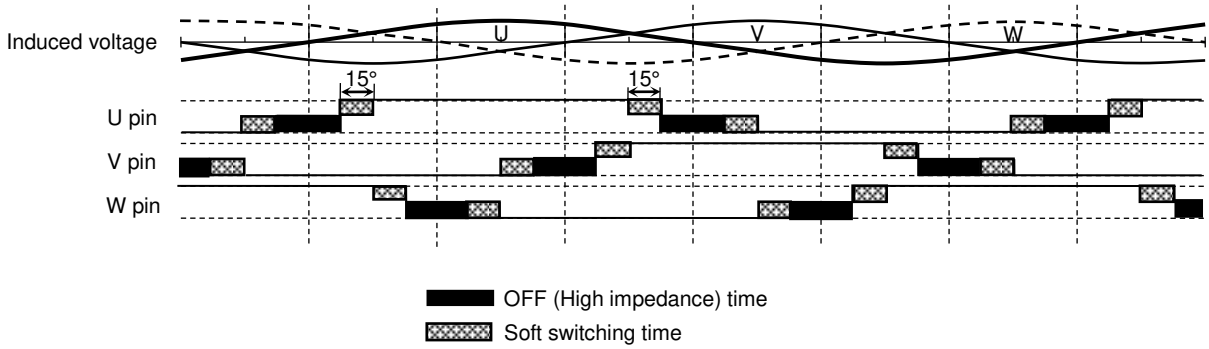
- SLOP pin = High, LAP pin = Low (150° commutation)



- SLOP pin = Low, LAP pin = Middle (135° commutation, 0° Lead angle)



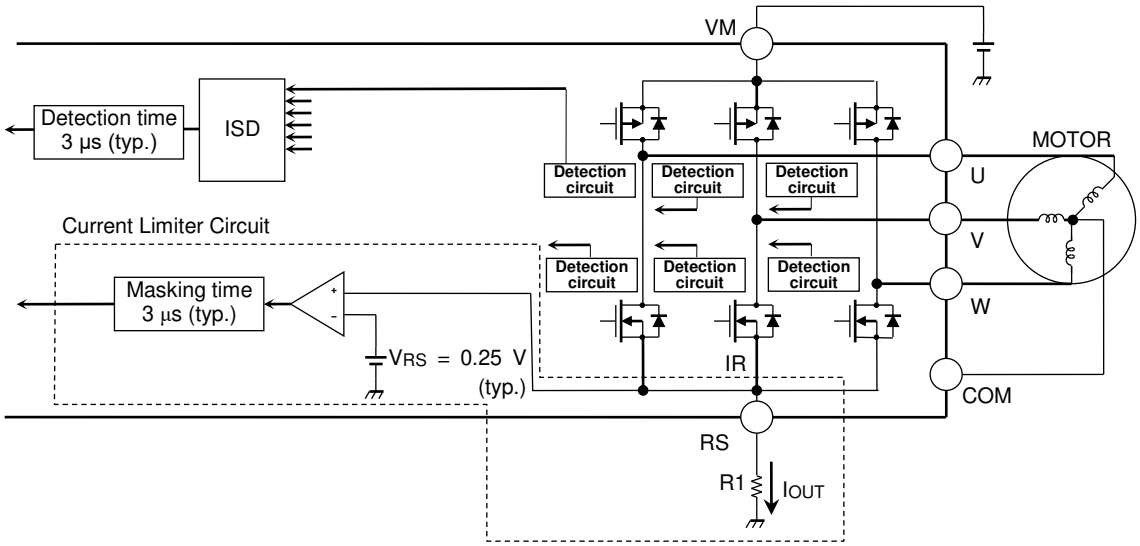
- SLOP pin = Low, LAP pin = High or Low (150° commutation, 0° Lead angle)



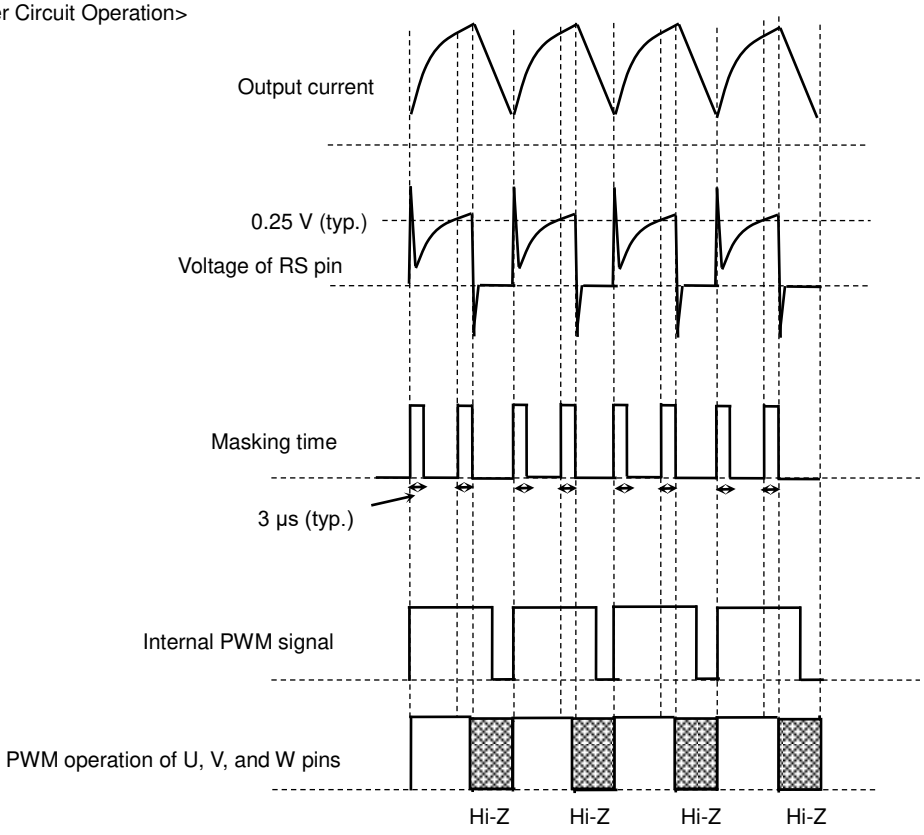
7. Current Limiter Circuit

The current limiter circuit limits the current by turning the high-side transistors off. These transistors are turned back on again when the PWM signal is turned on.
The output current is monitored as a voltage across R1 by a comparator. If it exceeds the rated V_{RS} voltage (0.25 V typ.), the current limiter is activated.
A masking time of current limit detection (T_{RS}) of 3 µs (typ.) is provided to avoid an incorrect operation by an external noise, etc.

Example: When R1 is 0.3 Ω, the current I_{OUT} which actives the current limiter circuit is shown as bellow;
I_{OUT} = 0.25 V (typ.) ÷ 0.3 Ω ≈ 0.83 A



<Current Limiter Circuit Operation>



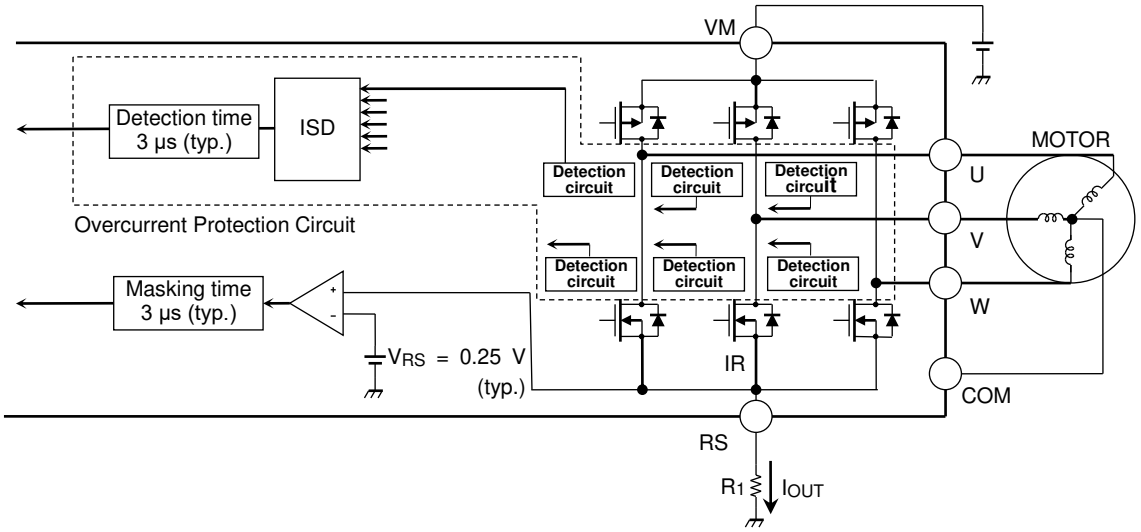
Hi-Z: High impedance

8. Overcurrent Protection Circuit (ISD)

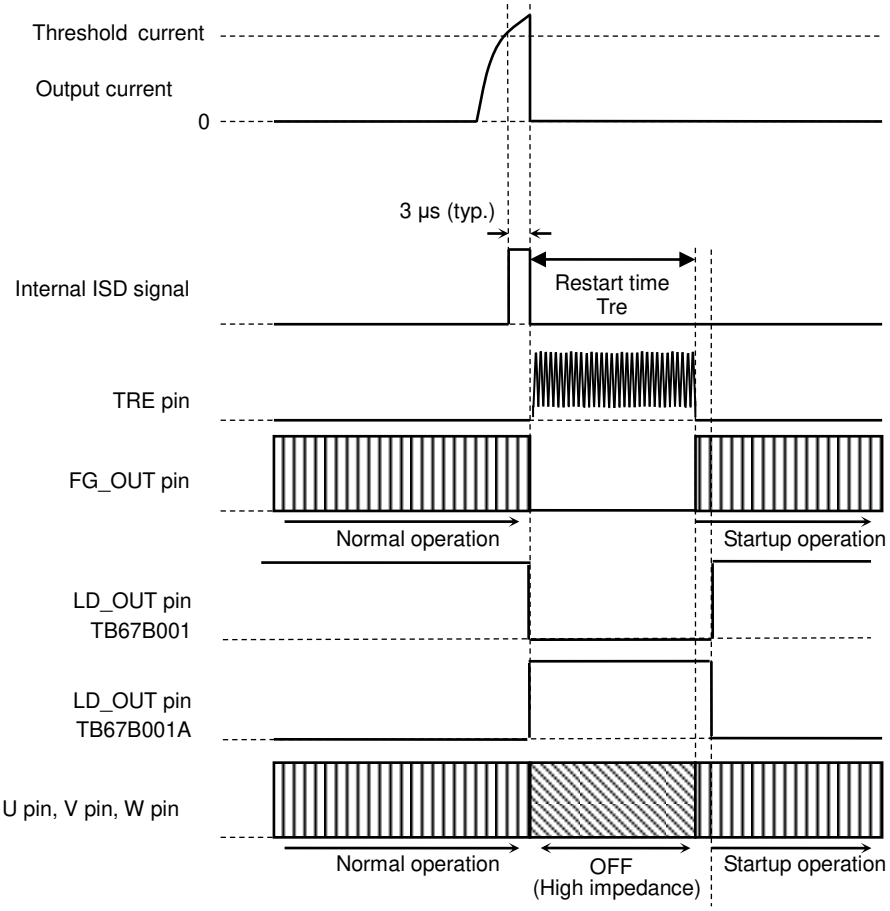
This IC incorporates the detection circuit for each six output transistors that monitors the current flowing. The six output of detection circuit are inputted to overcurrent protection circuit (ISD). The threshold current of overcurrent protection circuit is from 3 A to 6 A.

And if the current at any one of six transistors is the equal or more than the threshold current for 3 µs (Masking time of overcurrent protection circuit: T_{ISD}) (typ.) or longer, ISD makes all output transistors turning off (high impedance).

If the current at all transistors is less than the threshold current, this IC begins startup operation after the restart time (Tre) that is specified by the value of a capacitor connected to TRE pin has elapsed.



<ISD operation>



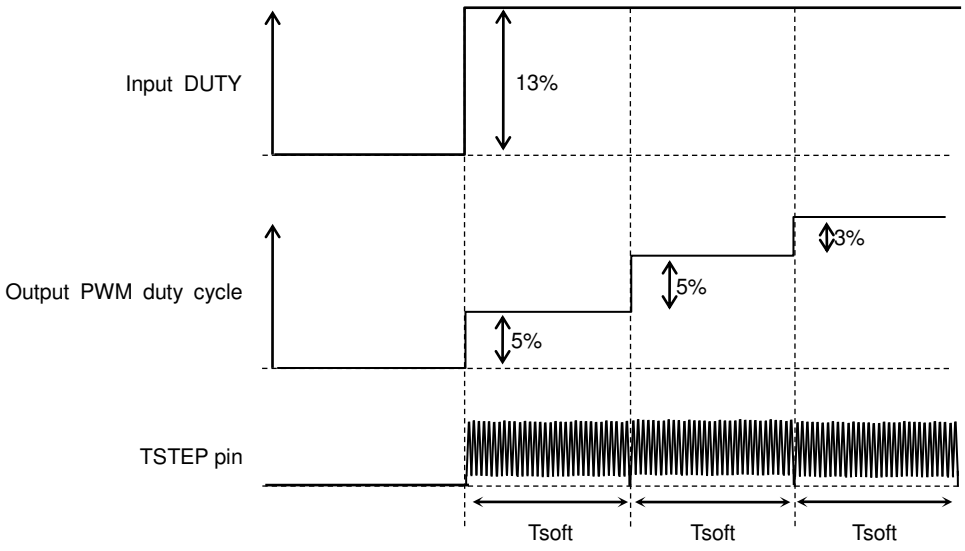
Note: When the ISD circuit is activated, the output current is more than the absolute maximum current rating. This circuit is provided as an auxiliary only and does not necessarily provide the IC with a perfect protection from damages due to overcurrent caused by power fault, ground fault, load-short and the like.

9. PWM duty cycle increasing time Control Circuit

When the value of the control signal to TSP/VSP pin is increasing, the time which is from changing the control signal to changing the output PWM duty cycle can be specified.
By the PWM duty increasing time control circuit, the output PWM duty cycle can be gradually increased in a startup operation.
The output PWM duty cycle increasing time is specified by a value of a capacitor (C) connected to TSTEP pin.

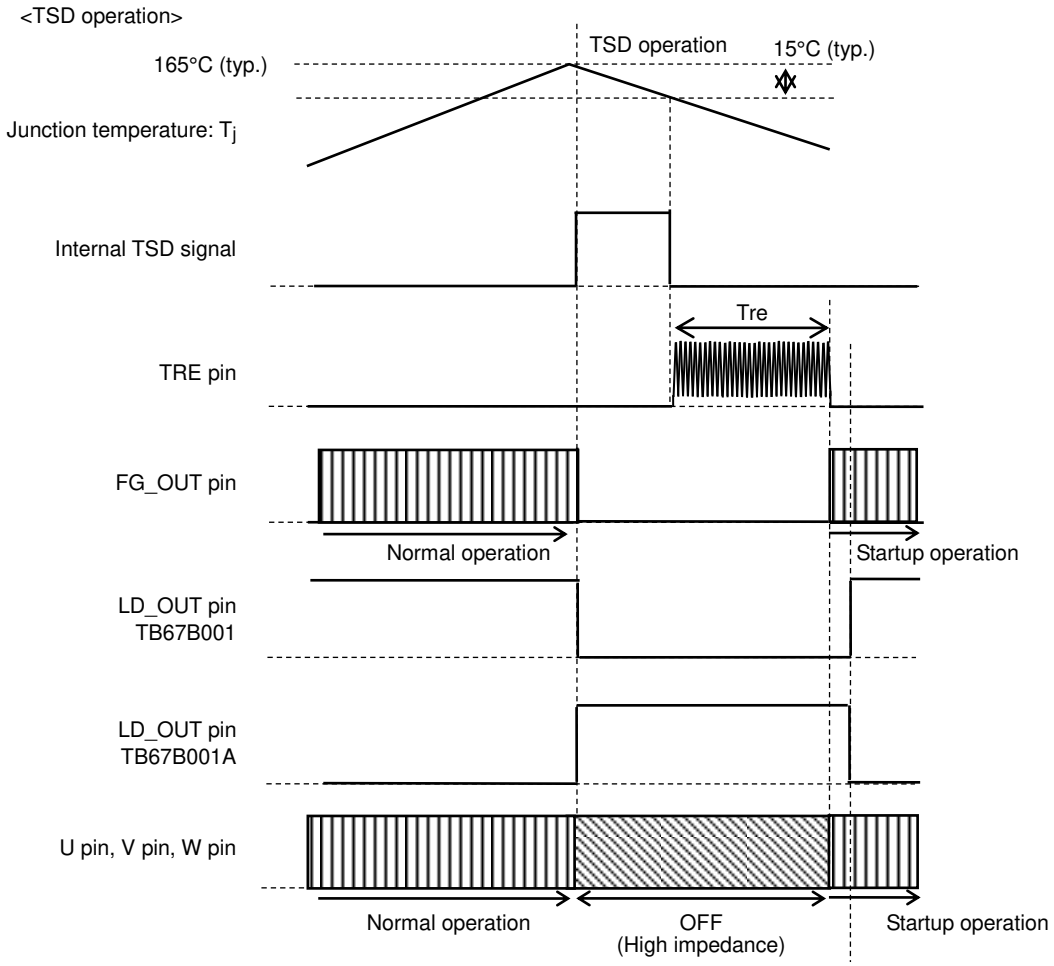
Example: PWM duty cycle increasing time: Tsoft (s) = 0.313 × 31.5 times × C (F) × 10^6
When C is 0.01 µF, Tsoft is 0.0986 s.

- When the control signal increases of 13%



10. Thermal Shutdown Circuit (TSD)

This IC has the thermal shutdown circuit (TSD). When the junction temperature (T_j) exceeds 165°C (typ.), a thermal shutdown circuit makes all output transistors turning off (high impedance). The hysteresis width of a threshold temperature of thermal shutdown circuit is 15°C (typ.).
When the junction temperature is lowered less than 150°C (typ.), this IC begins startup operation after the restart time (Tre) that is specified by the value of a capacitor connected to TRE pin has elapsed.



Note: The TSD circuit is activated if the absolute maximum junction temperature rating (T_j) of 150°C is violated. Note that the circuit is provided as an auxiliary only and does not necessarily provide the IC with a perfect protection from any kind of damages.

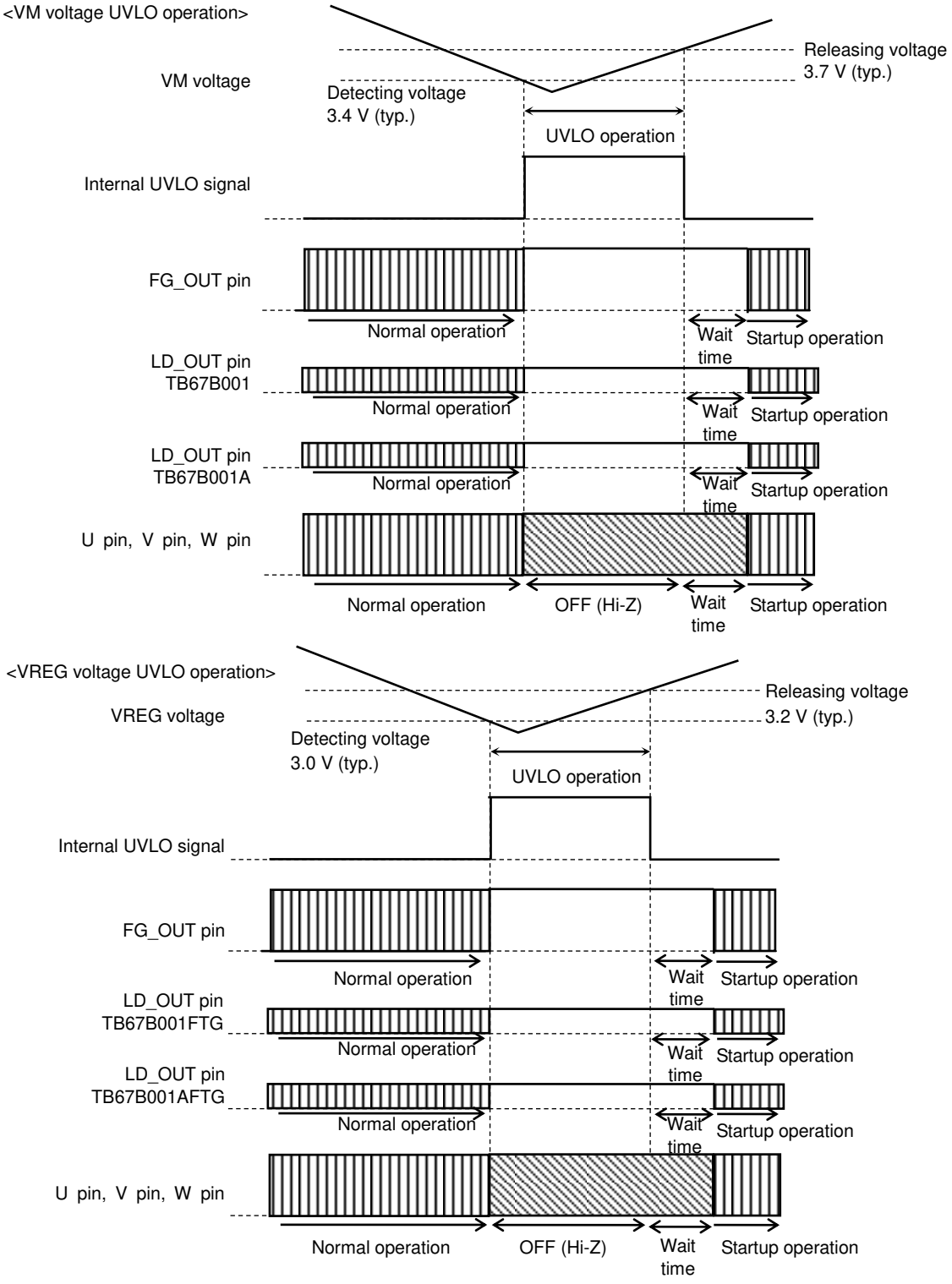
11. Under voltage Lockout Circuit (UVLO)

This IC includes an under voltage lockout circuit.

It resets the internal logic and makes all output transistors turning off (high-impedance) when VM decreases to 3.4 V (typ.) or less. The hysteresis width of under voltage lockout is 0.3 V (typ.). The releasing voltage is 3.7 V (typ.).

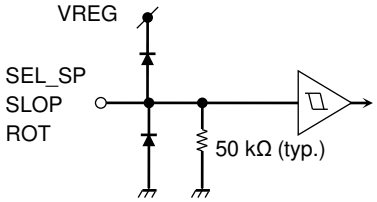
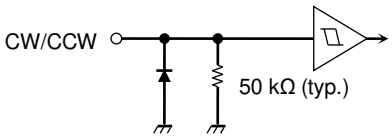
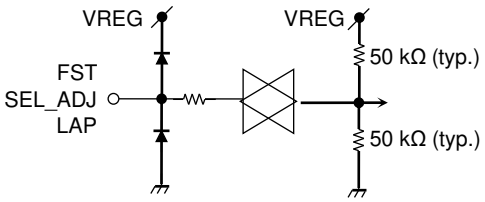
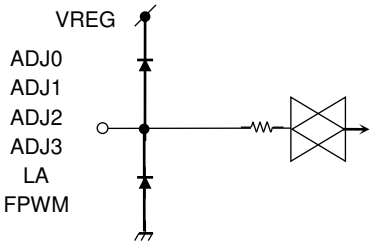
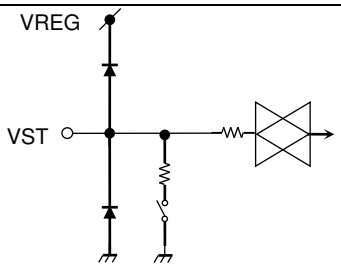
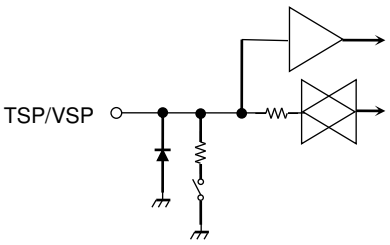
This IC resets the internal logic and makes all output transistors turning off (high-impedance) when VREG decreases to 3.0 V (typ.) or less. The hysteresis width of under voltage lockout is 0.2 V (typ.). The releasing voltage is 3.2 V (typ.).

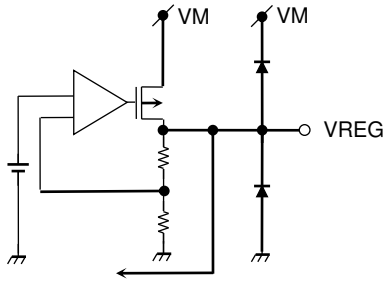
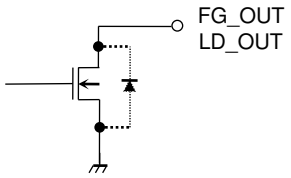
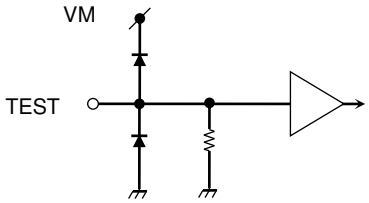
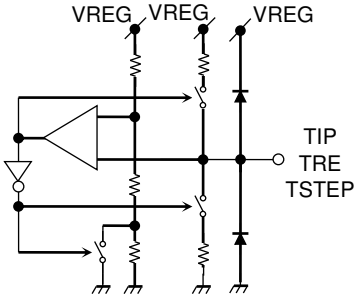
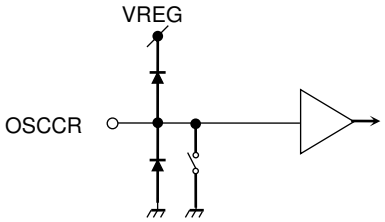
Note: Wait time in startup depends on the state of the motor; stopping and the rotation number in futile state, etc. It is approximately from 0.02 s to 0.34 s.

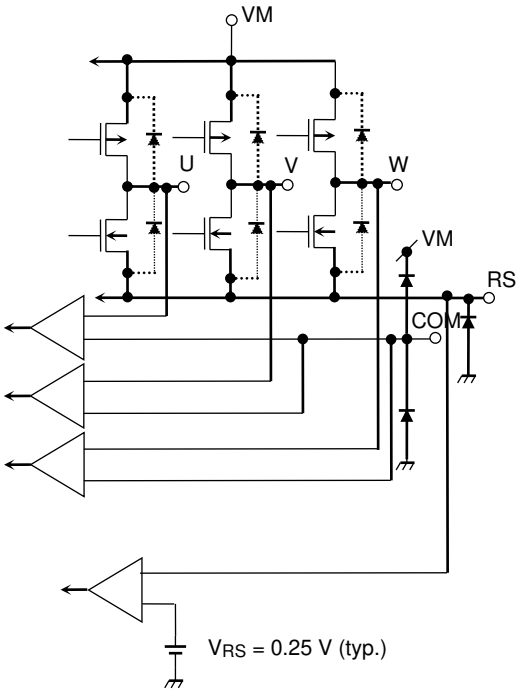


I/O Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Pin Name	I/O Signal Description	I/O Internal Circuit
SEL_SP SLOP ROT	Control signal inputted via TSP/VSP pin select input pin Soft switching select input pin Rotation speed of lead angle switching select input pin	
CW/CCW	Forward/Reverse rotation direction select input pin	
FST SEL_ADJ LAP	Forced commutation frequency select input pin PWM duty function setting input pin Overlapping commutation select pin	
ADJ0 ADJ1 ADJ2 ADJ3 LA FPWM	Adjusting pin for characteristics of speed command input Adjusting pin 1 for characteristics of output PWM duty cycle Adjusting pin 2 for characteristics of output PWM duty cycle Adjusting pin 3 for characteristics of output PWM duty cycle Lead angle setting input pin Output PWM frequency select input pin	
VST	Output PWM duty cycle setting pin in DC excitation and forced commutation modes	
TSP/VSP	Speed command input pin (PWM duty cycle control or analog voltage control) in sensorless drive mode	

Pin Name	I/O Signal Description	I/O Internal Circuit
VREG	Reference voltage output	
FG_OUT LD_OUT	Rotation speed detection signal output pin (open-drain) Lock detecting signal output pin (open-drain) An externally attached pull-up resistor enables the High output.	
TEST	Test pin Connect to ground.	
TIP TRE TSTEP	Connection pin for a capacitor to set the DC excitation time Connection pin for a capacitor to set the restart time Connection pin for a capacitor to set the Output PWM duty cycle increasing time	
OSCCR	Connection pin for the oscillator	

Pin Name	I/O Signal Description	I/O Internal Circuit
U V W VM COM RS	U-phase output V-phase output W-phase output Motor power supply pin Connection pin for the center tap of the motor Connection pin for an output shunt resistor	

Absolute Maximum Ratings (Note) (Ta = 25 °C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	VM	25	V
Input voltage	V_{IN1} (Note1)	-0.3 to 6.0	V
	V_{IN2} (Note2)	-0.3 to 25	V
	V_{IN3} (Note3)	-0.3 to VREG + 0.3	V
Output voltage	V_{OUT1} (Note4)	25	V
	V_{OUT2} (Note5)	25	V
Output current	I_{OUT1} (Note6)	3 (Note9)	A
	I_{OUT2} (Note7)	10	mA
	I_{OUT3} (Note8)	5	mA
Power dissipation	P_D	2.8 (Note10)	W
Operating temperature	T_{opr}	-40 to 105	°C
Storage temperature	T_{stg}	-55 to 150	°C

Note: The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating (s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
Please use this IC within the specified operating ranges.

Note1: V_{IN1} is applicable to the voltage at the following pins:
TSP/VSP pin and CW/CCW pin

Note2: V_{IN2} is applicable to the voltage at the following pin:
COM pin.

Note3: V_{IN3} is applicable to the voltage at the following pins.
SLOP pin, ROT pin, SEL_SP pin, ADJ0 pin, ADJ1 pin, ADJ2 pin, ADJ3 pin, OSCCR pin,
VST pin, FPWM pin, LA pin, SEL_ADJ pin, LAP pin, FST pin, TSTEP pin, TIP pin, and TRE pin

Note4: V_{OUT1} is applicable to the voltage at the following pins:
U pin, V pin, and W pin

Note5: V_{OUT2} is applicable to the voltage at the following pins:
FG_OUT pin and LD_OUT pin

Note6: I_{OUT1} is the current from the following pins:
U pin, V pin, and W pin

Note7: I_{OUT2} is the current from the following pins:
FG_OUT pin and LD_OUT pin

Note8: I_{OUT3} is the current from the following pin:
VREG pin.

Note9: Output current may be limited by the ambient temperature or the device implementation. The maximum junction temperature should not exceed 150°C

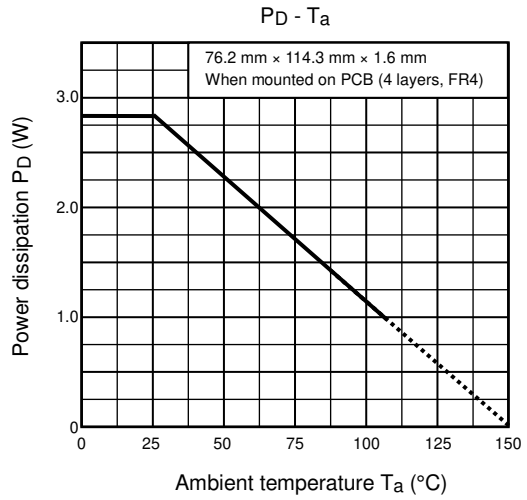
Note10: When mounted on the PCB (4 layers: FR4: 76.2 mm x 114.3 mm x 1.6 mm)

Operating Ranges

Characteristics	Symbol	Min	Typ.	Max	Unit
Power supply voltage 1	VM_{opr1}	5.5	12	22	V
Power supply voltage 2 (Note1)	VM_{opr2}	4	5	5.5	V
Input frequency of TSP/VSP pin (Note2)	foprTSP	0.4	25	100	kHz

Note 1: When voltage of VM is 5.5 V or less, the characteristics of the ON-resistance of output transistor and VREG output voltage change.
Note 2: When the control signal of TSP/VSP pin is the pulse duty (SEL_SP pin = Low).

Package Power Dissipation (Reference data)



Electrical Characteristics (Ta = 25°C, VM = 12 V, unless otherwise specified)

Characteristics	Symbol	Test Conditions	Min	Typ.	Max	Unit
Static power supply current at VM	IM	When TSP/VSP pin = 0 V	—	5.5	8	mA
Dynamic power supply current at VM	$I_{M(opr)}$	When TSP/VSP pin = VREG, RS pin = TIP pin = COM pin = 0 V	—	6	8.5	mA
Input current	$I_{IN1(H)}$	When V_{IN} = 5 V FST, LAP, SEL_ADJ pins	—	100	150	µA
	$I_{IN1(L)}$	When V_{IN} = 0 V, FST, LAP, SEL_ADJ pins	-150	-100	—	
	I_{IN2A}	When V_{IN} = 0 V to VREG and SEL_SP = VREG TSP/VSP pin	-1	—	1	
	$I_{IN2D(H)}$	When V_{IN} = VREG and SEL_SP pin = 0 V TSP/VSP pin	—	100	150	
	$I_{IN2D(L)}$	When V_{IN} = 0 V and SEL_SP pin = 0 V TSP/VSP pin	-1	—	1	
	I_{IN3}	When V_{IN} = 0 V to VREG ADJ0, ADJ1, ADJ2, ADJ3, VST, LA, FPWM pins	-1	—	1	
	$I_{IN4(H)}$	When V_{IN} = 5 V SEL_SP, CW/CCW, SLOP, ROT pin	—	100	150	
	$I_{IN4(L)}$	When V_{IN} = 0 V SEL_SP, CW/CCW, SLOP, ROT pin	-1	0	—	
Input voltage	$V_{IN1(H)}$	When SEL_SP pin = 0 V TSP/VSP pin	2.0	—	—	V
	$V_{IN1(L)}$		0	—	0.8	
	$V_{IN2(H)}$	FST, LAP, SEL_ADJ pins	VREG × 0.8	—	VREG + 0.3	
	$V_{IN2(M)}$		VREG × 0.4	—	VREG × 0.6	
	$V_{IN2(L)}$		0	—	VREG × 0.2	
	$V_{IN3(H)}$	SEL_SP, CW/CCW, SLOP, ROT pins	2.0	—	—	
	$V_{IN3(L)}$	SEL_SP, CW/CCW, SLOP, ROT pins	0	—	0.8	
Input voltage hysteresis	V1hys	When SEL_SP pin = 0 V TSP/VSP pin (Reference data)	—	0.12	—	V
	V2hys	SEL_SP, CW/CCW, SLOP pins (Reference data)	—	0.12	—	
Output PWM duty cycle increasing time	Tsoft	When a value of the capacitor connected to TSTEP pin = 0.01 µF (Reference data)	—	0.0986	—	s
DC excitation time	Tip	When a value of the capacitor connected to TIP pin = 0.1 µF (Reference data)	—	0.986	—	s
Restart time	Tre	When a value of the capacitor connected to TRE pin = 1 µF (Reference data)	—	9.86	—	s
High-level output voltage at TIP, TRE, and TSTEP pins	VH	—	2.25	2.5	2.75	V
Low-level output voltage at TIP, TRE, and TSTEP pins	VL	—	0.45	0.5	0.55	V
COM pin input current	I_{COM}	—	-5	-1.3	1	µA
Position detection comparator offset voltage	Voffset	(Reference data)	-10	0	10	mV
Low-level output voltage at FG_OUT / LD_OUT pins	V_{LFG_OUT}	When I_{OUT} = 5 mA	0	—	0.5	V
Leakage current at FG_OUT / LD_OUT pins	I_{LFG_OUT}	When V_{OUT} = 25 V	—	0	2	µA

Characteristics	Symbol	Test Conditions	Min	Typ.	Max	Unit
ON-resistance of Output transistor at the U, V and W pins	$R_{ON1(H)}$	When I_{OUT} = -0.1 A	—	0.3	0.6	Ω
	$R_{ON1(L)}$	When I_{OUT} = 0.1 A	—	0.3	0.6	
	$R_{ON2(H)}$	When I_{OUT} = -0.1 A, VM = 4.0 V	—	0.33	0.6	
	$R_{ON2(L)}$	When I_{OUT} = 0.1 A, VM = 4.0 V	—	0.33	0.6	
Output leakage current at the U, V and W pins	$I_{L(H)}$	When V_{OUT} = 0 V	-10	0	—	μA
	$I_{L(L)}$	When V_{OUT} = 25 V	—	0	10	
Output diodes' forward voltage at the U, V and W pins	$V_{F(H)}$	When I_{OUT} = 1.5 A (Reference data)	—	1.0	1.4	V
	$V_{F(L)}$	When I_{OUT} = -1.5 A (Reference data)	—	1.0	1.4	
VST ON resistance in power on	RVST	—	—	600	1000	Ω
TSP/VSP I/O characteristics in analog voltage control	$V_{AD(L)}$	Voltage of TSP/VSP pin when output PWM duty cycle = 0% in SEL_SP pin = High	0.56	0.625	0.69	V
	$V_{AD(H)}$	Voltage of TSP/VSP pin when output PWM duty cycle = 100% in SEL_SP pin = High	2.81	3.125	—	
Masking time of current limit detection	T_{RS}	(Reference data)	—	3	—	μs
Voltage of RS pin for current limit detection	V_{RS}	—	0.225	0.25	0.275	V
PWM oscillation frequency	FPWM4	(Reference data)	171.5	190.6	209.7	kHz
	FPWM3	(Reference data)	85.7	95.3	104.9	
	FPWM2	(Reference data)	42.8	47.7	52.5	
	FPWM1	(Reference data)	21.4	23.8	26.3	
OSC frequency	OSC	When R = 20 kΩ and C = 180 pF (Reference data)	10.98	12.2	13.42	MHz
Masking time of overcurrent protection circuit	T_{ISD}	(Reference data)	—	3	—	μs
Threshold current of overcurrent protection circuit	I_{ISD}	(Reference data)	3	4.5	6	A
Threshold temperature of thermal shutdown circuit	TSD	(Reference data)	—	165	—	°C
	TSDhys	Hysteresis width (Reference data)	—	15	—	
UVLO detection voltage at the VM pin	VMUVLO	—	3.1	3.4	3.7	V
UVLO releasing voltage at the VM pin	VMUVLOR	—	3.4	3.7	3.98	V
UVLO detection voltage at the VREG pin	VREGUVLO	—	2.7	3.0	3.3	V
UVLO releasing voltage at the VREG pin	VREGUVLOR	—	2.9	3.2	3.45	V
VREG output voltage	VREG1	When IVREG = -5 mA	4.5	5	5.5	V
	VREG2	When IVREG = -5 mA, VM = 4.0 V	3.6	3.9	4.0	V

Note: The characteristics which has "Reference data" does not implement testing before shipping.

Application Circuit Example

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.
The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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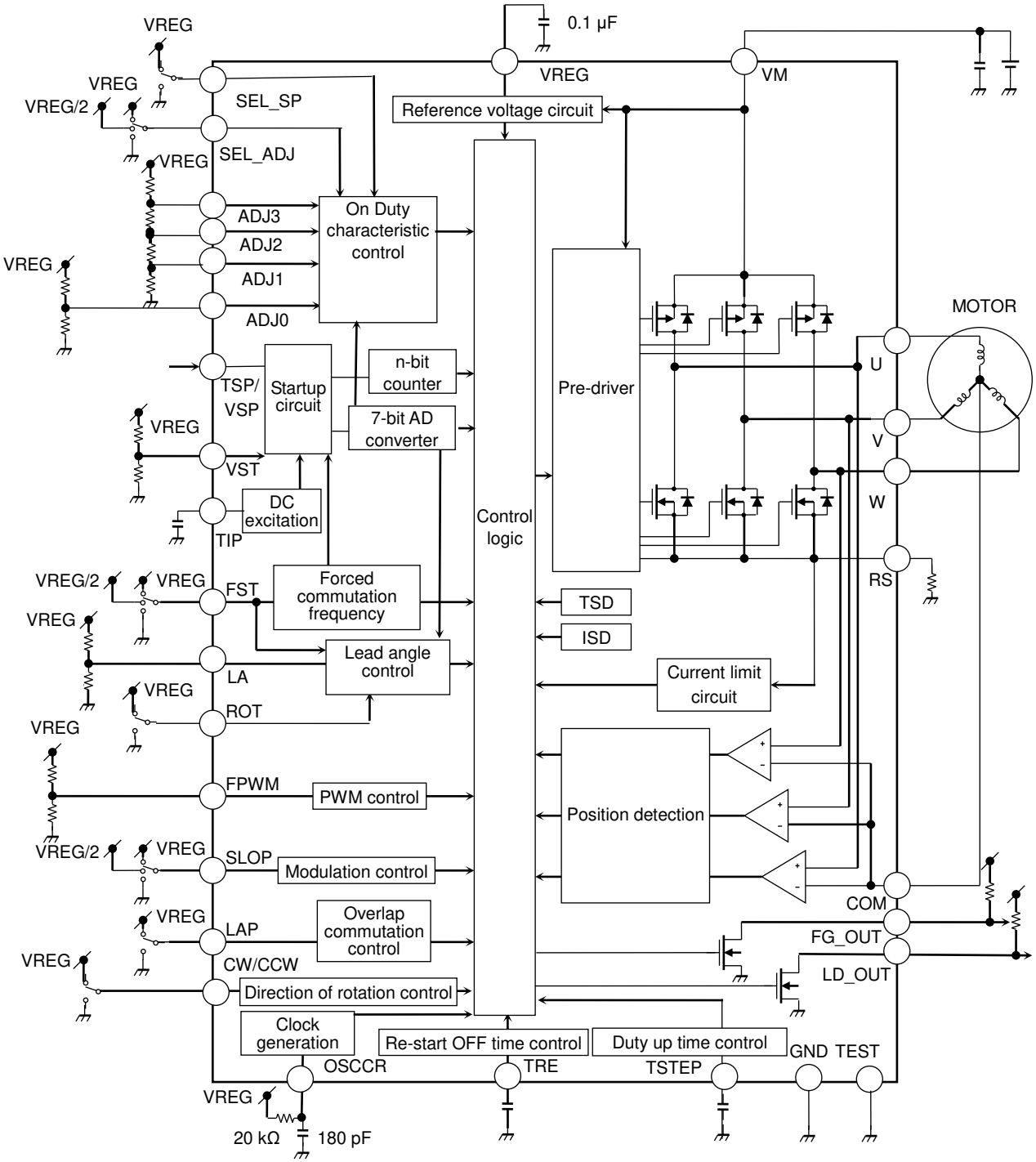
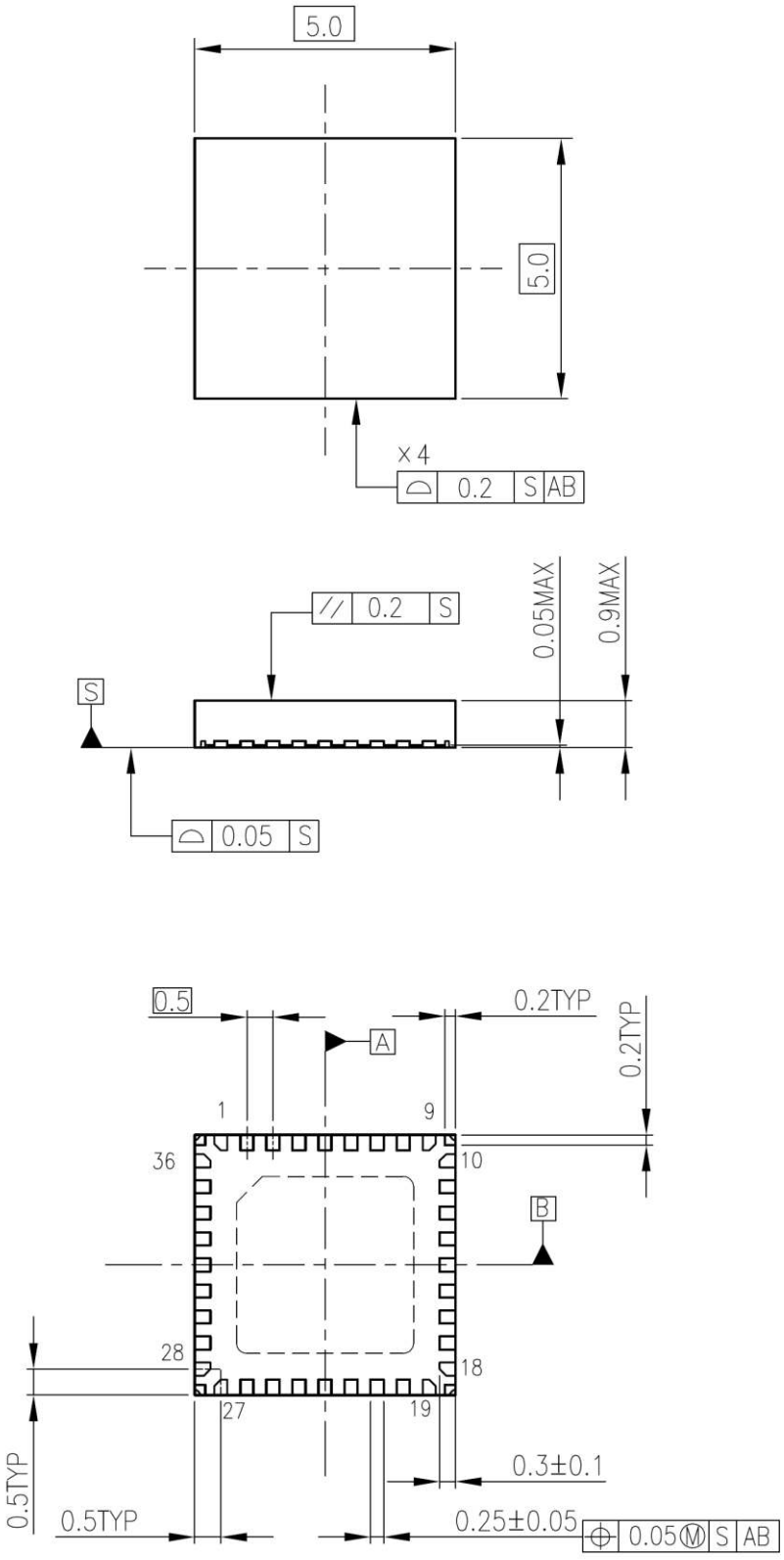


Package Dimensions

P-VQFN36-0505-0.50-001

Unit: mm



Weight: 0.05 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.

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IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to remember on handling of ICs

(1) Over current Protection Circuit
Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF
When a motor reverses the rotation direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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