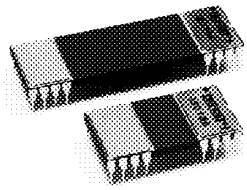
BURR-BROWN®



ISO102
ISO106

SIGNAL ISOLATION BUFFER AMPLIFIERS

FEATURES

- 14-BIT LINEARITY
- INDUSTRY'S FIRST HERMETIC ISOLATION AMPLIFIERS AT LOW COST
- EASY-TO-USE COMPLETE CIRCUIT
- RUGGED BARRIER, HV CERAMIC CAPACITORS
- 100% TESTED FOR HIGH VOLTAGE BREAKDOWN
  ISO102: 4000Vrms/10s, 1500Vrms/1min
  ISO106: 8000Vpk/10s, 3500Vrms/1min
- ULTRA HIGH IMR: 125dB min at 60Hz, ISO106
- WIDE INPUT RANGE: –10V to +10V
- WIDE BANDWIDTH: 70kHz
- VOLTAGE REFERENCE OUTPUT: 5VDC

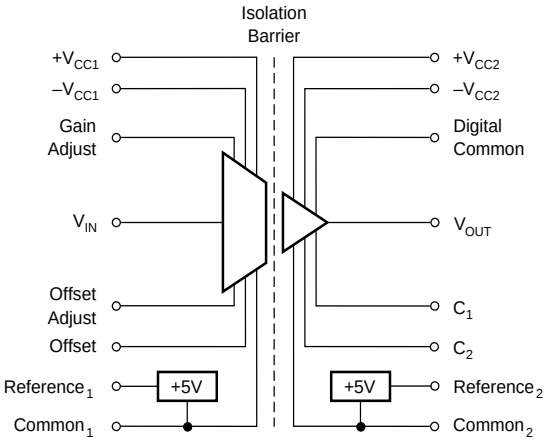
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer channel isolator for thermocouples, RTDs, pressure bridges, flow meters
- 4mA TO 20mA LOOP ISOLATION
- MOTOR AND SCR CONTROL
- GROUND LOOP ELIMINATION
- BIOMEDICAL/ANALYTICAL MEASUREMENTS
- POWER PLANT MONITORING
- DATA ACQUISITION/TEST EQUIPMENT ISOLATION
- MILITARY EQUIPMENT

DESCRIPTION

The ISO102 and ISO106 isolation buffer amplifiers are two members of our series of capacitive coupled isolation products from Burr-Brown. They have the same electrical performance and they differ in accuracy. The ISO102 is rated for 1500Vrms in a 24-pin DIP. The ISO106 is rated for 3500Vrms in a 40-pin DIP. Both side-brazed DIPs are 600mil wide and have industry standard package dimensions with the exception of missing pins between input and output stages. This permits utilization of automatic insertion techniques in production. The three-chip hybrid with its generous high voltage spacing is easy to use (no external components are required).

Each buffer accurately isolates ±10V analog signals by digitally encoding the input voltage and uniquely coupling across a differential ceramic capacitive barrier. All elements necessary for operation are contained within the DIP. This provides compact signal isolation in a hermetic package.



Covered by patent number 4,748,419 and others pending.

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SBOS151

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $V_{CC1} = V_{CC2}$ = ±15V unless otherwise noted.

PARAMETER	CONDITIONS	ISO102, ISO106, ISO102B, ISO106B MIN	TYP	MAX	UNITS
ISOLATION					
Voltage					
Rated Continuous[1]					
ISO102: AC, 60Hz	T_{MIN} to T_{MAX}	1500			Vrms
DC	T_{MIN} to T_{MAX}	2121			VDC
ISO106: AC, 60Hz	T_{MIN} to T_{MAX}	3500			Vrms
DC	T_{MIN} to T_{MAX}	4950			VDC
Test Breakdown, AC, 60Hz					
ISO102	10s	4000			Vrms
ISO106	10s	8000			Vpk
Isolation-Mode Rejection[2]	V_{ISO} = Rated Continuous, 60Hz				
AC: ISO102		115	120		dB
			1	2	µVrms/V
ISO106		125	130		dB
			0.3	0.6	µVrms/V
DC		140	160		dB
			0.01	0.10	µVDC/V
Barrier Resistance			10^{14}		Ω
Barrier Capacitance			6		pF
Leakage Current	V_{ISO} = 240Vrms, 60Hz		0.5	1	µArms
INPUT					
Voltage Range	Rated Operation	–10		+10	V
Resistance		75	100		kΩ
Capacitance			5		pF
OUTPUT					
Voltage Range	Rated Operation	–10		+10	V
	Derated Operation	–12		+12	V
Current Drive		±5			mA
Short Circuit Current		9	20	50	mA
Ripple Voltage[6]	f = 0.5MHz to 1.5MHz		3		mVp-p
Resistance			0.3	1	Ω
Capacitive Load Drive Capability		10,000			pF
Overload Recovery Time, 0.1%	$\|V_O\|$ > 12V		30		µs
OUTPUT VOLTAGE NOISE					
Voltage: f = 0.1Hz to 10Hz			300		µVp-p
f = 0.1Hz to 70kHz			16		µV/$\sqrt{Hz}$
Dynamic Range[7]: f = 0.1Hz to 70kHz	12-Bit Resolution, 1LSB, 20V FS		74		dB
f = 0.1Hz to 280Hz	16-Bit Resolution, 1LSB, 20V FS		96		dB
FREQUENCY RESPONSE					
Small Signal Bandwidth			70		kHz
Full Power Bandwidth, 0.1% THD	V_O = ±10V		5		kHz
Slew Rate	V_O = ±10V		0.5		V/µs
Settling Time, 0.1%	V_O = –10V to +10V		100		µs
Overshoot, Small Signal[8]	$C_1 = C_2$ = 0		40		%
VOLTAGE REFERENCES					
Voltage Output, Ref_1, Ref_2	No Load	+4.975	+5	+5.025	VDC
B Grade	No Load	+4.995	+5	+5.005	VDC
vs Temperature			±5	20	ppm/°C
vs Supplies			10		µV/V
vs Load			400	1000	µV/mA
Current Output		–0.1		+5	mA
Short Circuit Current		6	14	30	mA
POWER SUPPLIES					
Rated Voltage, $\pm V_{CC1}$, $\pm V_{CC2}$	Rated Performance		±15		V
Voltage Range		±10		±20	V
Quiescent Current: $+V_{CC1}$	No Load		+11	+15	mA
$-V_{CC1}$			–9	–12	mA
$+V_{CC2}$			+25	+33	mA
$-V_{CC2}$			–15	–20	mA
Dissipation: $\pm V_{CC1}$			300	400	mW
$\pm V_{CC2}$			600	800	mW
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating[9]		–25		+85	°C
Storage		–65		+150	°C
Thermal Resistance, θ_{JA}			40		°C/W
θ_{JC}			12		°C/W

ELECTRICAL (CONT)

PARAMETER	CONDITIONS	ISO102 MIN	ISO102 TYP	ISO102 MAX	ISO102B MIN	ISO102B TYP	ISO102B MAX	UNITS
GAIN								
Nominal Gain			1			*		V/V
Initial Error[3]			±0.1	±0.25		0.07	0.13	% FSR
Gain vs Temperature			±20	±50		±12	±25	ppm FSR/°C
Nonlinearity[4]	V_O = –10V to +10V		±0.007	±0.012		±0.002	±0.003	% FSR
INPUT OFFSET VOLTAGE								
Initial Offset	V_{IN} = 0V		±25	±70		±15	±25	mV
vs Temperature			±250	±500		±150	±250	µV/°C
vs Power Supplies[5]	Input Stage, V_{CC1} = ±10V to ±20V	0	1.4	4.0	*	*	*	mV/V
	Output Stage, V_{CC2} = ±10V to ±20V	–4	–1.4	0	*	*	*	mV/V

PARAMETER	CONDITIONS	ISO106 MIN	ISO106 TYP	ISO106 MAX	ISO106B MIN	ISO106B TYP	ISO106B MAX	UNITS
GAIN								
Nominal Gain			1			*		V/V
Initial Error[3]			±0.1	±0.25		0.07	*	% FSR
Gain vs Temperature			±20	±50		±12	±25	ppm FSR/°C
Nonlinearity[4]	V_O = –10V to +10V		±0.04	±0.075		±0.007	±0.025	% FSR
INPUT OFFSET VOLTAGE								
Initial Offset	V_{IN} = 0V		±25	±70		*	*	mV
vs Temperature			±250	±500		±150	±250	µV/°C
vs Power Supplies[5]	Input Stage, V_{CC1} = ±10V to ±20V		3.7			*		mV/V
	Output Stage, V_{CC2} = ±10V to ±20V		–3.7			*		mV/V

* Specification same as model to the left.

NOTES: (1) 100% tested at rated continuous for one minute. (2) Isolation-mode rejection is the ratio of the change in output voltage to a change in isolation barrier voltage. It is a function of frequency as shown in the Typical Performance Curves. This is specified for barrier voltage slew rates not exceeding 100V/µs. (3) Adjustable to zero. FSR = Full Scale Range = 20V. (4) Nonlinearity is the peak deviation of the output voltage from the best fit straight line. It is expressed as the ratio of deviation to FSR. (5) Power supply rejection = change in V_{OS}/20V supply change. (6) Ripple is the residual component of the barrier carrier frequency generated internally. (7) Dynamic range = FSR/(voltage spectral noise density x square root of user bandwidth). (8) Overshoot can be eliminated by band-limiting. (9) See “Power Dissipation vs Temperature” performance curve for limitations. (10) Band limited to 10Hz, bypass capacitors located less than 0.25" from supply pins.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
ISO102	Ceramic	–25°C to +85°C
ISO102B	Ceramic	–25°C to +85°C
ISO106	Ceramic	–25°C to +85°C
ISO106B	Ceramic	–25°C to +85°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ISO102	24-Pin Ceramic	208
ISO102B	24-Pin Ceramic	208
ISO106	40-Pin Ceramic	206
ISO106B	40-Pin Ceramic	206

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply Without Damage ..... ±20V
Input Voltage Range ..... ±50V
Transient Immunity, dV/dt 100kV/µs
Continuous Isolation Voltage Across Barrier
  ISO102 ..... 1500Vrms
  ISO106 ..... 3500Vrms
Junction Temperature ..... +160°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Amplifier and Reference Output
  Short Circuit Duration ..... Continuous to Common

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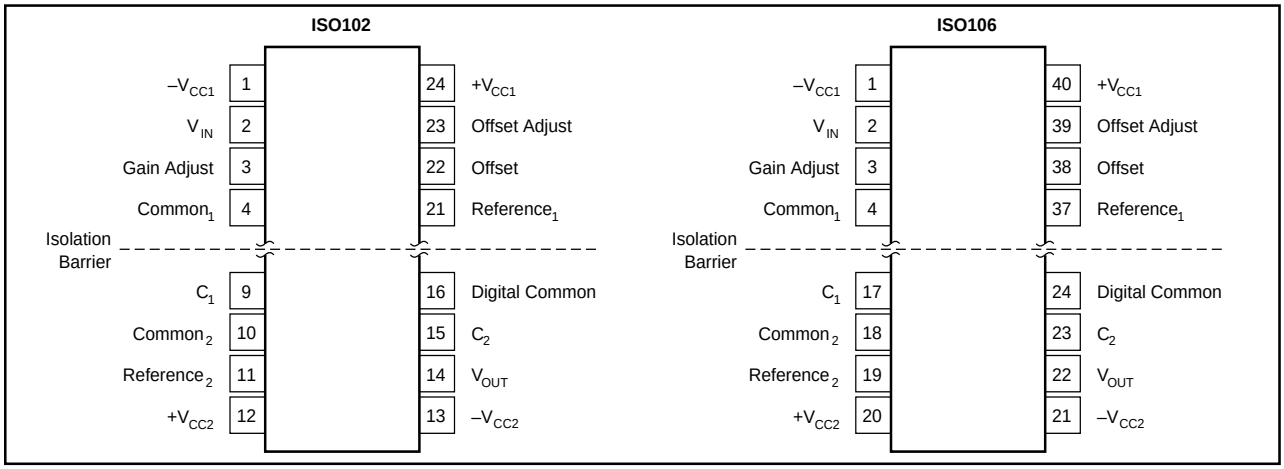
PIN CONFIGURATION



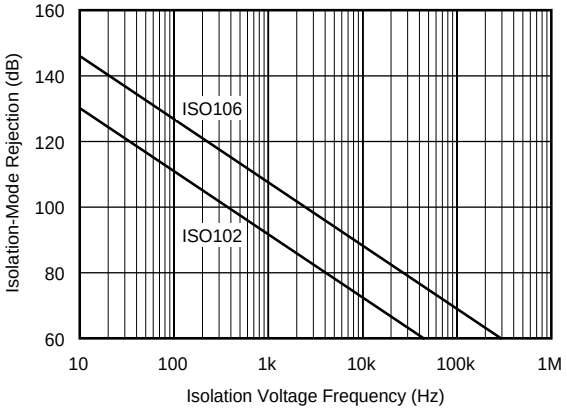
PIN DESCRIPTIONS

$\pm V_{CC1}$, $Common_1$	Positive and negative power supply voltages and common (or ground) for the input stage. $Common_1$ is the analog reference voltage for input signals. The voltage between $Common_1$ and $Common_2$ is the isolation voltage and appears across the internal high voltage barrier.
$\pm V_{CC2}$, $Common_2$	Positive and negative power supply voltages and common (or ground) for the output stage. $Common_2$ is the analog reference voltage for output signals. The voltage between $Common_1$ and $Common_2$ is the isolation voltage and appears across the internal high voltage barrier.
V_{IN}	Signal input pin. Input impedance is typically 100kΩ. The input range is rated for ±10V. The input level can actually exceed the input stage supplies. Output signal swing is limited only by the output supply voltages.
Gain Adjust	This pin is an optional signal input. A series 5kΩ potentiometer between this pin and the input signal allows a guaranteed ±1.5% gain adjustment range. When gain adjustment is not required, the Gain Adjust should be left open. Figure 4 illustrates the gain adjustment connection.
$Reference_1$	+5V reference output. This low-drift zener voltage reference is necessary for setting the bipolar offset point of the input stage. **This pin must be strapped to either Offset or Offset Adjust to allow the isolation amplifier to function.** The reference is often useful for input signal conditioning circuits. See "Effect of Reference Loading on Offset" performance curve for the effect of offset voltage change with reference loading. $Reference_1$ is identical to, but independent of, $Reference_2$. This output is short circuit protected.
$Reference_2$	+5V reference output. This reference circuit is identical to, but independent of, $Reference_1$. It controls the bipolar offset of the output stage through an internal connection. This output is short-circuit protected.
Offset	Offset input. **This input must be strapped to $Reference_1$** unless user adjustment of bipolar offset is required.
Offset Adjust	This pin is for optional offset control. When connected to the $Reference_1$ pin through a 1kΩ potentiometer, ±150mV of adjustment range is guaranteed. Under this condition, the Offset pin should be connected to the Offset Adjust pin. When offset adjustment is not required, the Offset Adjust pin is left open. See Figure 4.
Digital Common	Digital common or ground. This separate ground carries currents from the digital portions of the output stage circuit. The best grounding practices require that digital common current does not flow in analog common connections. Both pins can be tied directly to a ground plane if available. Difference in potentials between the $Common_2$ and Digital Common pins can be ±1V. See Figure 2.
V_{OUT}	Signal output. Because the isolation amplifier has unity gain, the output signal is ideally identical to the input signal. The output is low impedance and is short-circuit protected. This signal is referenced to $Common_2$; subsequent circuitry should have a separate "sense" connection to $Common_1$ as well as V_{OUT}.
C_1, C_2	Capacitors for small signal bandwidth control. These pins connect to the internal rolloff frequency controlling nodes of the output low-pass filter. Additional capacitance added to these pins will modify the bandwidth of the buffer. C_2 is always twice the value of C_1. See "Bandwidth Control" performance curve for the relationship between bandwidth and C_1 and C_2. When no connections are made to these pins, the full small-signal bandwidth is maintained. Be sure to shield C_1 and C_2 pins from high electric fields on the PC board. This preserves AC isolation-mode rejection by reducing capacitive coupling effects.

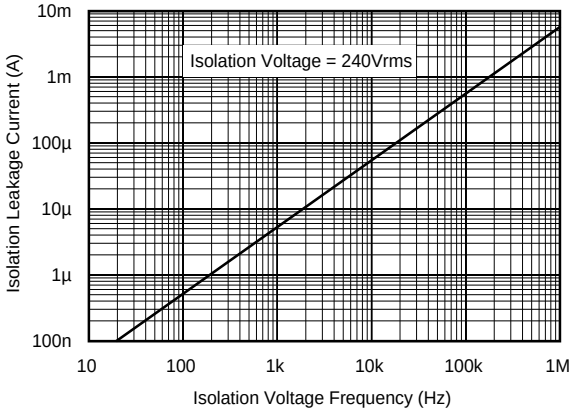
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

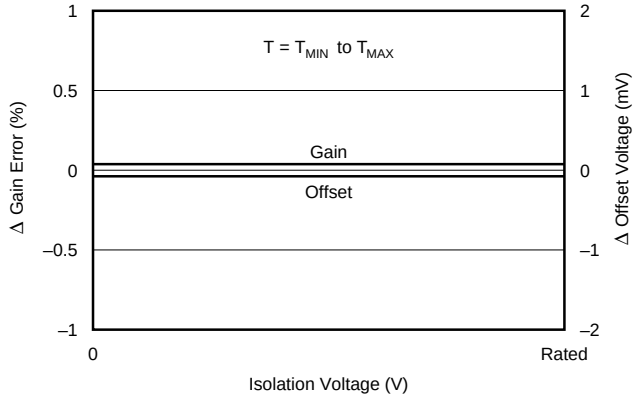
ISOLATION-MODE REJECTION
vs ISOLATION VOLTAGE FREQUENCY



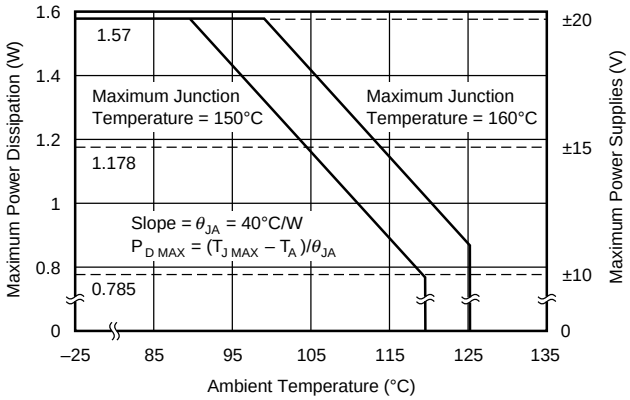
ISOLATION LEAKAGE CURRENT
vs ISOLATION VOLTAGE FREQUENCY



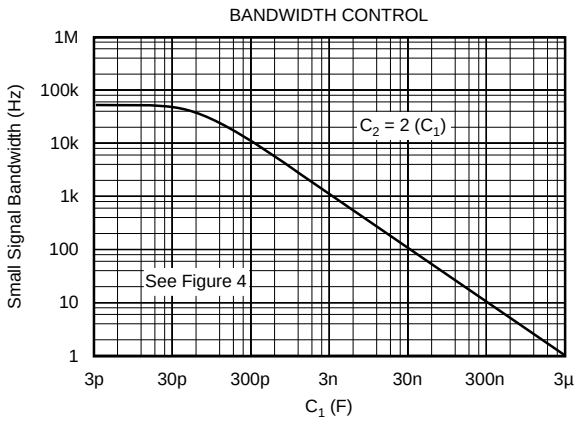
Δ GAIN ERROR AND Δ OFFSET VOLTAGE
vs ISOLATION VOLTAGE



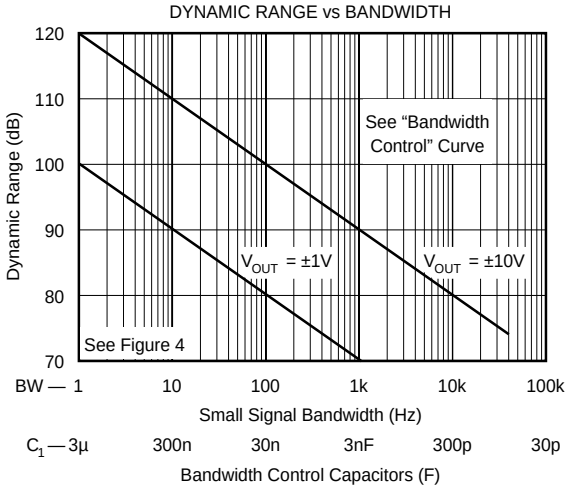
POWER DISSIPATION vs TEMPERATURE



BANDWIDTH CONTROL



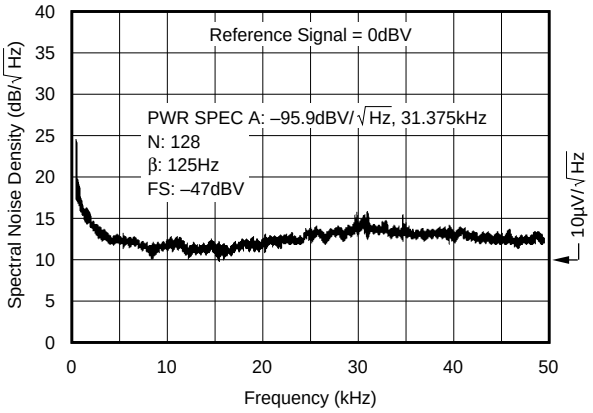
DYNAMIC RANGE vs BANDWIDTH



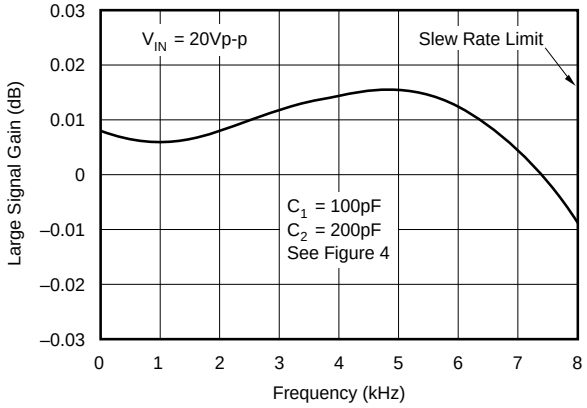
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

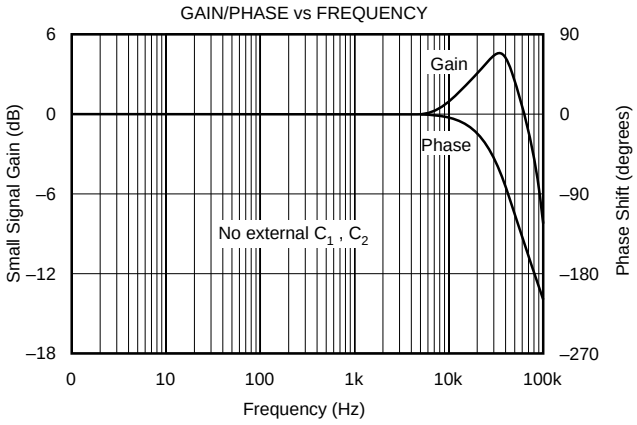
OUTPUT SPECTRAL NOISE DENSITY



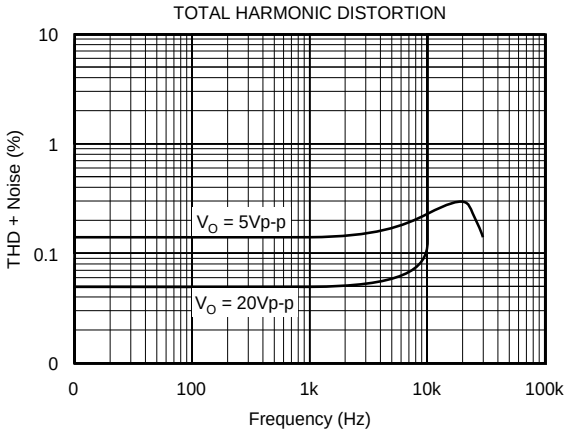
GAIN FLATNESS vs FREQUENCY



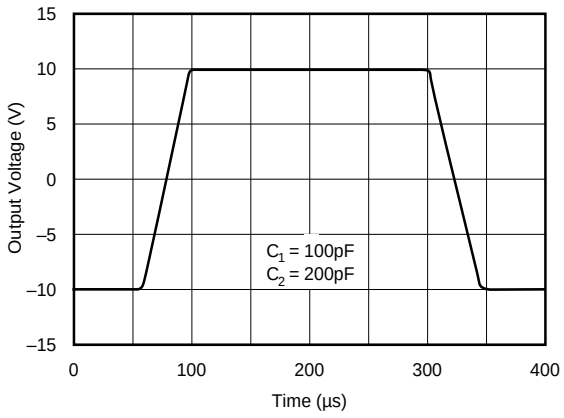
GAIN/PHASE vs FREQUENCY



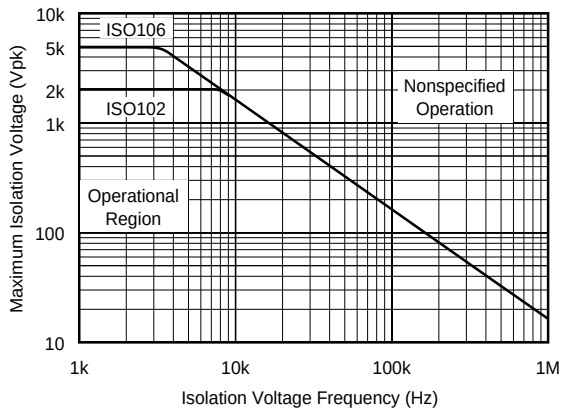
TOTAL HARMONIC DISTORTION



LARGE SIGNAL TRANSIENT RESPONSE



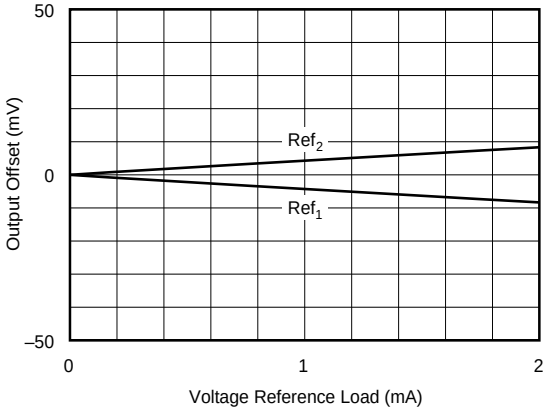
RECOMMENDED RANGE OF ISOLATION VOLTAGE



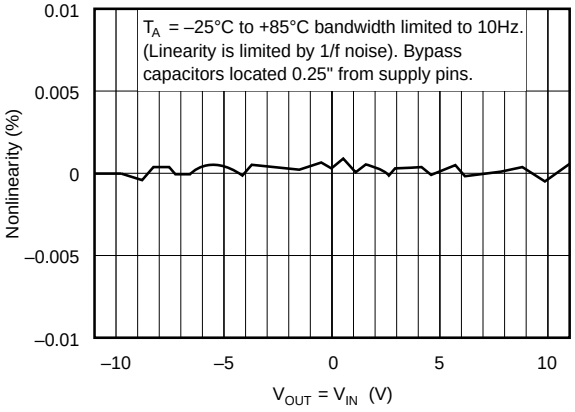
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

EFFECT OF REFERENCE LOADING ON OFFSET



ISO102B TYPICAL LINEARITY



THEORY OF OPERATION

The ISO102 and ISO106 have no galvanic connection between the input and output. The analog input signal referenced to the input common is accurately duplicated at the output referenced to the output common. Because the barrier information is digital, potentials between the two commons can assume a wide range of voltages and frequencies without influencing the output signal. Signal information remains undisturbed until the slew rate of the barrier voltage exceeds 100V/µs. The isolation amplifier's ability to reject fast dV/dt changes between the two grounds is specified as transient immunity. The amplifier is protected from damage for slew rates up to 100,000V/µs.

A simplified diagram of the ISO102 and ISO106 is shown in Figure 1. The design consists of an input voltage-controlled oscillator (VCO) also known as a voltage-to-frequency converter (VFC), differential capacitors, and output phase lock loop (PLL). The input VCO drives digital levels directly into the two 3pF barrier capacitors. The digital signal is frequency modulated and appears differentially across the barrier, while the externally applied isolation voltage appears common-mode.

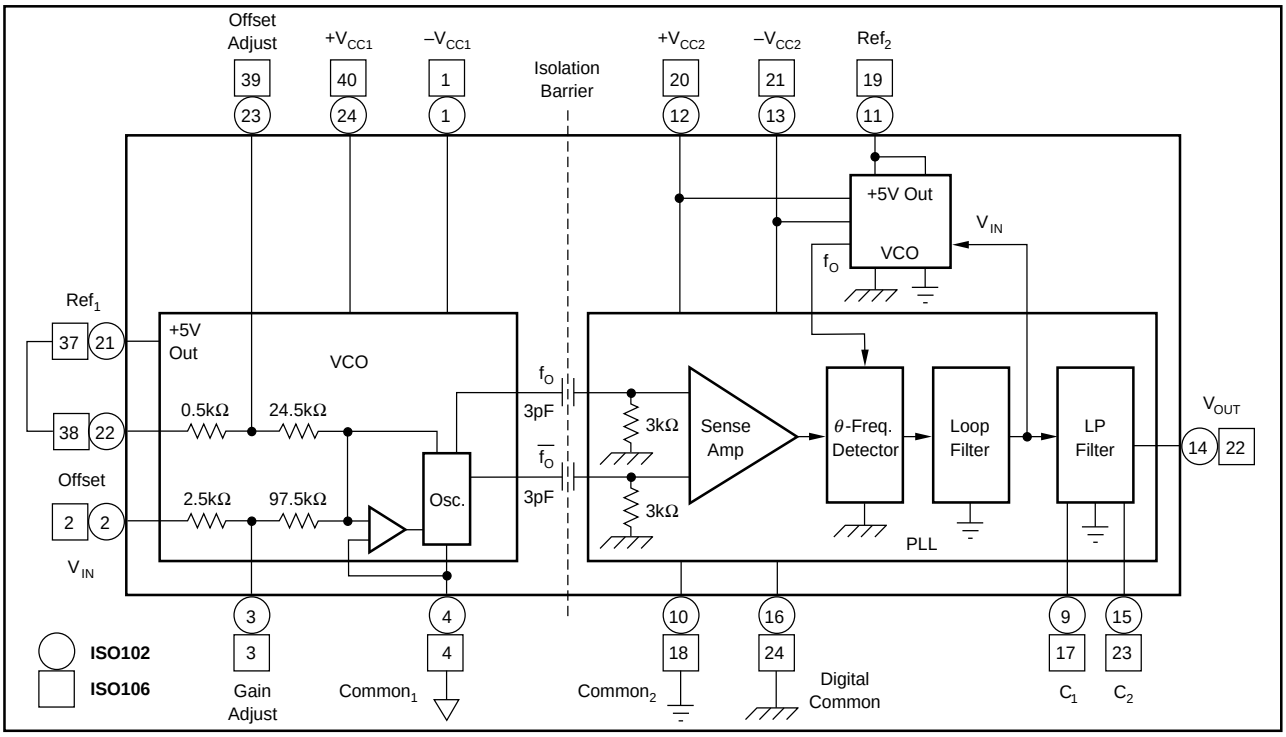


FIGURE 1. Simplified Diagram of ISO102 and ISO106.

A sense amplifier detects only the differential information. The output stage decodes the frequency modulated signal by the means of a PLL. The feedback of the PLL employs a second VCO that is identical to the encoder VCO. The PLL forces the second VCO to operate at the same frequency (and phase) as the encoder VCO; therefore, the two VCOs have the same input voltage. The input voltage of the decoder VCO serves as the isolation buffer's output signal after passing through a 100kHz second-order active filter.

For a more detailed description of the internal operation of the ISO102 and ISO106, refer to *Proceedings of the 1987 International Symposium on Microelectronics*, pages 202-206.

ABOUT THE BARRIER

For any isolation product, barrier composition is of paramount importance in achieving high reliability. Both the ISO102 and ISO106 utilize two 3pF high voltage ceramic coupling capacitors. They are constructed of tungsten thick film deposited in a spiral pattern on a ceramic substrate. Capacitor plates are buried in the package, making the barrier very rugged and hermetically sealed. Capacitance results from the fringing electric fields of adjacent metal runs. Dielectric strength exceeds 10kV and resistance is typically $10^{14}\Omega$. Input and output circuitry are contained in separate solder-sealed cavities, resulting in the industry's first fully hermetic hybrid isolation amplifier.

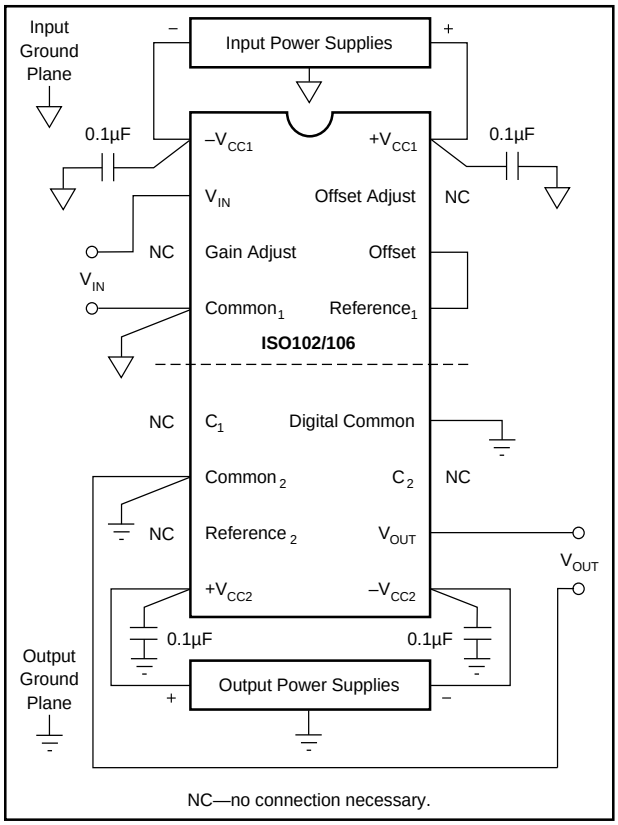


FIGURE 2. Power Supply and Signal Connection.

The ISO102 and ISO106 are designed to be free from partial discharge at rated voltages. Partial discharge is a form of localized breakdown that degrades the barrier over time. Since it does not bridge the space across the barrier, it is difficult to detect. Both isolation amplifiers have been extensively evaluated at high temperature and high voltage.

POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 2 shows the proper power supply and signal connections. Each supply should be AC-bypassed to Analog Common with 0.1µF ceramic capacitors as close to the amplifier as possible. Short leads will minimize lead inductance. A ground plane will also reduce noise problems. Signal common lines should tie directly to the common pin even if a low impedance ground plane is used. Refer to Digital Common in the Pin Descriptions table.

To avoid gain and isolation-mode rejection (IMR) errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance. Any capacitance across the barrier will increase AC leakage current and may degrade high frequency IMR. The schematic in Figure 3 shows the proper technique for wiring analog and digital commons together.

DISCUSSION OF SPECIFICATIONS

The IS0102 and IS0106 are unity gain buffer isolation amplifiers primarily intended for high level input voltages on the order of 1V to 10V. They may be preceded by operational, differential, or instrumentation amplifiers that precondition a low level signal on the order of millivolts and translate it to a high level.

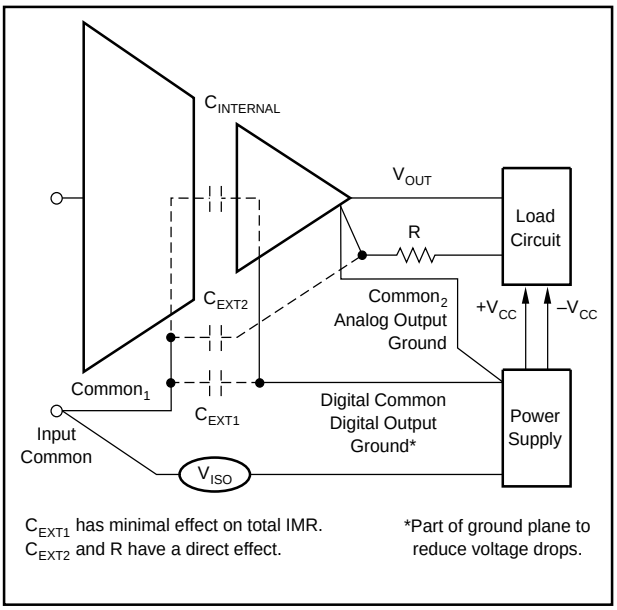


FIGURE 3. Technique for Wiring Analog and Digital Commons Together.

ISOLATION-MODE REJECTION

The IS0102 and IS0106 provide exceptionally high isolation-mode rejection over a wide range of isolation-mode voltages and frequencies. The typical performance curves should be used to insure operation within the recommended range. The maximum barrier voltage allowed decreases as the frequency of the voltage increases. As with all isolation amplifiers, a change of voltage across the barrier will induce leakage current across the barrier. In the case of the IS0102 and IS0106, there exists a threshold of leakage current through the signal capacitors that can cause over-drive of the decoder's sense amplifier. This occurs when the slew rate of the isolation voltage reaches 100V/µs. The output will recover in about 50µs from transients exceeding 100V/µs.

The first two performance curves indicate the expected isolation-mode rejection over a wide range of isolation voltage frequencies. Also plotted is the typical leakage current across the barrier at 240Vrms. The majority of the leakage current is between the input common pin and the output digital ground pin.

The IS0102 and IS0106 are intended to be continuously operated with fully rated isolation voltage and temperature without significant drift of gain and offset. See the "Gain Error/Offset Isolation Voltage" performance curve for changes in gain and offset with isolation voltage.

SUPPLY AND TEMPERATURE RANGE

The IS0102 and IS0106 are rated for +15V supplies; however, they are guaranteed to operate from ±10V to ±20V. Performance is also rated for an ambient temperature range of –25°C to +85°C. For operation outside this temperature range, refer to the "Power Dissipation vs Temperature" performance curve to establish the maximum allowed supply voltage. Supply currents are fairly insensitive to changes in supply voltage or temperature. Therefore, the maximum current limits can be used in computing the maximum junction temperature under nonrated conditions.

OPTIONAL BANDWIDTH CONTROL

The following discussion relates optimum dynamic range performance to bandwidth, noise, and settling time.

The outputs of the IS0102 and IS0106 are the outputs of a second-order low-pass Butterworth filter. Its low impedance output is rated for ±5mA drive and ±12V range with 10,000pF loads. The closed-loop bandwidth of the PLL is 70kHz, while the output filter is internally set at 100kHz. The output filter lowers the residual voltage of the barrier FM signal to below the noise floor of the output signal.

Two pins are available for optional modification of the filter's bandwidth. Only two capacitors are required. The "Bandwidth Control" performance curve gives the value of C_1 (C_2 is equal to twice C_1) for the desired bandwidth. Figure 4 illustrates the optional connection of both capacitors.

A tradeoff can be achieved between the required signal bandwidth and system dynamic range. The noise floor of the output limits the dynamic range of the output signal. The noise power varies with the square root of the bandwidth of the buffer. It is recommended that the bandwidth be reduced to about twice the maximum signal bandwidth for optimum dynamic range as shown in the "Dynamic Range vs Bandwidth" performance curve. The output spectral noise density measurement is displayed in the "Output Spectral Noise Density" performance curve. The noise is flat to within 5dB$\sqrt{\text{Hz}}$ between 0.1Hz to 70kHz.

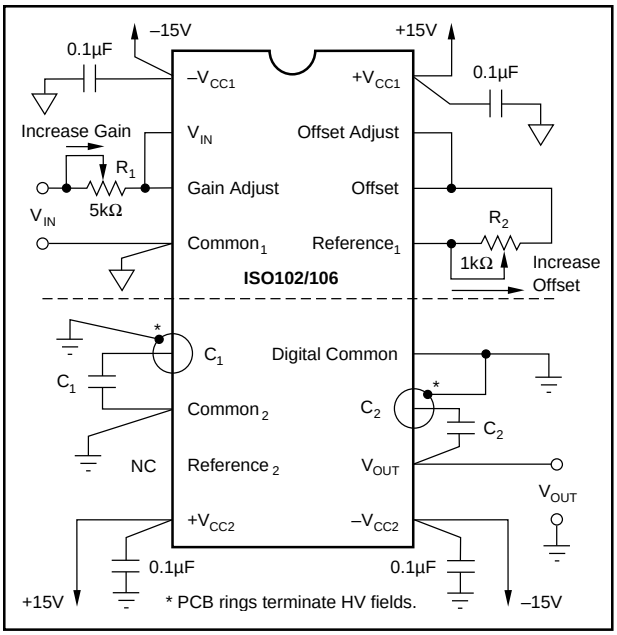


FIGURE 4. Optional Gain Adjust, Offset Adjust, and Bandwidth Control.

The overall AC gain of the buffer amplifiers is shown in two performance curves: "Gain Flatness vs Frequency" and "Gain/Phase vs Frequency." Note that with C_1 = 100pF and C_2 = 200pF, the AC gain remains flat within ±0.01dB up to 7kHz. The total harmonic distortion for large-signal sine wave outputs is plotted in the "Total Harmonic Distortion" performance curve. The phase-lock-loop displays slightly nonuniform rise and fall edges under maximum slew conditions. Reducing the output filter bandwidth to below 70kHz smoothes the output signal and eliminates any overshoot. See the "Large Signal Transient Response" performance curve.

OPTIONAL OFFSET AND GAIN ADJUSTMENT

In many applications the factory-trimmed offset is adequate. For situations where reduced or modified gain and offset are required, adjustment of each is easy. The addition of two potentiometers as shown in Figure 4 provides for a two step calibration.

Offset should be adjusted first. Gain adjustment does not interfere with offset. The potentiometer's TCR adds only 2% to overall temperature drift. The offset and gain adjustment procedures are as follows:

1. Set V_{IN} to 0V and adjust R_1 to desired offset at the output.
2. Set V_{IN} to full scale (not zero). Adjust R_2 for desired gain.

PRINTED CIRCUIT BOARD LAYOUT

The distance across the isolation barrier, between external components, and conductor patterns, should be maximized to reduce leakage and arcing at high voltages. Good layout techniques that reduce stray capacitance will assure low leakage current and high AC IMR. For some applications, applying conformal coating compound such as urethane is useful in maintaining good performance. This is especially true where dirt, grease or moisture can collect on the PC board surface, component surface, or component pins. Following this industry-accepted practice will give best results, particularly when circuits are operated or tested in a moisture-condensing environment. Optimum coating can be achieved by administering urethane under vacuum conditions. This allows complete coverage of all areas. Grounded rings around the C_1 and C_2 contacts on the board greatly reduce high voltage electric fields at these pins.

APPLICATIONS

The ISO102 and ISO106 isolation amplifiers are used in three categories of applications:

1. accurate isolation of signals from high voltage ground potentials,
2. accurate isolation of signals from severe ground noise, and
3. fault protection from high voltages in analog measurement systems.

Figures 5 through 15 show a variety of application circuits.

Additional discussion of applications can be found in the December 11, 1986 issue of *Electronic Design*, pages 91-96.

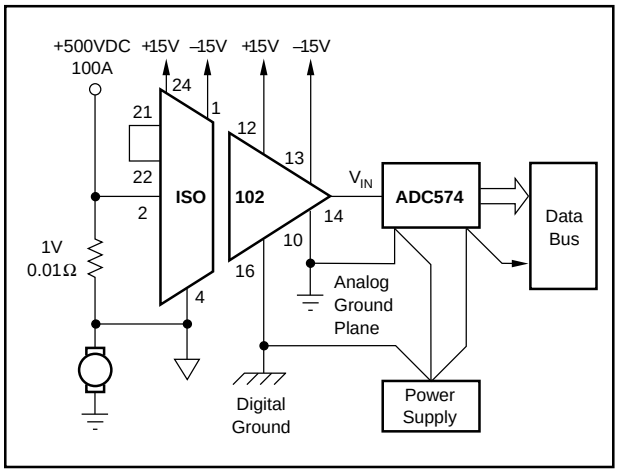


FIGURE 5. Isolated Power Current Monitor for Motor Circuit. (The ISO102 allows reliable, safe measurement at high voltages.)

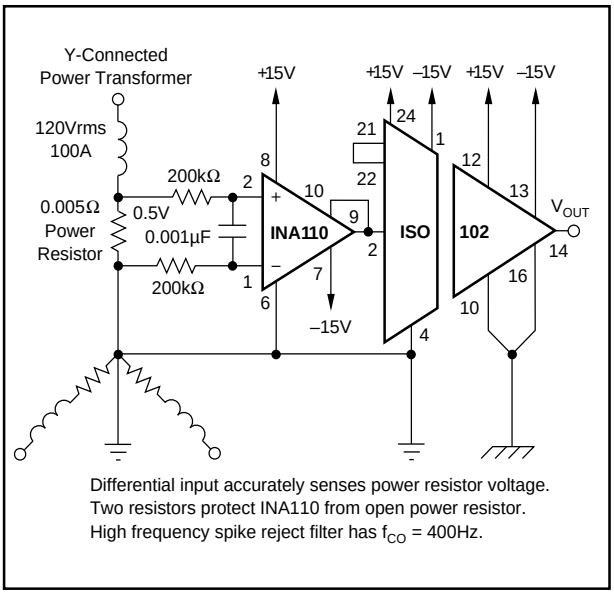


FIGURE 6. Isolated Power Line Monitor (0.5µA leakage current at 120Vrms).

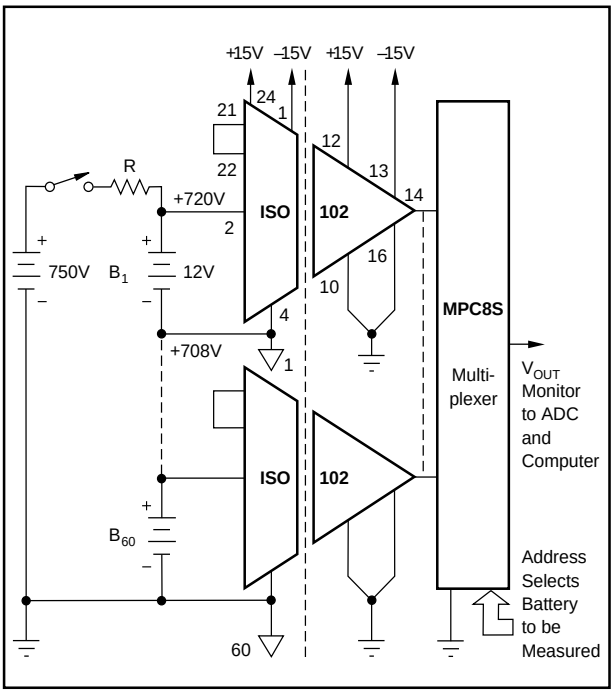


FIGURE 7. Battery Monitor for High Voltage Charging Circuit.

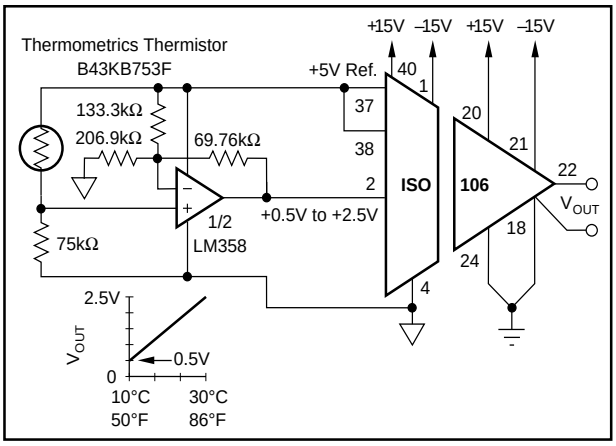


FIGURE 8. Isolated RTD Temperature Amplifier.

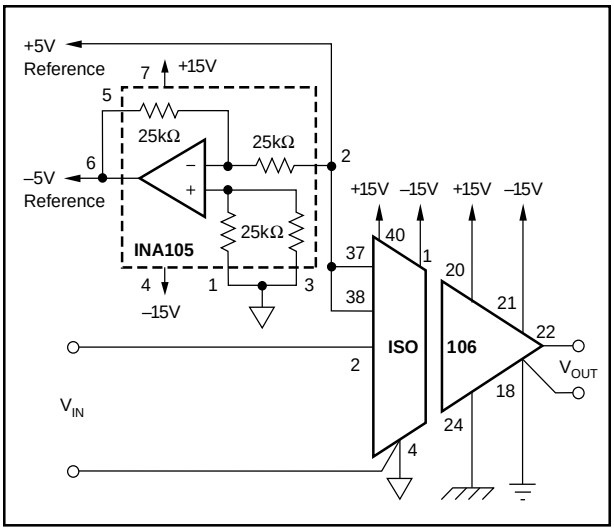


FIGURE 10. Isolation Amplifier with Isolated Bipolar Input Reference.

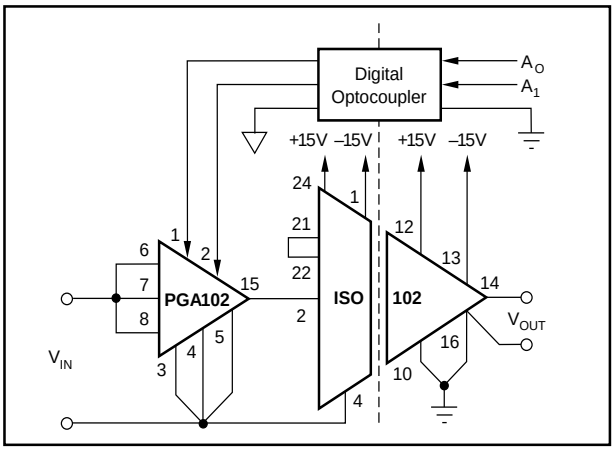


FIGURE 9. Programmable-Gain Isolation Channel with Gains of 1, 10, and 100.

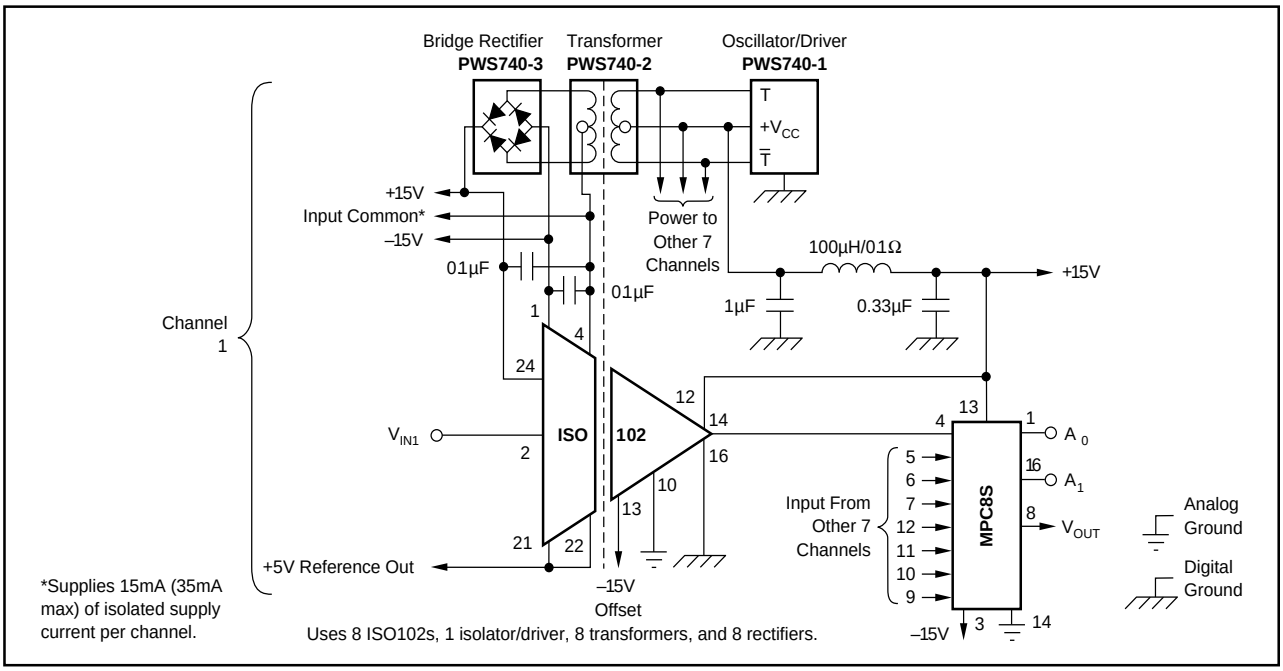


FIGURE 11. Low Cost Eight-Channel Isolation Amplifier Block with Channel-to-Channel Isolation.

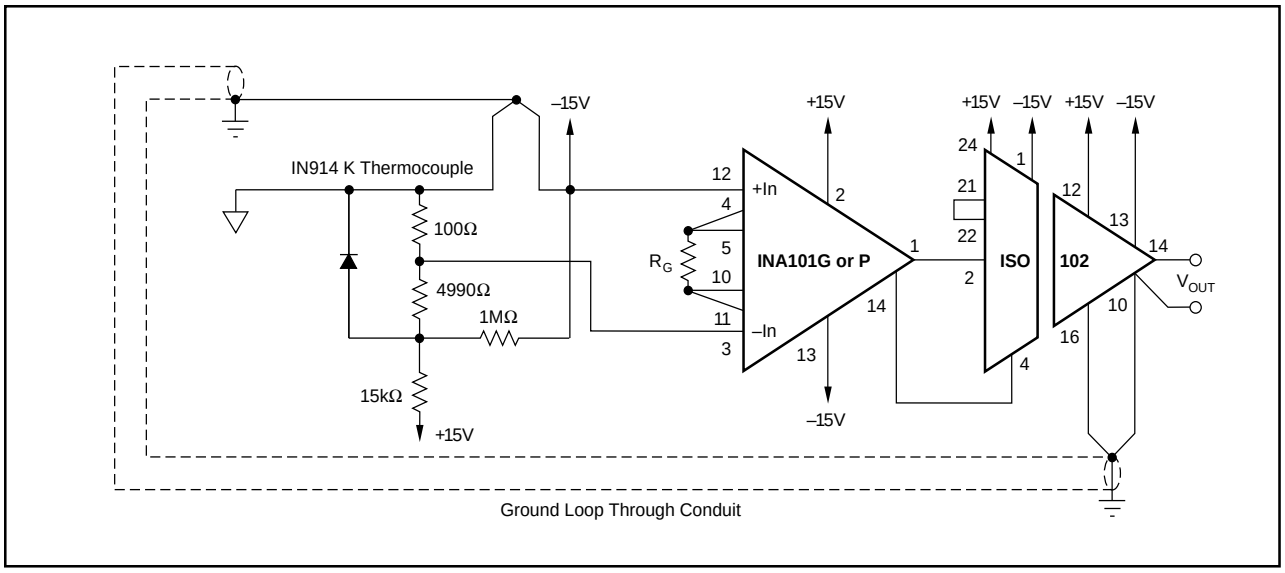


FIGURE 12. Thermocouple Amplifier with Ground Loop Elimination, Cold Junction Compensation, and Upscale Burn-out.

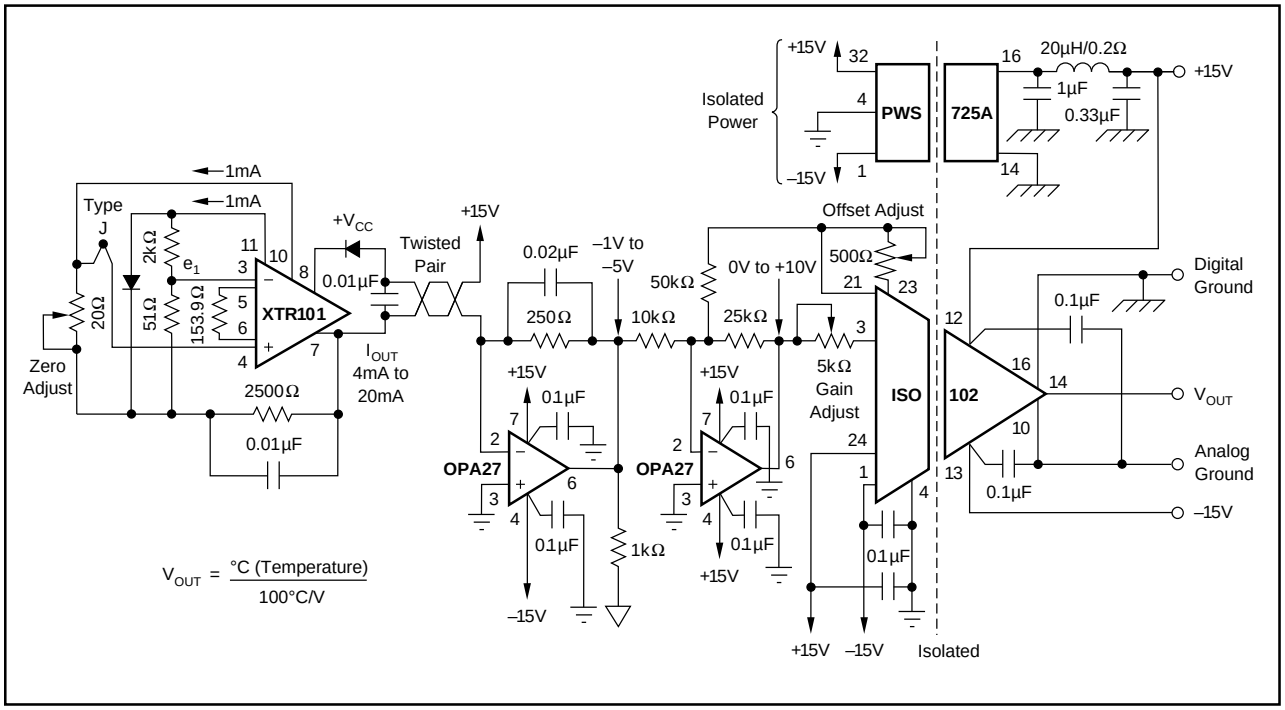


FIGURE 13. Remote Isolated Thermocouple Transmitter with Cold Junction Compensation.

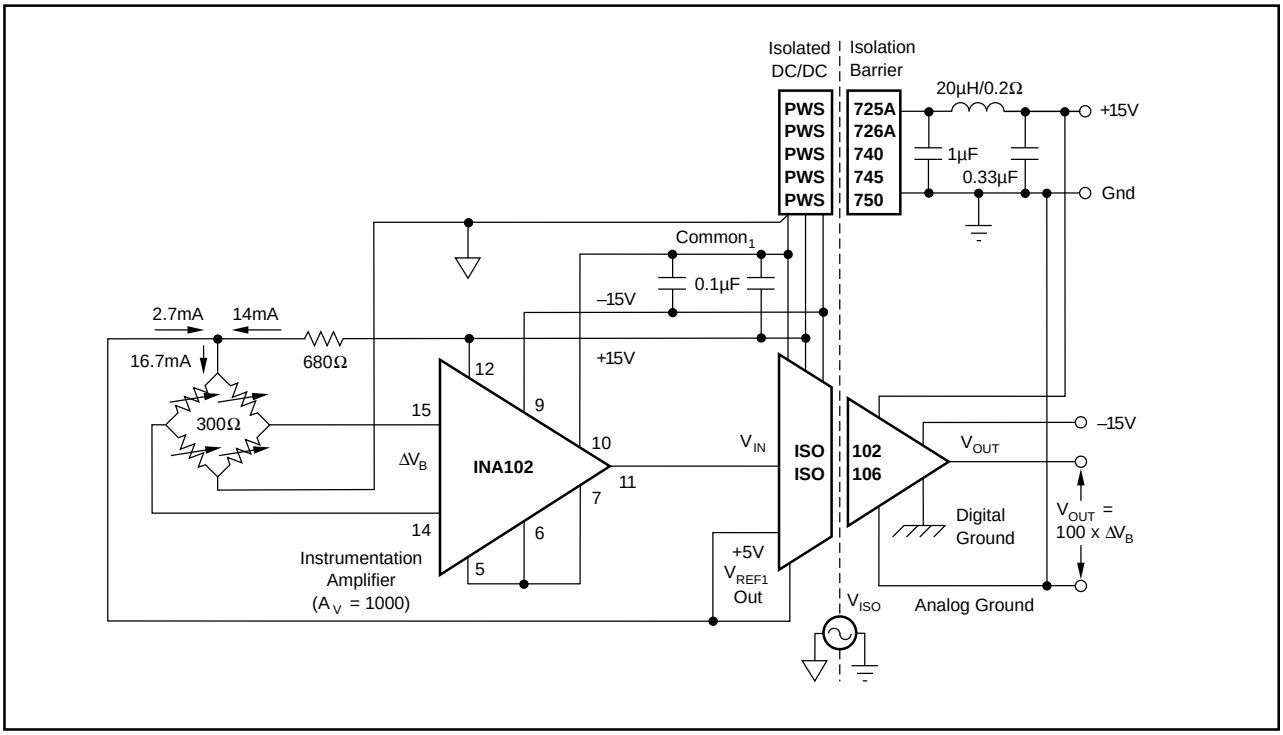


FIGURE 14. Isolated Instrumentation Amplifier for 300Ω Bridge. (Reference voltage from isolation amplifier is used to excite bridge.)

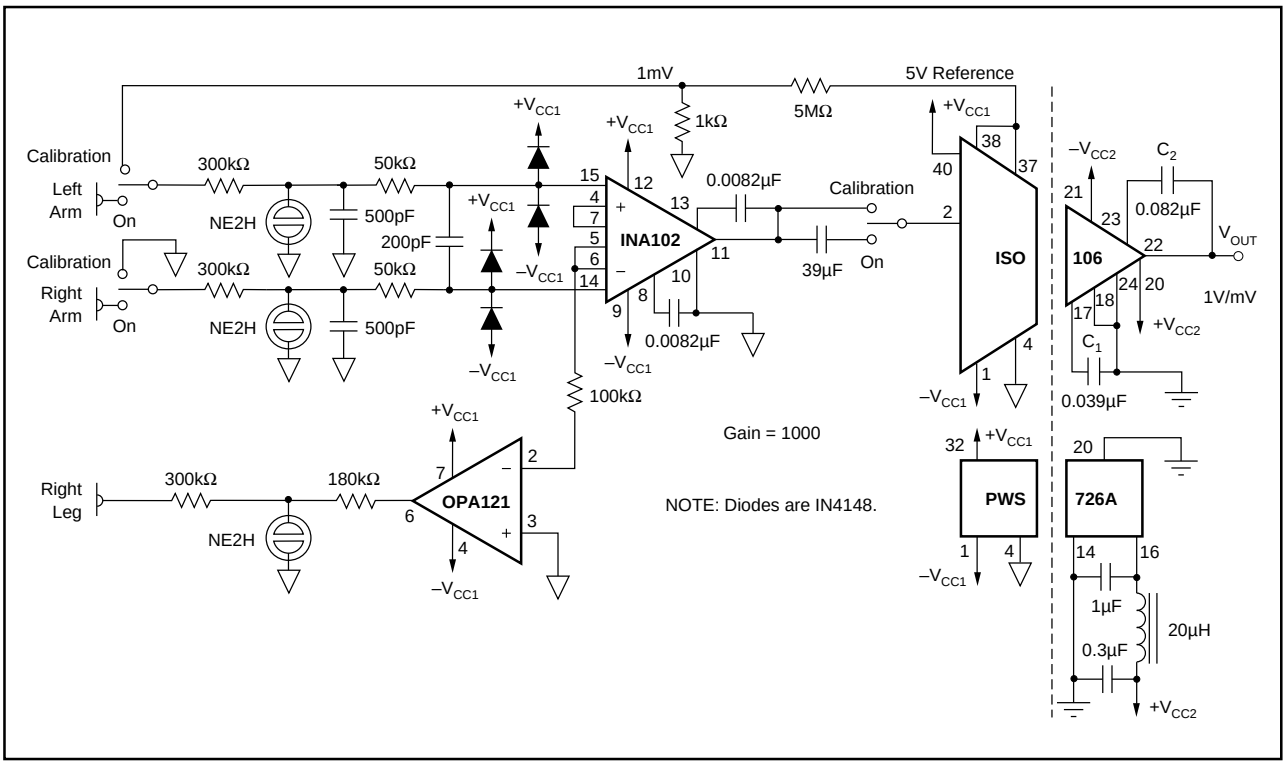


FIGURE 15. Right-Leg-Driven ECG Amplifier (with defibrillator protection and calibrator).

AN ERROR ANALYSIS OF THE IS0102 IN A SMALL SIGNAL MEASURING APPLICATION

High accuracy measurements of low-level signals in the presence of high isolation mode voltages can be difficult due to the errors of the isolation amplifiers themselves.

This error analysis shows that when a low drift operational amplifier is used to preamplify the low-level source signal, a low cost, simple and accurate solution is possible.

In the circuit shown in Figure 16, a 50mV shunt is used to measure the current in a 500VDC motor. The OPA27 amplifies the 50mV by 200 x to 10V full scale. The output of the OPA27 is fed to the input of the IS0102, which is a unity-gain isolation amplifier. The 5kΩ and 1kΩ potentiometers connected to the IS0102 are used to adjust the gain and offset errors to zero as described in Discussion of Specifications.

Some Observations

The total errors of the op amp and the ISO amp combined are approximately 0.11% of full-scale range (see Figure 17). If the op amp had not been used to preamplify the signal, the errors would have been 2.6% of FSR. Clearly, the small cost of adding the op amp buys a large performance improvement. Optimum performance, therefore, is obtained when the full ±10V range of the IS0102/106 is utilized.

The rms noise of the IS0102 with a 120Hz bandwidth is only 0.18mVrms, which is only 0.0018% of the 10V full scale output. Therefore, even though the 16µV/ √Hz noise spectral density specification may appear large compared to other isolation amplifiers, it does not turn out to be a significant error term. It is worth noting that even if the bandwidth is increased to 10kHz, the noise of the iso amp would only contribute 0.016%FSR error.

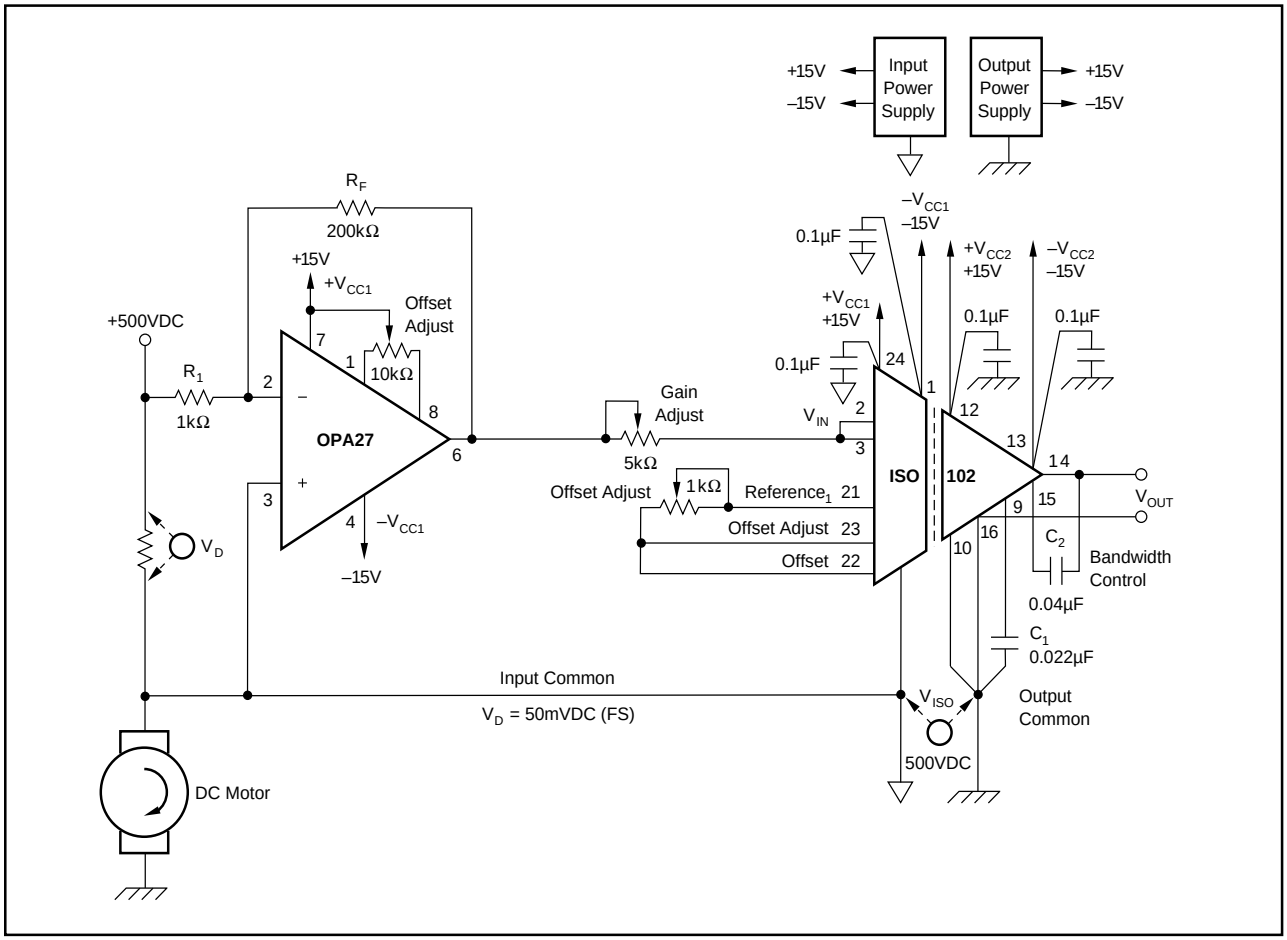


FIGURE 16. 50mV Shunt Measures Current in a 500VDC Motor.

The Errors of the Op Amp at 25°C (Referred to Input, RTI)

$$V_{E\,(OPA)} = V_D \left\{1 - \frac{1}{1 + \frac{1}{\beta A_{VOL}}}\right\} + V_{OS}\,(1 + R_1/R_F) + I_B R_1 + \text{P.S.R.} + \text{Noise}$$

$V_{E\,(OPA)}$ = Total Op Amp Error (RTI)

V_D = Differential Voltage (Full Scale) Across Shunt

$\left\{1 - \frac{1}{1 + \frac{1}{\beta A_{VOL}}}\right\}$ = Gain Error Due to Finite Open Loop Gain

β = Feedback Factor

A_{VOL} = Open Loop Gain at Signal Frequency

V_{OS} = Input Offset Voltage

I_B = Input Bias Current

P.S.R. = Power Supply Rejection (µV/V) [Assuming a 5% change with ±15V supplies. Total error is twice that due to one supply.]

Noise = 5nV/$\sqrt{\text{Hz}}$ (for 1kΩ source resistance and 1kHz bandwidth)

$ERROR_{(OPA)}$ (RTI)		**GAIN ERROR**		**OFFSET**		**P.S.R.**		**NOISE**
$V_{E\,(OPA)}$	=	$50mV\left\{1 - \frac{1}{1 + \frac{1}{10^6/200}}\right\}$		$\{0.025mV\,(1 + 1/200) + 40 \times 10^{-9} \times 10^3\}$		$(20\mu V/V \times 0.75V \times 2)$		$\{5nV\sqrt{120}$ (nVrms)$\}$
	=	0.01mV		(0.0251mV + 0.04mV)	+	0.03mV	+	0.055×10^{-3}mVrms
Error as % of FSR	=	0.02%	+	(0.05% + 0.08%)	+	0.06%	+	0.00011%
After Nulling								
	=	0.01mV	+	(0mV + 0mV)	+	0.03mV	+	0.055×10^{-3}mVrms
	=	0.10mV						
Error as % of FSR*	=	0.02%	+	(0% + 0%)	+	0.06%	+	0.00011%
	=	0.08% of 50mV						

*FSR = Full-Scale Range. 50mV at input to op amp, or 10V at input (and output) of ISO amp.

The Errors of the Iso Amp at 25°C (RTI)

$$V_{E\,(ISO)} = 1/200\,(V_{ISO}/\text{IMR} + V_{OS} + \text{G.E.} + \text{Nonlinearity} + \text{P.S.R.} + \text{Noise})$$

$V_{E\,(ISO)}$ = Total ISO Amp Error

IMR = Isolation Mode Rejection

V_{OS} = Input Offset Voltage

$V_{ISO} = V_{IMV}$ = Isolation Voltage = Isolation Mode Voltage

G.E. = Gain Error (% of FSR)

Nonlinearity = Peak-to-peak deviation of output voltage from best-fit straight line. It is expressed as ratio based on full-scale range.

P.S.R. = Change in V_{OS}/10V x Supply Change

Noise = Spectral noise density x $\sqrt{\text{bandwidth}}$. It is recommended that bandwidth be limited to twice maximum signal bandwidth for optimum dynamic range.

$ERROR_{(ISO)}$ (RTI)		**IMR**		**V_{OS}**		**G.E.**		**NONLINEARITY**		**P.S.R.**		**NOISE**
$V_{E\,(ISO)}$	=	1/200 { 500VDC/140dB	+	70mV	+	20V x 0.25/100	+	0.003/100 x 20V		1.4mV x 0.75V x 2	+	$16\mu V\sqrt{120}$ (rms) }
	=	1/200 { 0.05mV	+	70mV	+	50mV	+	0.6mV	+	2.1mV	+	0.175mVrms }
Error as % of FSR	=	0.0005%	+	0.7%	+	0.5%	+	0.006%	+	0.021%	+	0.00175%
After Nulling												
$V_{E\,(ISO)}$	=	1/200 { 0.05mV	+	0mV	+	0mV	+	0.6mV	+	2.1mV	+	0.175mVrms }
	=	1/200 (3.0mV)										
	=	0.03mV										
Error as % of FSR	=	0.0005%	+	0%	+	0%	+	0.006%	+	0.021%	+	0.00175%
	=	0.03% of 50mV										

Total Error	=	$V_{E\,(OPA)}$	+	$V_{E\,(ISO)}$
	=	0.10mV	+	0.03mV
	=	0.08% of 50mV	+	0.03% of 50mV
	=	0.11% of 50mV		

FIGURE 17. Op Amp and Iso Amp Error Analysis.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ISO102	NRND	CDIP SB	JVE	16	1	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type
ISO102B	NRND	CDIP SB	JVE	16	1	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type
ISO106	NRND	CDIP SB	JVD	16	1	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type
ISO106B	NRND	CDIP SB	JVD	16	1	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

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