

# SPIDER - TLE7234E

8 Channel High-Side and Low-Side Relay Switch

Automotive Power



Never stop thinking

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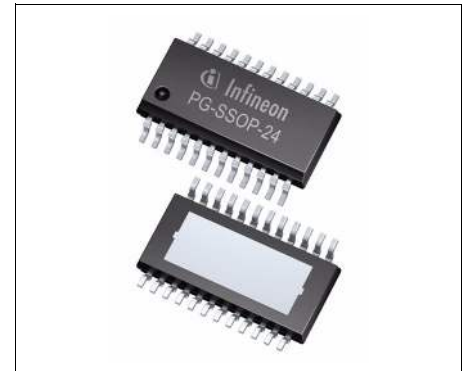
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## 1 Overview

### Features

- 8 bit SPI for diagnostics and control, providing daisy chain capability
- Very wide range for digital supply voltage
- Three configurable input pins offer complete flexibility for PWM operation
- Stable behavior at under voltage
- Green Product (RoHS compliant)
- AEC Qualified



PG-SSOP-24-4

### Description

The TLE7234E is an eight channel high-side and low-side power switch in PG-SSOP-24-4 package providing embedded protective functions. It is especially designed for standard relays and LEDs in automotive applications. The output stages incorporate two low-side, four high-side and two auto configuring high-side or low-side switches.

A serial peripheral interface (SPI) is utilized for control and diagnosis of the device and the load. For direct control, there are three input pins available.

The power transistors are built by N-channel power MOSFETs. The device is monolithically integrated in Smart Power Technology.

Type	Package	Marking
TLE7234E	PG-SSOP-24-4	TLE7234E

**Table 1 Product Summary**

Operating range power supply voltage	$V_{bb}$	5.5 ... 28 V
Digital supply voltage	$V_{DD}$	3.0 ... 5.5 V
Typical On-State resistance at 25 °C	$R_{DS(ON)}$	
high-side: 2 channels (Relay)		0.9 $\Omega$
high-side: 2 channels (Generic, LED)		1.6 $\Omega$
auto configuring: 2 channels (Relay, Supplies)		0.9 $\Omega$
low-side: 2 channels (Relay)		0.9 $\Omega$
Nominal load current (all channels active)	$I_{L(nom, min)}$	
Relay		350 mA
LED, Generic		175 mA
Over load switch off threshold	$I_{DS(OVL, min)}$	500 mA
Output leakage current per channel at 25 °C	$I_{DS(OFF, max)}$	1 $\mu$ A
Drain to source clamping voltage	$V_{DS(CL, min)}$	41 V
Source to ground clamping voltage	$V_{bb(CL, max)}$	-16 V
SPI clock frequency	$f_{SCLK(max)}$	5 MHz

**Protective Functions**

- Over load and short circuit protection
- Thermal shutdown
- Electrostatic discharge protection (ESD)

**Diagnostic Functions**

- Latched diagnostic information via SPI
- Open load detection in OFF-state
- Over load detection in ON-state
- Over temperature

**Applications**

- Especially designed for driving relays and LEDs in automotive applications
- All types of resistive and inductive loads
- Suitable to switch 5 V power supply lines by auto configuring channels

### Detailed Description

The TLE7234E is an eight channel high-side and low-side relay switch providing embedded protective functions. The output stages incorporate two low-side switches ( $0.9\ \Omega$  per channel), four high-side switches (two channels with  $0.9\ \Omega$  and two channels with  $1.6\ \Omega$ ) and two auto-configuring high-side or low-side switches ( $0.9\ \Omega$  per channel). The auto-configuring switches can be utilized in high-side or low-side configuration just by connecting the load accordingly. They are also suitable to switch a 5 V supply line in high-side configuration. Protective and diagnostic functions adjust automatically to the chosen configuration.

The 8 bit serial peripheral interface (SPI) is utilized for control and diagnosis of the device and the loads. The SPI interface provides daisy chain capability in order to assemble multiple devices in one SPI chain by using the same number of micro-controller pins.

Furthermore, the TLE7234E is equipped with three input pins that can be individually routed to the output control of each channel thus offering complete flexibility in design and PCB-layout. The input multiplexer is controlled via SPI.

The device provides full diagnosis of the load via open load, over load and short circuit detection. SPI diagnosis flags indicate latched fault conditions that may have occurred.

Each output stage is protected against short circuit. In case of over load, the affected channel switches off. There are temperature sensors available for each channel to protect the device against over temperature.

The device protects itself with a build in reverse polarity protection which prohibits intrinsic current flow through the logic during reverse polarity. However the output stages still incorporate a reverse diode where current can flow through during reverse polarity.

The power transistors are built by N-channel power MOSFETs. The inputs are ground referenced CMOS compatible. The device is monolithically integrated in Smart Power Technology.

## 2 Block Diagram

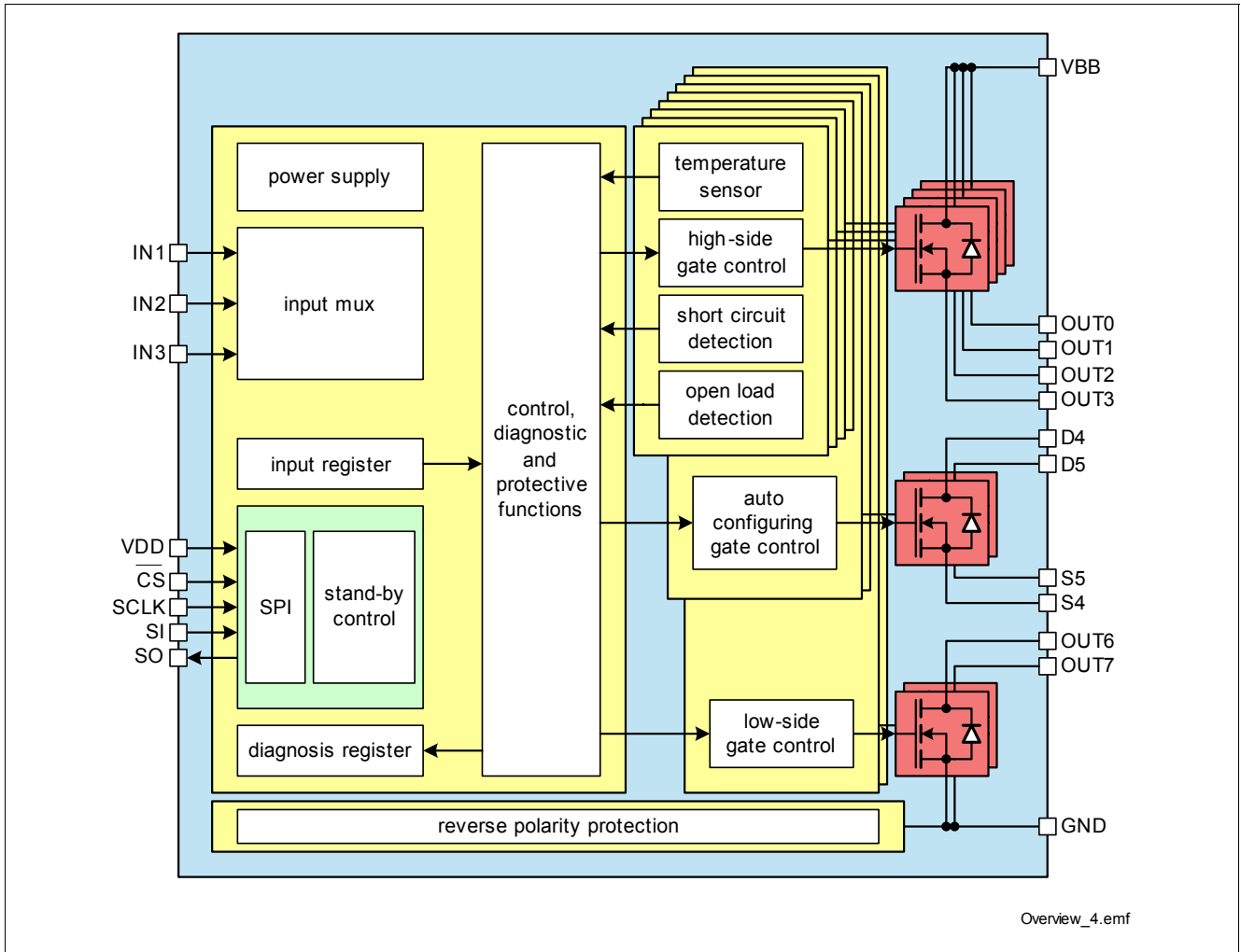


Figure 1 Block Diagram

## 2.1 Terms

Figure 2 shows all terms used in this data sheet.

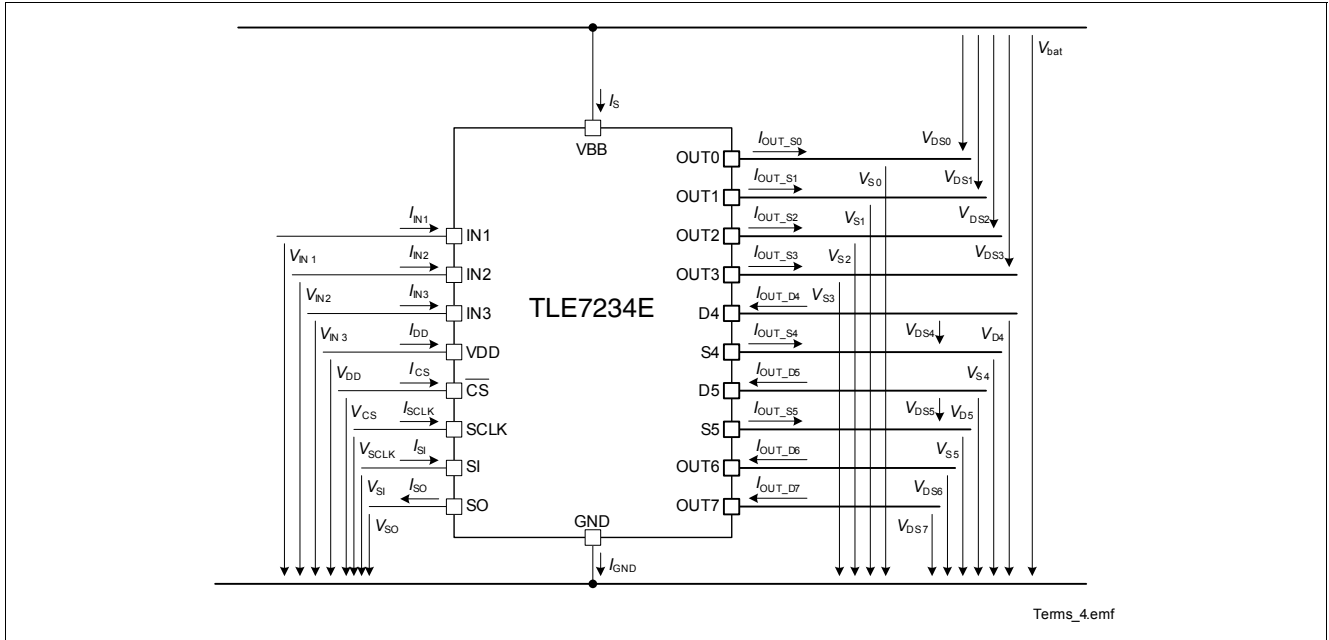


Figure 2 Terms

In all tables of the electrical characteristics is valid:

Channel related symbols without channel number are valid for each channel separately (e.g.  $V_{DS}$  specification is valid for  $V_{DS0} \dots V_{DS7}$ ). In order to make the description of output currents easier, the load current  $I_{Out}$  is equivalent to the drain current  $I_{OUT\_D}$  in low-side configuration and the source current  $I_{OUT\_S}$  in high-side configuration.

All SPI register bits are marked as follows: ADDR.PARAMETER (e.g. ICR01.INX1). In SPI register description, the values in bold letters (e.g. **0**) are default values.

### 3 Pin Configuration

#### 3.1 Pin Assignment

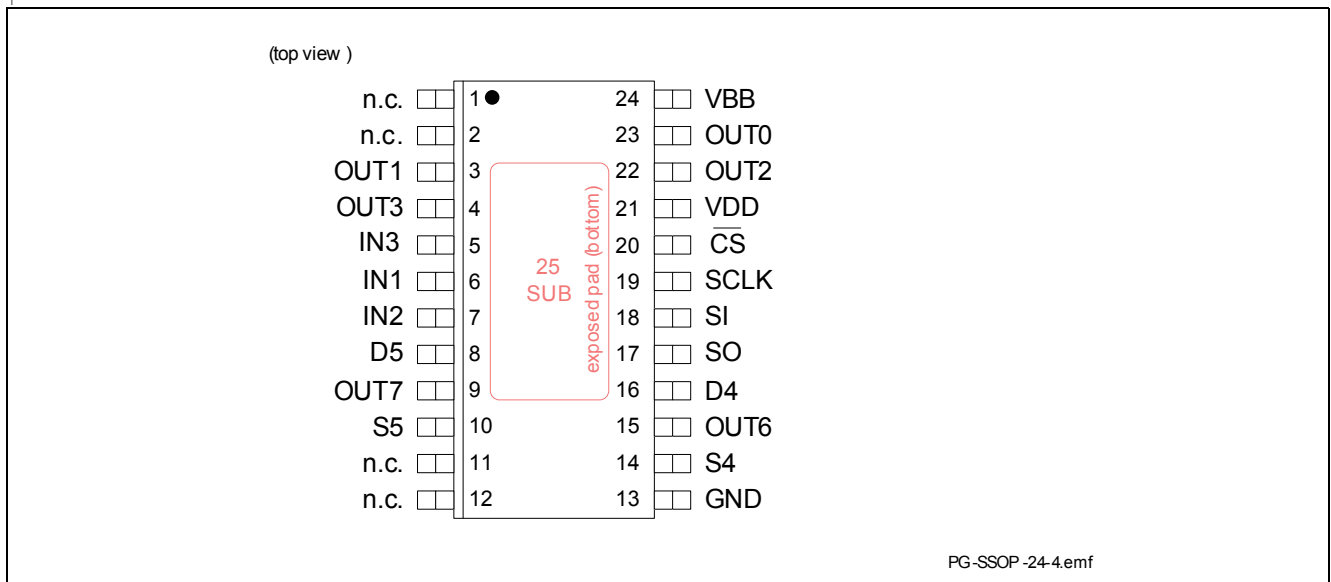


Figure 3 Pin Configuration PG-SSOP24-4

#### 3.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
<b>Power Supply</b>			
21	VDD	-	Digital power supply
24	VBB	-	Power supply
13	GND	-	Digital, analog and power ground
25	SUB	-	Substrate pins for thermal connection. <b>To enable reverse polarity protection these pins must be floating</b>
<b>Power Stages</b>			
23	OUT0	O	Source of high side power transistor channel 0
3	OUT1	O	Source of high side power transistor channel 1
22	OUT2	O	Source of high side power transistor channel 2
4	OUT3	O	Source of high side power transistor channel 3
16	D4	O	Drain of auto configuring power transistor 4
14	S4	O	Source of auto configuring power transistor 4
8	D5	O	Drain of auto configuring power transistor 5
10	S5	O	Source of auto configuring power transistor 5
15	OUT6	O	Drain of low side power transistor channel 6
9	OUT7	O	Drain of low side power transistor channel 7
<b>Inputs</b>			
6	IN1	I	Input multiplexer input 1 pin (pull down)
7	IN2	I	Input multiplexer input 2 pin (pull down)



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**Pin Configuration**

Pin	Symbol	I/O	Function
5	IN3	I	Input multiplexer input 3 pin (pull down)
<b>SPI</b>			
20	$\overline{\text{CS}}$	I	SPI Chip select (pull up)
19	SCLK	I	Serial clock
18	SI	I	Serial data in
17	SO	O	Serial data out
<b>Others</b>			
1,2,11,12	n.c.	I	not connected

## 4 Electrical Characteristics

### 4.1 Absolute Maximum Ratings <sup>1)</sup>

Stresses above the ones listed here may affect device reliability or may cause permanent damage to the device. The values below are not considering combinations of different maximum conditions at one time

$T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Absolute Maximum Ratings <sup>1)</sup>						
Pos.	Parameter	Symbol	Limit Values		Unit	Test Conditions
			min.	max.		
<b>Power Supply</b>						
4.1.1	Power supply voltage	$V_{bb}$	-16	40	V	-16V max. 2 minutes
4.1.2	Digital supply voltage	$V_{DD}$	-0.3	5.5	V	–
4.1.3	Power supply voltage for full short circuit protection (single pulse) ( $T_j = -40\text{ °C} \dots 150\text{ °C}$ )	$V_{bat(SC)}$	0	28	V	–
<b>Power Stages</b>						
4.1.4	Load current channel 0, 1, 4, 5, 6, 7 channel 2, 3	$I_L$	-0.5 -0.25	0.5 0.25	A	–
4.1.5	Voltage at power transistor	$V_{DS}$	–	41	V	–
4.1.6	Power transistor's source voltage	$V_{Out\_S}$	-16	–	V	–
4.1.7	Power transistor's drain voltage	$V_{Out\_D}$	–	41	V	–
4.1.8	Max. energy dissipation one channel single pulse for ch. 0, 1, 4, 5, 6, 7	$E_{AS}$	–	65 50	mJ	<sup>2)</sup> $T_{j(0)} = 105\text{ °C}$ $I_{D(0)} = 0.35\text{ A}$ $T_{j(0)} = 150\text{ °C}$ $I_{D(0)} = 0.250\text{ A}$
4.1.9	Maximum energy dissipation one channel repetitive pulses for ch. 0, 1, 4, 5, 6, 7 $1 \cdot 10^4$ cycles $1 \cdot 10^6$ cycles	$E_{AR}$	–	18 13	mJ	<sup>2)</sup> $T_{j(0)} = 105\text{ °C}$ $I_{D(0)} = 0.250\text{ A}$ $T_{j(0)} = 105\text{ °C}$ $I_{D(0)} = 0.220\text{ A}$
4.1.10	Max. energy dissipation one channel single pulse for ch. 2,3	$E_{AS}$	–	50 30	mJ	<sup>2)</sup> $T_{j(0)} = 105\text{ °C}$ $I_{D(0)} = 0.250\text{ A}$ $T_{j(0)} = 150\text{ °C}$ $I_{D(0)} = 0.250\text{ A}$

1) not subject to production test

**Electrical Characteristics**

$T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

<b>Absolute Maximum Ratings<sup>1)</sup></b>						
Pos.	Parameter	Symbol	Limit Values		Unit	Test Conditions
			min.	max.		
4.1.11	Maximum energy dissipation one channel repetitive pulses for ch. 2,3 $1 \cdot 10^4$ cycles	$E_{AR}$	-	12	mJ	2) $T_{j(0)} = 105\text{ °C}$ $I_{D(0)} = 0.180\text{ A}$
	$1 \cdot 10^6$ cycles		-	11		

**Logic Pins**

4.1.12	Voltage at input pins	$V_{IN}$	-0.3	$V_{DD} + 0.3$	V	3)
4.1.13	Voltage at chip select pin	$V_{CS}$	-0.3	$V_{DD} + 0.3$	V	3)
4.1.14	Voltage at serial clock pin	$V_{SCLK}$	-0.3	$V_{DD} + 0.3$	V	3)
4.1.15	Voltage at serial input pin	$V_{SI}$	-0.3	$V_{DD} + 0.3$	V	3)
4.1.16	Voltage at serial output pin	$V_{SO}$	-0.3	$V_{DD} + 0.3$	V	3)

**Temperatures**

4.1.17	Junction Temperature	$T_j$	-40	150	°C	-
4.1.18	Storage Temperature	$T_{stg}$	-55	150	°C	-

**ESD Susceptibility**

4.1.19	ESD susceptibility on all pins	$V_{ESD}$	-2	2	kV	HBM <sup>4)</sup>
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1) not subject to production test

2) Pulse shape represents inductive switch off:  $I_L(t) = I_L(0) \cdot (1 - t/t_{pulse})$ ;  $0 < t < t_{pulse}$

3)  $V_{DD} + 0.3\text{ V} < 5.5\text{ V}$

4) ESD susceptibility, HBM according to EIA/JESD 22-A114

## 4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply Voltage Range for Nominal Operation	$V_{bb(nom)}$	9	16	V	-
4.2.2	upper Supply Voltage Range for Extended Operation	$V_{bb(ext),up}$	16	28	V	Parameter Deviations possible
4.2.3	lower Supply Voltage Range for Extended Operation	$V_{bb(ext),low}$	5.5	9	V	Parameter Deviations possible
4.2.4	Junction Temperature	$T_j$	-40	150	°C	-

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

## 4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards.

For more information, go to [www.jedec.org](http://www.jedec.org).

Thermal Resistance <sup>1)</sup>							
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case, bottom	$R_{thJC,back}$	–	–	4	K/W	<sup>2)</sup>
4.3.2	Junction to Case, top	$R_{thJC,top}$	–	–	35	K/W	<sup>2)</sup>
4.3.3	Junction to Pin (6,7,18 or 19)	$R_{thJPin}$	–	–	12	K/W	<sup>2)</sup>
4.3.4	Junction to Ambient (1s0p, min. footprint)	$R_{thJA,min}$	–	95	–	K/W	<sup>3)</sup>
4.3.5	Junction to Ambient (1s0p+300mm <sup>2</sup> Cu)	$R_{thJA,300}$	–	50	–	K/W	<sup>4)</sup>
4.3.6	Junction to Ambient (1s0p+600mm <sup>2</sup> Cu)	$R_{thJA,600}$	–	40	–	K/W	<sup>5)</sup>
4.3.7	Junction to Ambient (2s2p)	$R_{thJA,2s2p}$	–	31	–	K/W	<sup>6)</sup>

- 1) Not subject to production test
- 2) Specified  $R_{thJSP}$  value is simulated at natural convection on a cold plate setup (all pins are fixed to ambient temperature).  $T_a = 85\text{ °C}$ . Ch1 to Ch8 are dissipating 1 W power (0.125 W each).
- 3) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-3 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with minimal footprint copper area and 70  $\mu\text{m}$  thickness.  $T_a = 85\text{ °C}$ , Ch1 to Ch8 are dissipating 1 W power (0.125 W each).
- 4) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-3 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional heatspreading copper area of 300mm<sup>2</sup> and 70  $\mu\text{m}$  thickness.  $T_a = 85\text{ °C}$ , Ch1 to Ch8 are dissipating 1 W power (0.125 W each).
- 5) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-3 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional heatspreading copper area of 600mm<sup>2</sup> and 70  $\mu\text{m}$  thickness.  $T_a = 85\text{ °C}$ , Ch1 to Ch8 are dissipating 1 W power (0.125 W each).
- 6) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70  $\mu\text{m}$  Cu, 2 x 35  $\mu\text{m}$  Cu).  $T_a = 85\text{ °C}$ , Ch1 to Ch8 are dissipating 1 W power (0.125 W each).

## 5 Power Supply

The TLE7234E is supplied by two supply voltages  $V_{bb}$  and  $V_{DD}$ . The  $V_{bb}$  supply line is connected to a battery feed and used by the power switches and by an integrated power supply for the register banks. There is an under voltage reset function implemented for the  $V_{bb}$  power supply. After start-up of the power supply, all SPI registers are reset to their default values and the device is in sleep mode (standby). The SPI command `CMD.WAKE = 1` is switching the device to operation mode (ON), while a command `CMD.STB = 1` send the device to sleep mode (standby) again.

The  $V_{DD}$  supply line is used by the SPI shift register related circuitry and for driving the SO line. As a result, the daisy chain function is available as soon as  $V_{DD}$  is provided in the specified range independent of  $V_{bb}$ . A capacitor between pins  $V_{DD}$  and GND is recommended (especially in case of EMI).

The device provides a sleep mode (stand by) to minimize current consumption, which also resets the register banks. It is entered and left by dedicated SPI commands or by turning off the VDD supply.

### 5.1 Reset

There are several reset trigger implemented in the device. A reset switches off all channels and sets the registers to default values. After any kind of reset, the transmission error flag (TER) is set.

#### **Under Voltage Reset:**

During this device condition a read on SPI always delivers the Standard Diagnostic Frame with a TER flag. This under voltage reset is released when all the supply voltages levels are above under voltage threshold.

**Reset Command:** There is a reset command available to reset all register bits of the register bank and the diagnosis registers. As soon as `CMD.RST = 1`, a reset is triggered.

## 5.2 Electrical Characteristics

Unless otherwise specified:

$V_{DD} = 3.0\text{ V to }5.5\text{ V}$ ,  $V_{BAT} = 9.0\text{ V to }16\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
<b>Power Supply <math>V_{bb}</math></b>							
5.2.1	Supply voltage for full operation	$V_{bb}$	9	–	28	V	
5.2.2	Under voltage reset threshold voltage	$V_{bb(UV)}$	–	–	5.5	V	
5.2.3	Operating current	$I_S$	–	–	15	mA	$V_{bb} = 16\text{ V}$
			–	–	12	mA	<sup>1)</sup> $V_{bb} = 16\text{ V}$ all diagnosis off
5.2.4	Sleep mode current with disconnected loads (stand by)	$I_{S(\text{Sleep})}$	–	–	10	$\mu\text{A}$	$V_{bb} = 16\text{ V}$  $AWK = 0$ $T_j = 25\text{ °C}^{1)}$
			–	–	13		$T_j = 85\text{ °C}^{1)}$
			–	–	20		$T_j = 150\text{ °C}$
<b>Digital Power Supply <math>V_{DD}</math></b>							
5.2.5	Logic supply voltage	$V_{DD}$	3.0	–	5.5	V	
5.2.6	Under voltage reset threshold voltage	$V_{DD(PO)}$	–	–	3.0	V	
5.2.7	Logic supply current	$I_{DD}$	–	–	0.2	mA	$f_{SCLK} = 0\text{ Hz}$ $V_{CS} = 0\text{ V}$ $AWK = 1$ $V_{CS} = 0\text{ V}$
5.2.8	Logic supply sleep mode current	$I_{DD(\text{Sleep})}$	–	–	20	$\mu\text{A}$	$V_{CS} = V_{DD}$ $AWK = 0$ $T_j = 25\text{ °C}^{1)}$
			–	–	20		$T_j = 85\text{ °C}^{1)}$
			–	–	40		$T_j = 150\text{ °C}$
<b>Timings</b>							
5.2.9	Sleep mode wake-up time	$t_{wu(\text{Sleep})}$	–	–	200	$\mu\text{s}$	<sup>1)</sup>
5.2.10	$V_{bb}$ under voltage reset delay time	$t_{bb(UVR)}$	–	–	1	$\mu\text{s}$	<sup>1)</sup>
5.2.11	$V_{DD}$ under voltage reset delay time	$t_{DD(UVR)}$	–	–	1	$\mu\text{s}$	<sup>1)</sup>

1) Not subject to production test, specified by design.

*Note: Characteristics show the deviation of parameter at the given supply voltage and junction temperature. Typical values show the typical parameters expected at  $V_{bb} = 13.5\text{ V}$ ,  $V_{DD} = 5.0\text{ V}$ ,  $T_j = 25\text{ °C}$ .*

## 6 Power Stages

The TLE7234E is an eight channel high-side and low-side relay switch. The power stages are built by N-channel vertical power MOSFET transistors. The gates of the high-side switches are controlled by charge pumps.

### 6.1 Input Circuit

There are three input pins available at TLE7234E, which can be configured to be used for control of the output stages. The INXn parameter of the input configuration register provide following possibilities:

- channel is switched off
- channel is switched according to signal level at input pin IN1
- channel is switched according to signal level at input pin IN2 or IN3
- channel is switched on

Figure 4 shows the input circuit of TLE7234E.

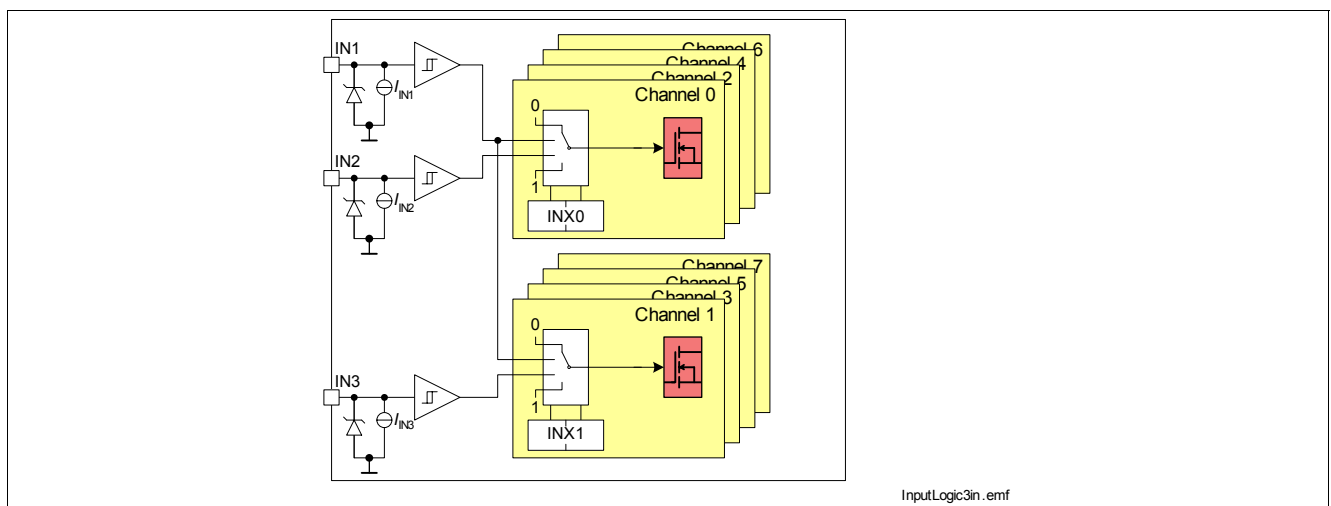


Figure 4 Input Multiplexer

The current sink to ground ensures that the channels switch off in case of open input pin. The zener diode protects the input circuit against ESD pulses.

### 6.2 Channels 4 and 5

The TLE7234E provides two auto-configuring high-side or low-side switches (channels 4 and 5). They adjust the diagnostic and protective functions according their potentials at drain and source automatically.

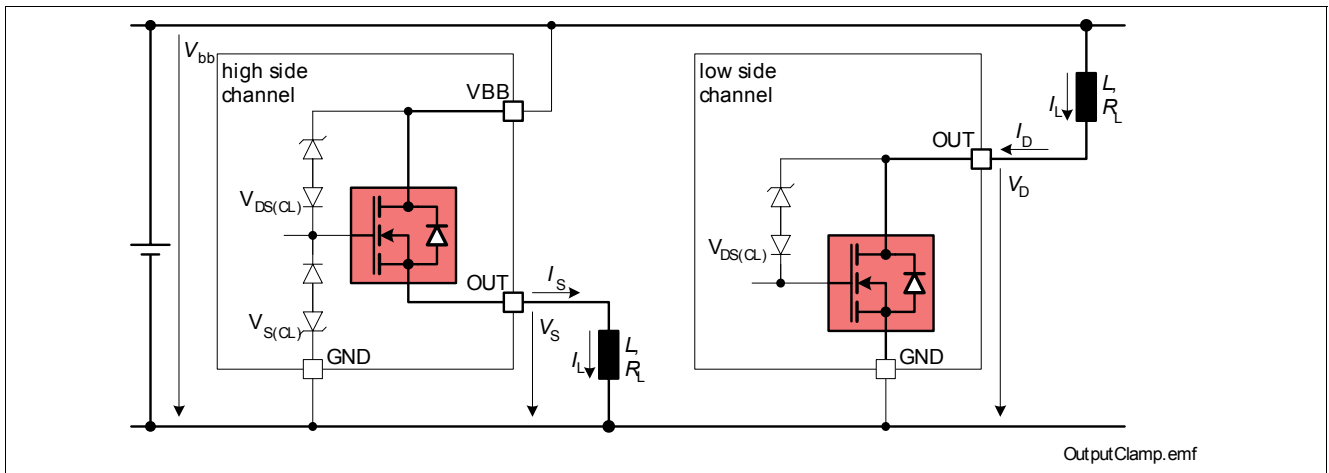
In high-side configuration, the load is connected between ground and source of the power transistors (S4 or S5). The drain of the power transistors (D4 and D5) can be connected to any potential between GND-pin potential and VBB-pin potential. When the drain is connected to VBB, the channel behave like the other high side channels. The drain can also be connected to a 5 V power supply and the source pin will be utilized as switched 5 V supply line.

In low-side configuration, the source of the power transistors are to be connected to GND.

The configuration can be chosen for each of these channels individually, so it is feasible to connect one channel in low-side and the other in high-side configuration.

### 6.3 Inductive Output Clamp

When switching off inductive loads with low-side switches, the potential at pin OUT rises to  $V_{DS(CL)}$  potential, because the inductance intends to continue driving the current. For the high-side channels, the potential at pin OUT drops below ground potential to  $V_{S(CL)}$ . The voltage clamping is necessary to prevent destruction of the device, see **Figure 5** for details. Nevertheless, the maximum allowed load inductance is limited by the max. clamping energy  $E_{AR}$  see electrical characteristics “**E<sub>AR</sub>**” on **Page 10**.



**Figure 5** Output Clamp Implementation

#### Maximum Load Inductance

During demagnetization of inductive loads, energy has to be dissipated in the TLE7234E. This energy can be calculated with following equations:

$$E = V_{D(CL)} \cdot \left[ \frac{V_{bb} - V_{D(CL)}}{R_L} \cdot \ln \left( 1 - \frac{R_L \cdot I_L}{V_{bb} - V_{D(CL)}} \right) + I_L \right] \cdot \frac{L}{R_L} \quad \text{Low-side} \quad (1)$$

$$E = (V_{bb} - V_{S(CL)}) \cdot \left[ \frac{V_{S(CL)}}{R_L} \cdot \ln \left( 1 - \frac{R_L \cdot I_L}{V_{S(CL)}} \right) + I_L \right] \cdot \frac{L}{R_L} \quad \text{High-side} \quad (2)$$

These equations simplify under the assumption of  $R_L = 0$ :

$$E = \frac{1}{2} L I_L^2 \cdot \left( 1 - \frac{V_{bb}}{V_{D(CL)}} \right) \quad \text{Low-side} \quad (3)$$

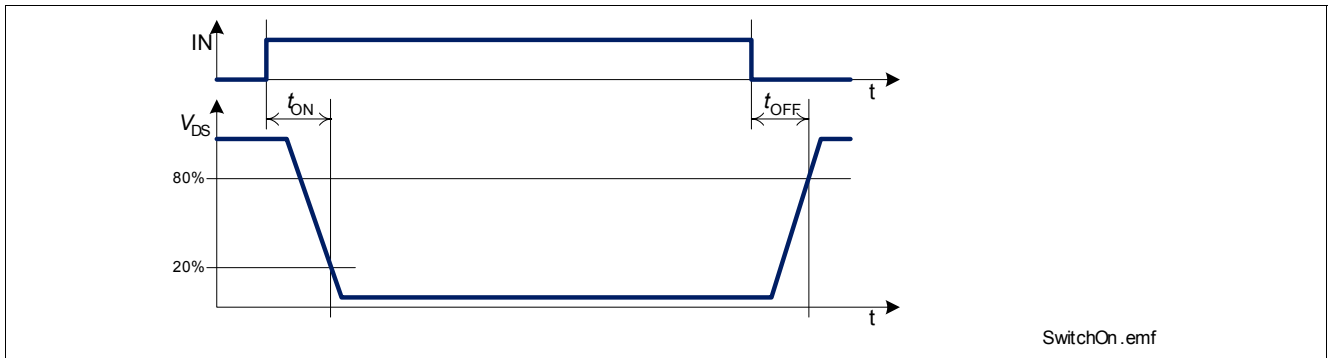
$$E = \frac{1}{2} L I_L^2 \cdot \left( 1 - \frac{V_{bb}}{V_{S(CL)}} \right) \quad \text{High-side} \quad (4)$$

The maximum energy, which is converted into heat, is limited by the thermal design of the component.



### 6.4 Timing Diagrams

The power transistors are switched on and off with a dedicated slope via the  $INX$  bits of the serial peripheral interface (SPI). The switching times  $t_{ON}$  and  $t_{OFF}$  are designed equally.



**Figure 6 Switching a Resistive Load**

In input mode, a high signal at the input pin is equivalent to a SPI ON command and a low signal to SPI OFF command respectively. Please refer to [Section 9.3](#) for details on SPI protocol.

## 6.5 Electrical Characteristics

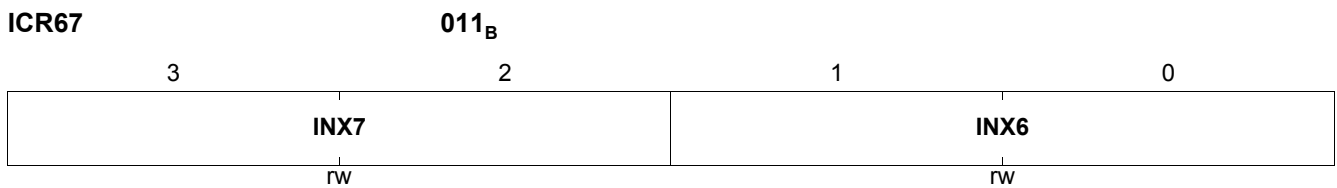
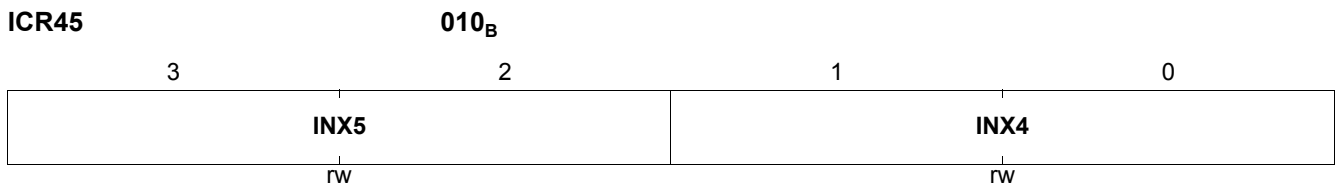
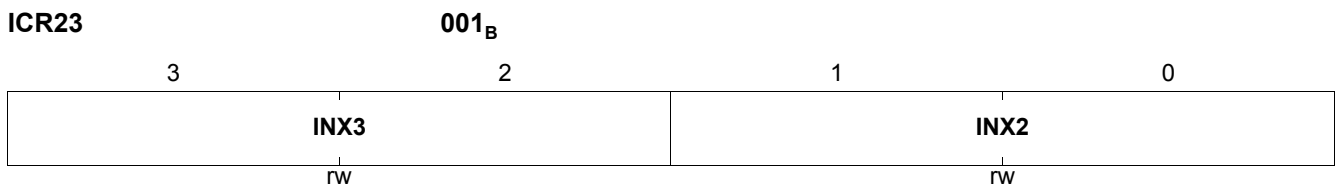
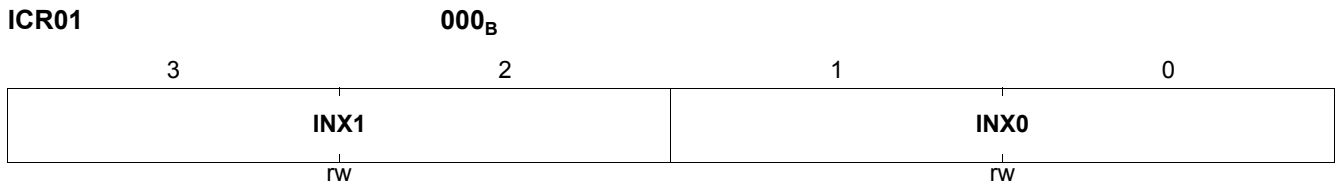
Unless otherwise specified:  $V_{DD} = 3.0\text{ V to }5.5\text{ V}$ ,  $V_{BAT} = 9.0\text{ V to }16\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$   
 typical values:  $V_{DD} = 5.0\text{ V}$ ,  $V_{BAT} = 13.5\text{ V}$ ,  $T_j = 25\text{ °C}$

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
<b>Output Characteristics</b>							
6.5.1	On-State resistance channel 0, 1, 4, 5, 6, 7	$R_{DS(ON)}$	–	0.9	–	$\Omega$	$I_L = 220\text{ mA}$ $T_j = 25\text{ °C}$
			–	1.4	1.9		$T_j = 150\text{ °C}$
	channel 2, 3		–	1.6	–		$I_L = 110\text{ mA}$ $T_j = 25\text{ °C}$
			–	2.6	3.9		$T_j = 150\text{ °C}$
6.5.2	Nominal load current	$I_{Out(nom)}$				mA	all channels on $T_a = 100\text{ °C}$ $T_{j,max} = 150\text{ °C}$ based on $R_{thja}$
	channel 0, 1, 4, 5, 6, 7		350	500	–		1)
	channel 2, 3		175	250	–		1)
6.5.3	Output leakage current in sleep mode	$I_{Out(Sleep)}$	–	–	1	$\mu\text{A}$	$V_{DS} = 13.5\text{ V}$ $T_j = 25\text{ °C}^{1)}$
			–	–	2		$T_j = 85\text{ °C}^{1)}$
			–	–	5		$T_j = 150\text{ °C}$
6.5.4	Output clamping voltage	$V_{OUT\_S(CL)}$	–	–	-16	V	–
		$V_{OUT\_DS(CL)}$	41	–	–	V	–
<b>Input Characteristics</b>							
6.5.5	L level of pin IN	$V_{IN(L)}$	0	–	0.6	V	–
6.5.6	H level of pin IN	$V_{IN(H)}$	1.8	–	5.5	V	–
6.5.7	Input voltage hysteresis at pin IN	$\Delta V_{IN}$	–	0.1	–	V	1)
6.5.8	L-input pull-down current through pin IN	$I_{IN(L)}$	1.5	–	–	$\mu\text{A}$	$V_{IN} = 0.6\text{ V}^{1)}$
6.5.9	H-input pull-down current through pin IN	$I_{IN(H)}$	10	40	80	$\mu\text{A}$	$V_{IN} = 5\text{ V}$
<b>Timings</b>							
6.5.10	Turn-on time $V_{DS} = 20\% V_{bat}$ channel 0, 1,4,5 channel 2, 3 channel 6,7	$t_{ON}$	–	–	100	$\mu\text{s}$	$V_{bb} = 13.5\text{ V}$ resistive load $I_{DS} = 250\text{ mA}$
			–	–	100		$I_{DS} = 120\text{ mA}$
			–	–	100		$I_{DS} = 250\text{ mA}$
6.5.11	Turn-off time $V_{DS} = 80\% V_{bb}$ channel 0, 1, 4, 5 channel 2, 3 (HS) channel 6, 7 (LS)	$t_{OFF}$	–	–	100	$\mu\text{s}$	$V_{bb} = 13.5\text{ V}$ resistive load $I_{DS} = 250\text{ mA}$
			–	–	100		$I_{DS} = 120\text{ mA}$
			–	–	100		$I_{DS} = 250\text{ mA}$

1) Not subject to production test, specified by design.

## 6.6 Command Description

### Input Configuration Registers



Field	Bits	Type	Description
INXn n = 7 to 0	[3:2], [1:0]	rw	<b>Input Multiplexer Configuration Channel n</b> <b>00</b> Channel n is switched off <b>01</b> Channel n is switched by input 1 <b>10</b> Channel n is switched by input 2 or 3 <b>11</b> Channel n is switched on

## 7 Protection Functions

The device provides embedded protective functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

### 7.1 Over Load Protection

The TLE7234E is protected in case of over load or short circuit of the load. After time  $t_{OFF(OVL)}$ , the over loaded channel  $n$  switches off and the according diagnosis flag  $D_n$  is set. The channel can be switched on after clearing the protection latch by command  $CMD.CPL = 1$ . The CPL command clears itself with the next valid SPI communication frame. Please refer to [Figure 7](#) for details.

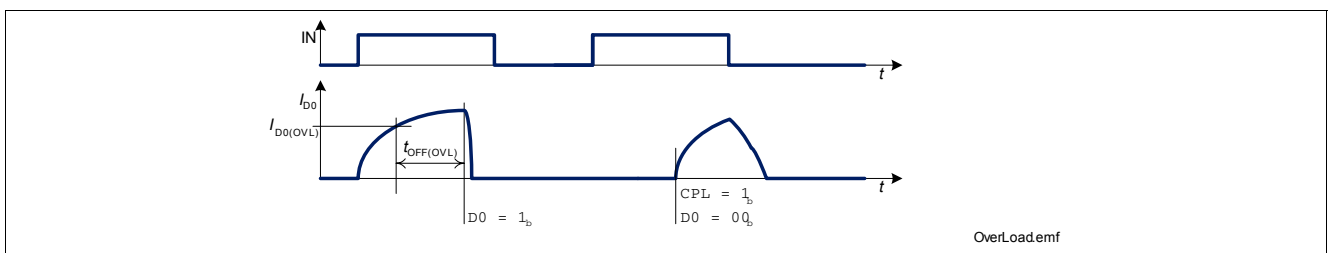


Figure 7 Shut Down at Over Load

### 7.2 Over Temperature Protection

A temperature sensor for each channel causes an overheated channel to switch off to prevent destruction. The according diagnosis flag is set. This flag is also set in OFF state, if the regarding channel temperature is too high. The channel can be only switched on after clearing the protection latch by SPI command  $CMD.CPL = 1$ . The CPL command clears itself with the next valid SPI communication frame. Please refer to [“Diagnostic Features” on Page 22](#) for information on diagnosis features.

### 7.3 ESD protection

There is a designed in protection against ESD disturbances up to the specified limit by using the defined model. Please see electrical characteristics [“ESD susceptibility on all pins” on Page 11](#)

### 7.4 Reverse Polarity Protection

There is a reverse polarity protection implemented in the TLE7234E. This protection has to be divided into two parts. First the protection of the control circuits and second in the protection of the power transistors.

The control circuits are reverse polarity protected by protective measures in the ground connection. In case of reverse polarity, there is no current flow through the control circuits. The digital pins need serial resistors if the connected input stages are not floating to ground.

The power transistors contain intrinsic body diodes that cause power dissipation. The reverse current through these intrinsic body diodes has to be limited by the connected loads. The over temperature and over load protection are not active during reverse polarity.

### 7.5 Loss of $V_{bb}$

In case of loss of  $V_{bb}$  connection in on-state, all inductances of the loads have to be demagnetized through the ground connection or through an additional path from  $V_{bb}$  to ground. Then for example, a diode (see D2 in [Figure 14 “Application Diagram” on Page 34](#)) can be placed.

## 7.6 Electrical Characteristics

Unless otherwise specified:

$V_{DD} = 3.0\text{ V to }5.5\text{ V}$ ,  $V_{BAT} = 9.0\text{ V to }16\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$

typical values:  $V_{DD} = 5.0\text{ V}$ ,  $V_{BAT} = 13.5\text{ V}$ ,  $T_j = 25\text{ °C}$

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
<b>Over Load Protection</b>							
7.6.1	Over load detection current at channel 0,1,4,5,6,7	$I_{Out(OVL)}$	0.5		1.0	A	
7.6.2	Over load detection current at channel 2,3	$I_{Out(OVL)}$	0.22		0.5	A	
7.6.3	Over load shut-down delay time	$t_{OFF(OVL)}$			60	$\mu\text{s}$	
<b>Over Temperature Protection</b>							
7.6.4	Thermal shut down temperature	$T_{j(SC)}$	150	170 <sup>1)</sup>		°C	

1) Not subject to production test, specified by design

## 8 Diagnostic Features

The SPI of TLE7234E provides diagnosis information about the device and about the load. The diagnosis information of the protective functions of channel  $n$  is latched in the diagnosis flags  $D_n$ . It is cleared by the SPI command  $CMD.CPL = 1$ . The CPL command clears itself with the next valid SPI communication frame.

The open load diagnosis of channel  $n$  is latched in the diagnosis flag  $OL_n$ . This flag is cleared by reading the according diagnosis register.

Following table shows possible failure modes and the according protective and diagnostic action.

Failure Mode	Comment
Open Load	<p>Diagnosis, when channel <math>n</math> is switched on: none</p> <p>Diagnosis, when channel <math>n</math> is switched off: according to voltage level at the output pin, flag <math>OL_n</math> is set after time <math>t_{d(OL)}</math>.</p> <p>A diagnosis current can be enabled by SPI command <math>DCCR.DCEN_n = 1</math>.</p>
Over Temperature	<p>When over temperature occurs, the according diagnosis flag <math>D_n</math> is set. If the affected channel <math>n</math> was active it is switched off.</p> <p>The diagnosis flags are latched until they have been cleared by SPI command <math>CMD.CPL = 1</math>.</p>
Over Load (Short Circuit)	<p>When over load is detected at channel <math>n</math>, the affected channel is switched off after time <math>t_{OFF(OVL)}</math> and the dedicated diagnosis flag <math>D_n</math> is set.</p> <p>The diagnosis flags are latched until they have been cleared by SPI command <math>CMD.CPL = 1</math>.</p>

## 8.1 Electrical Characteristics

Unless otherwise specified:

$V_{DD} = 3.0\text{ V to }5.5\text{ V}$ ,  $V_{BAT} = 9.0\text{ V to }16\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$

typical values:  $V_{BAT} = 13.5\text{ V}$ ,  $V_{DD} = 5.0\text{ V}$ ,  $T_j = 25\text{ °C}$

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
<b>OFF State Diagnosis</b>							
8.1.1	Open load diagnosis delay time	$t_{d(OL)}$	100	–	250	μs	–
<b>High Side Channels 0,1,2,3</b>							
8.1.2	Open load detection threshold voltage for Channel 0,1,2,3	$V_{D(OL0..3)}$	2.3	–	3.9	V	<sup>1)</sup>
8.1.3	Output diagnosis current channel 0,1,2,3	$I_{L(DC0..3)}$	50	–	300	μA	measured at $V_{D(OL)}$ threshold
<b>Configurable Channels 4,5</b>							
8.1.4	Open load detection threshold voltage for Channel 4,5 in all configurations	$V_{D(OL4,5)}$	1	–	2.2	V	<sup>1)</sup>
8.1.5	Output diagnosis current channel 4,5 in high side configuration	$I_{L(DCHS)}$	80	–	300	μA	measured at $V_{D(OL)}$ threshold
8.1.6	Output diagnosis current channel 4,5 in low side configuration	$I_{L(DCLS)}$	20	–	100	μA	measured at $V_{D(OL)}$ threshold
<b>Low side Channels 6,7</b>							
8.1.7	Open load detection threshold voltage for Channel 6,7	$V_{D(OL6,7)}$		–	2.2	V	<sup>1)</sup>
8.1.8	Output diagnosis current channel 6,7	$I_{L(DC6,7)}$	50	–	100	μA	measured at VOL threshold
<b>ON State Diagnosis (see also Protection in Chapter 7)</b>							
8.1.9	Over load detection current at channel 0,1,4,5,6,7	$I_{L(OVL)}$	0.5	–	1.0	A	–
8.1.10	Over load detection current at channel 2,3	$I_{L(OVL)}$	0.22	–	0.5	A	–
8.1.11	Over load detection delay time at channel 0,1,4,5,6,7	$t_{OFF(OVL)}$	–	–	60	μs	–

1) Open load detection voltages are referenced to ground

## 8.2 Command Description

Diagnosis Registers (read only, register bank RB = 1)

**DR01** **00<sub>B</sub>**

3	2	1	0
<b>OL1</b>	<b>D1</b>	<b>OL0</b>	<b>D0</b>
r	r	r	r

**DR23** **01<sub>B</sub>**

3	2	1	0
<b>OL3</b>	<b>D3</b>	<b>OL2</b>	<b>D2</b>
r	r	r	r

**DR45** **10<sub>B</sub>**

3	2	1	0
<b>OL5</b>	<b>D5</b>	<b>OL4</b>	<b>D4</b>
r	r	r	r

**DR67** **11<sub>B</sub>**

3	2	1	0
<b>OL7</b>	<b>D7</b>	<b>OL6</b>	<b>D6</b>
r	r	r	r

Field	Bits	Type	Description
Dn n = 7 to 0	2, 0	r	<b>Diagnostic Feedback of Channel n</b> 0 normal operation 1 over load or over temperature switch off occurred
OLn n = 7 to 0	3, 1	r	<b>Open Load Detection of Channel n</b> 0 normal operation 1 Open load at OFF-state occurred

**CMD**

**Command Register** **110<sub>B</sub>**

3	2	1	0
<b>Wake</b>	<b>STB</b>	<b>RST</b>	<b>CPL</b>
r/w	r/w	r/w	r/w

Field	Bits	Type	Description
CPL	0	r/w	please refer to <a href="#">Section 7</a> for description
RST	1	r/w	please refer to <a href="#">Section 5.1</a> for description
STB	2	r/w	please refer to <a href="#">Section 5</a> for description
Wake	3	r/w	please refer to <a href="#">Section 5</a> for description



**Diagnosis Current Configuration Register**

**DCCR0** **100<sub>B</sub>**

3	2	1	0
<b>DCEN3</b>	<b>DCEN2</b>	<b>DCEN1</b>	<b>DCEN0</b>
r/w	r/w	r/w	r/w

**DCCR1** **101<sub>B</sub>**

3	2	1	0
<b>DCEN7</b>	<b>DCEN6</b>	<b>DCEN5</b>	<b>DCEN5</b>
r/w	r/w	r/w	r/w

Field	Bits	Type	Description
DCENn n = 7 to 0	3 to 0	r/w	<b>Diagnosis Current Enable Channel n</b> <b>0</b> Diagnosis current disabled <b>1</b> Diagnosis current enabled

## 9 Serial Peripheral Interface (SPI)

The diagnosis and control interface is based on a serial peripheral interface (SPI).

The SPI is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and  $\overline{CS}$ . Data is transferred by the lines SI and SO at the data rate given by SCLK. The falling edge of  $\overline{CS}$  indicates the beginning of a data access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of  $\overline{CS}$ . A modulo 8 counter ensures that data is taken only, when a multiple of 8 bit has been transferred. The interface provides daisy chain capability.

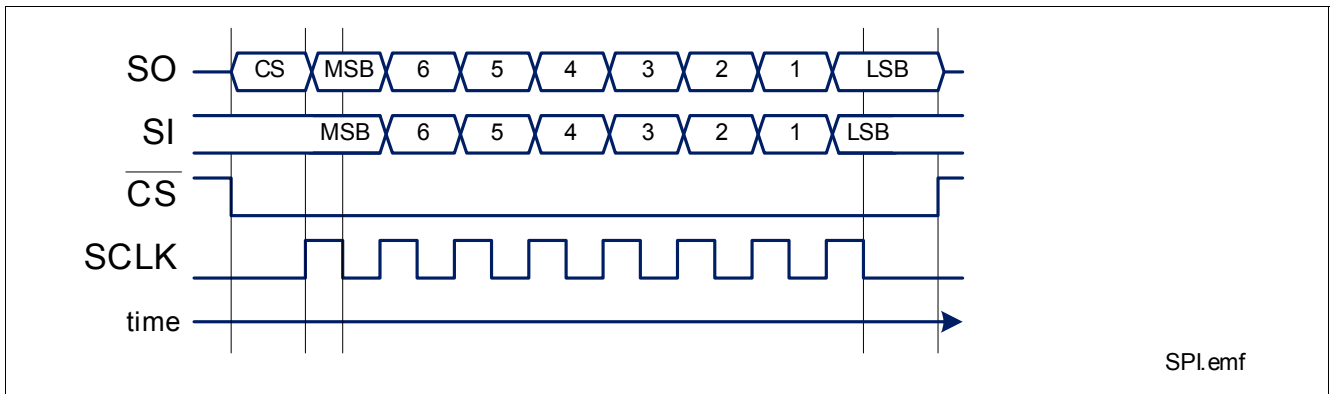


Figure 8 Serial Peripheral Interface

The SPI protocol is described in [Section 9.3](#). It is reset to the default values after reset.

### 9.1 SPI Signal Description

**$\overline{CS}$  - Chip Select:** The system micro controller selects the TLE7234E by means of the  $\overline{CS}$  pin. Whenever the pin is in low state, data transfer can take place. When  $\overline{CS}$  is in high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

**$\overline{CS}$  High to Low transition:**

- The diagnosis information is transferred into the shift register.
- SO changes from high impedance state to high or low state depending on the logic OR combination between the transmission error flag (TER) and the signal level at pin SI. As a result, even in daisy chain configuration, a high signal indicates a faulty transmission. For details, please refer to [Figure 9](#). This information stays available to the first rising edge of SCLK.

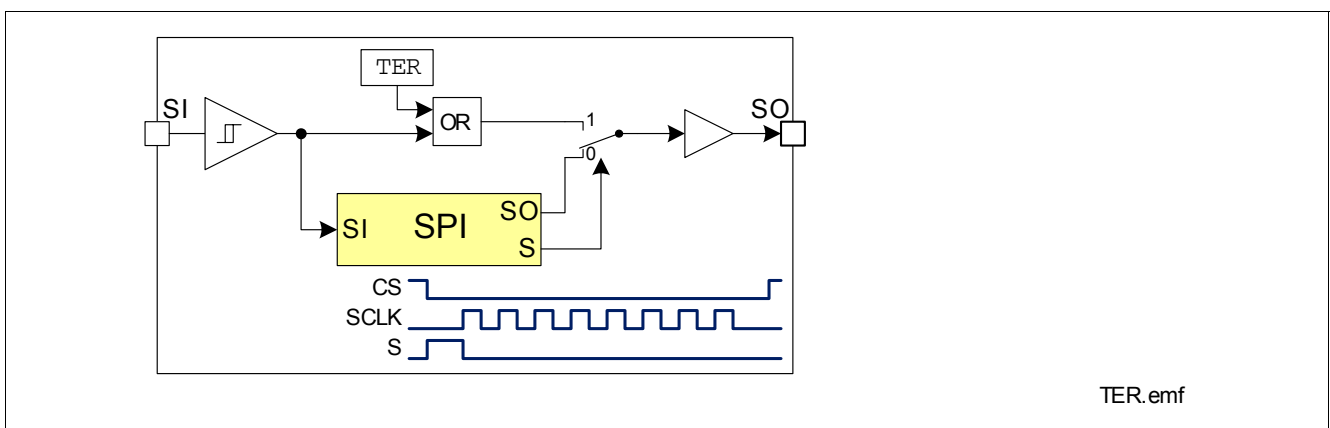


Figure 9 Transmission Error Flag on SO Line

**$\overline{CS}$  Low to High transition:** 

- Command decoding is only done, when after the falling edge of  $\overline{CS}$  exactly a multiple (1, 2, 3, ...) of eight SCLK signals have been detected. In case of faulty transmission, the transmission error flag ( $TER$ ) is set and the command is ignored.
- Data from shift register is transferred into the input matrix register.

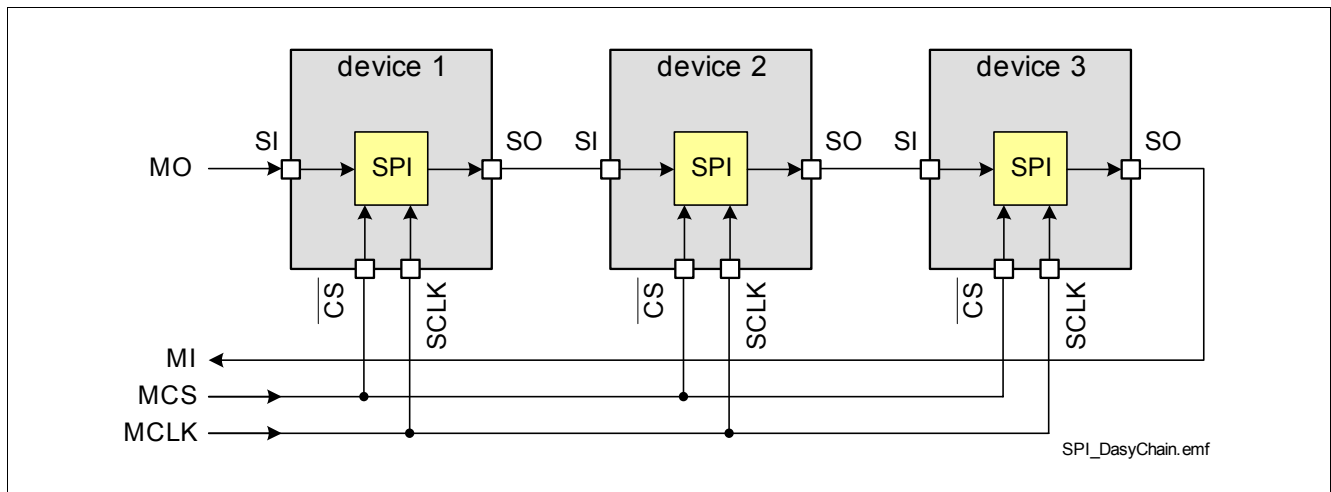
**SCLK - Serial Clock:** This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in low state whenever chip select  $\overline{CS}$  makes any transition.

**SI - Serial Input:** Serial input data bits are shifted in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. The 8 bit input data consist of two parts (control and data). Please refer to [Section 9.3](#) for further information.

**SO Serial Output:** Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the  $\overline{CS}$  pin goes to low state. New data will appear at the SO pin following the rising edge of SCLK. Please refer to [Section 9.3](#) for further information.

## 9.2 Daisy Chain Capability

The SPI of TLE7234E provides daisy chain capability. In this configuration several devices are activated by the same  $\overline{CS}$  signal  $\overline{MCS}$ . The SI line of one device is connected with the SO line of another device (see [Figure 10](#)), which builds a chain. The ends of the chain are connected with the output and input of the master device, MO and MI respectively. The master device provides the master clock MCLK, which is connected to the SCLK line of each device in the chain.



**Figure 10** Daisy Chain Configuration

In the SPI block of each device, there is one shift register where one bit from SI line is shifted in each SCLK. The bit shifted out can be seen at SO. After 8 SCLK cycles, the data transfer for one device has been finished. In single chip configuration, the  $\overline{CS}$  line must go high to make the device accept the transferred data. In daisy chain configuration the data shifted out at device #1 has been shifted in to device #2. When using three devices in daisy chain, three times 8 bits have to be shifted through the devices. After that, the  $\overline{MCS}$  line must go high (see [Figure 11](#)).

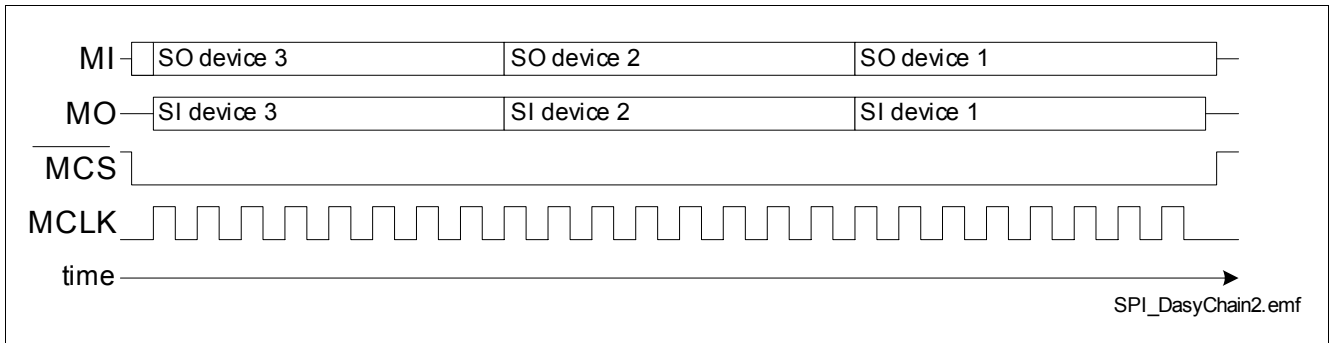


Figure 11 Data Transfer in Daisy Chain Configuration

### 9.3 SPI Protocol

The control and diagnosis function of the TLE7234E is based on two register banks which are accessed via following SPI protocol. The control register bank contains eight registers (with 4 bit each) addressed by a 3 bit pointer. The diagnosis register bank contains four registers (with 4 bit each) addressed by a 2 bit pointer. An additional indication bit is available to differentiate between standard diagnosis information and data read from a register bank.

#### Control and Diagnosis Mode

	CS <sup>1)</sup>	7	6	5	4	3	2	1	0
Write Register Command									
SI		1	ADDR			DATA			
Read Register Command									
SI		0	ADDR			x	x	0	RB
Read Standard Diagnosis									
SI		0	x	x	x	x	x	1	x
Standard Diagnosis									
SO	TER	0	0	AWK	0	D67	D45	D23	D01
Second Frame of Read Command									
SO	TER	0	1	ADDR (Diagnosis)			DATA		
SO	TER	1	ADDR (Control)			DATA			

1) This bit is valid between CS hi -> lo and first SCLK lo -> hi transition.

*Note: Reading a register needs two SPI frames. In the first frame the RD command is sent. In the second frame, the output at SPI signal SO will contain the requested information. Any command can be executed in the second frame.*

Field	Bits	Type	Description
<b>TER</b>			<b>Transmission Error</b> 0 Previous transmission was successful (modulo 8 clocks received) 1 Previous transmission failed or first transmission after reset
<b>RB</b>	0		<b>Register Bank</b> 0 CONTR Control Register Bank 1 DIAG Diagnosis Register Bank (read only)
<b>ADDR</b>	6:4		<b>Address</b> Pointer to register for read and write command
<b>DATA</b>	3:0		<b>Data</b> Data written to or read from register selected by address ADDR

**Standard Diagnosis:**

Field	Bits	Type	Description
<b>AWK</b>	5		<b>Awake, Device active</b>
<b>Dxy</b>	3, 2, 1, 0		<b>Failure mode alert of channel x and y</b>

## 9.4 Register Overview

**Control Register Bank**

Name	Addr	3	2	1	0	default <sup>1)</sup>	type
ICR01	000 <sub>B</sub>	INX1		INX0		0 <sub>H</sub>	r/w
ICR23	001 <sub>B</sub>	INX3		INX2		0 <sub>H</sub>	r/w
ICR45	010 <sub>B</sub>	INX5		INX4		0 <sub>H</sub>	r/w
ICR67	011 <sub>B</sub>	INX7		INX6		0 <sub>H</sub>	r/w
DCCR0	100 <sub>B</sub>	DCEN3	DCEN2	DCEN1	DCEN0	0 <sub>H</sub>	r/w
DCCR1	101 <sub>B</sub>	DCEN7	DCEN6	DCEN5	DCEN4	0 <sub>H</sub>	r/w
CMD	110 <sub>B</sub>	WAKE	STB	RST	CPL <sup>2)</sup>	0 <sub>H</sub>	w
unused	111 <sub>B</sub>	–	–	–	–	0 <sub>H</sub>	–

1) The default values are set after  $V_{bb}$  power-on, STB-command and RST-command  
All command bits are cleared at the end of transmission, respectively after execution

2) CPL bit needs a valid next SPI communication frame to be cleared

Diagnosis Register Bank (read only)

Name	Addr	3	2	1	0
DR01	000 <sub>B</sub>	OL1	D1	OL0	D0
DR23	001 <sub>B</sub>	OL3	D3	OL2	D2
DR45	010 <sub>B</sub>	OL5	D5	OL4	D4
DR67	011 <sub>B</sub>	OL7	D7	OL6	D6

9.5 Timing Diagrams

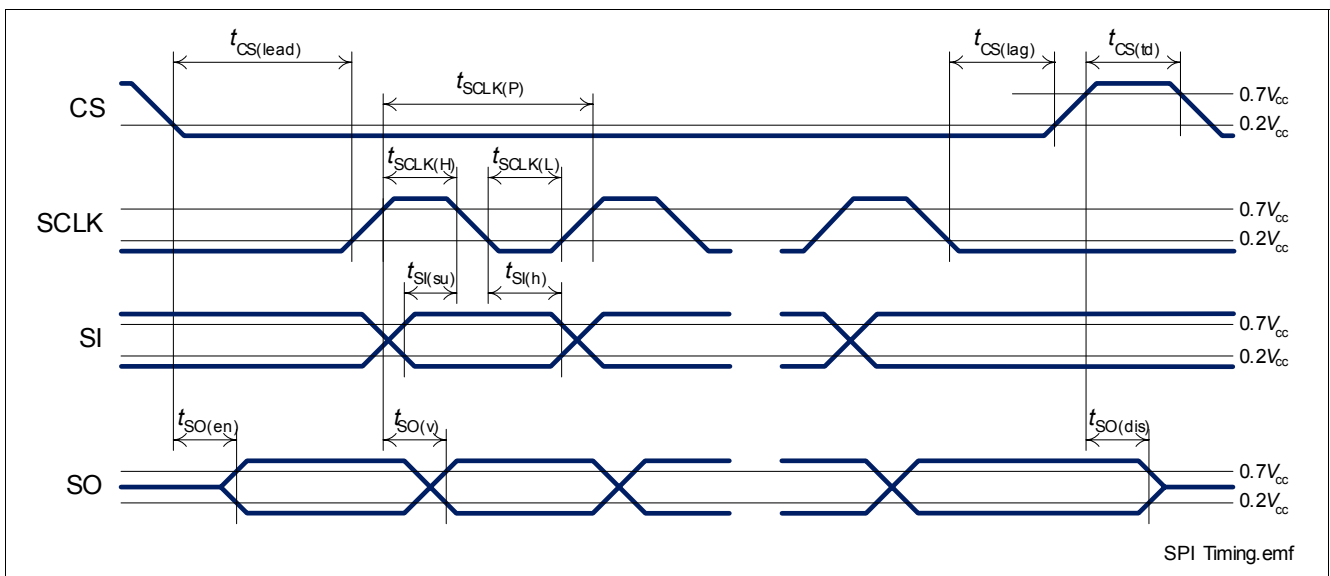


Figure 12 Timing Diagram

## 9.6 Electrical Characteristics

Unless otherwise specified:  $V_{DD} = 3.0\text{ V to }5.5\text{ V}$ ,  $V_{BAT} = 9.0\text{ V to }16\text{ V}$ ,  $T_j = -40\text{ }^\circ\text{C to }+150\text{ }^\circ\text{C}$   
 typical values:  $V_{DD} = 5.0\text{ V}$ ,  $V_{BAT} = 13.5\text{ V}$ ,  $T_j = 25\text{ }^\circ\text{C}$

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
<b>Input Characteristics (CS, SCLK, SI)</b>							
9.6.1	L level of pin $\overline{\text{CS}}$ SCLK SI	$V_{\text{CS(L)}}$ $V_{\text{SCLK(L)}}$ $V_{\text{SI(L)}}$	0	–	$0.2 \cdot V_{DD}$	V	–
9.6.2	H level of pin $\overline{\text{CS}}$ SCLK SI	$V_{\text{CS(H)}}$ $V_{\text{SCLK(H)}}$ $V_{\text{SI(H)}}$	$0.5 \cdot V_{DD}$	–	$V_{DD}$	V	–
9.6.3	L-input pull-up current through $\overline{\text{CS}}$	$I_{\text{CS(L)}}$	5	40	90	$\mu\text{A}$	$V_{\text{CS}} = 0\text{ V}$ $V_{DD} = 5\text{ V}$
9.6.4	H-input pull-up current through $\overline{\text{CS}}$	$I_{\text{CS(H)}}$	2.5	–	–	$\mu\text{A}$	<sup>1)</sup> $V_{DD} = 5\text{ V}$ $V_{\text{CS}} = 0.5 \cdot V_{DD}$
9.6.5	L-input pull-down current through pin SCLK SI	$I_{\text{SCLK(L)}}$ $I_{\text{SI(L)}}$	1.5	–	–	$\mu\text{A}$	<sup>1)</sup> $V_{DD} = 5\text{ V}$ $V_{\text{SCLK}} = V_{\text{SI}} = 0.2 \cdot V_{DD}$
9.6.6	H-input pull-down current through pin SCLK SI	$I_{\text{SCLK(H)}}$ $I_{\text{SI(H)}}$	10	40	80	$\mu\text{A}$	<sup>1)</sup> $V_{DD} = 5\text{ V}$ $V_{\text{SCLK}} = V_{\text{SI}} = V_{DD}$
<b>Output Characteristics (SO)</b>							
9.6.7	L level output voltage	$V_{\text{SO(L)}}$	0	–	0.4	V	$I_{\text{SO}} = +2\text{ mA}$
9.6.8	H level output voltage	$V_{\text{SO(H)}}$	$V_{DD} - 0.4\text{ V}$	–	$V_{DD}$		$I_{\text{SO}} = -1.5\text{ mA}$
9.6.9	Output tristate leakage current	$I_{\text{SO(OFF)}}$	-10	–	10	$\mu\text{A}$	$V_{\text{CS}} = V_{DD}$
<b>Timings</b>							
9.6.10	Serial clock frequency	$f_{\text{SCLK}}$	0	–	5	MHz	–
9.6.11	Serial clock period	$t_{\text{SCLK(P)}}$	200	–	–	ns	–
9.6.12	Serial clock high time	$t_{\text{SCLK(H)}}$	50	–	–	ns	<sup>1)</sup>
9.6.13	Serial clock low time	$t_{\text{SCLK(L)}}$	50	–	–	ns	<sup>1)</sup>
9.6.14	Enable lead time (falling $\overline{\text{CS}}$ to rising SCLK)	$t_{\text{CS(lead)}}$	250	–	–	ns	<sup>1)</sup>
9.6.15	Enable lag time (falling SCLK to rising $\overline{\text{CS}}$ )	$t_{\text{CS(lag)}}$	250	–	–	ns	<sup>1)</sup>
9.6.16	Transfer delay time (rising $\overline{\text{CS}}$ to falling $\overline{\text{CS}}$ )	$t_{\text{CS(td)}}$	250	–	–	ns	<sup>1)</sup>
9.6.17	Data setup time (required time SI to falling SCLK)	$t_{\text{SI(su)}}$	20	–	–	ns	<sup>1)</sup>
9.6.18	Data hold time (falling SCLK to SI)	$t_{\text{SI(h)}}$	20	–	–	ns	<sup>1)</sup>

**Serial Peripheral Interface (SPI)**

Unless otherwise specified:  $V_{DD} = 3.0\text{ V to }5.5\text{ V}$ ,  $V_{BAT} = 9.0\text{ V to }16\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$   
 typical values:  $V_{DD} = 5.0\text{ V}$ ,  $V_{BAT} = 13.5\text{ V}$ ,  $T_j = 25\text{ °C}$

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
9.6.19	Output enable time (falling $\overline{\text{CS}}$ to SO valid)	$t_{\text{SO(en)}}$	–	–	200	ns	$C_L = 20\text{ pF}^{1)}$
9.6.20	Output disable time (rising $\overline{\text{CS}}$ to SO tri-state)	$t_{\text{SO(dis)}}$	–	–	200	ns	$C_L = 20\text{ pF}^{1)}$
9.6.21	Output data valid time with capacitive load	$t_{\text{SO(v)}}$	–	–	100	ns	$C_L = 20\text{ pF}^{1)}$

1) Not subject to production test, specified by design.



10 Package Outlines

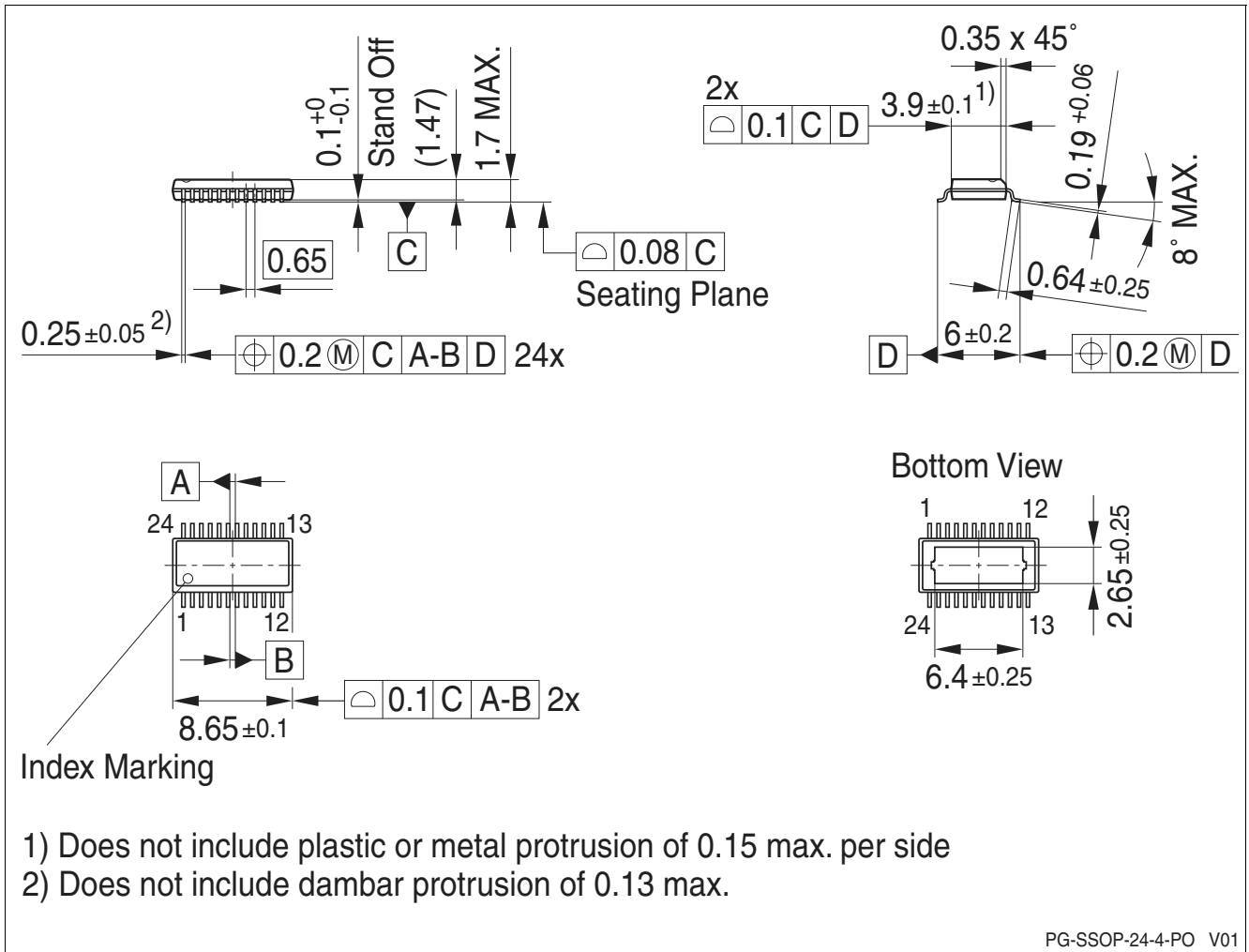


Figure 13 PG-SSOP-24-4 (Plastic Green Slim Small Outline Package)

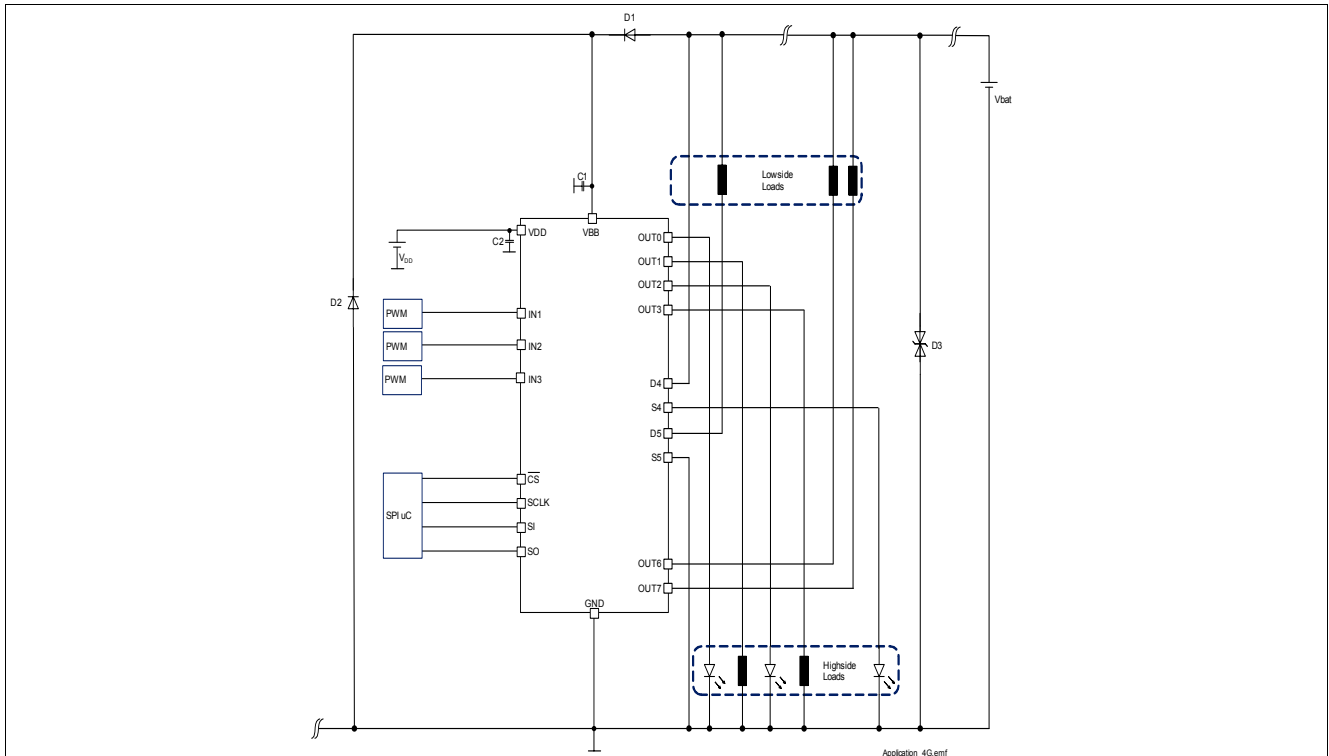
Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

## 11 Application Information

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

**Figure 14** shows a simplified application circuit. Vdd need to be externally reverse polarity protected.



**Figure 14 Application Diagram**

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

The circuit above shows a example of using this device in a automotive target application.

D1,C1 are used for blocking negative disturbances from Battery supply.

D2 is optional for loss of battery if no other circuit on this battery feed can limit the voltage to the negative max. rating of the device (-16 V) .

D3 is limiting the battery voltage below the maximum rated positive voltage of the VBB pin (40 V).

C2 is for EMC and to stabilize the digital driver, recommended value is 47nF.

There are no resistors to the µC needed due to the internal reverse polarity protection.

For further information you may contact <http://www.infineon.com/>

## 12 Revision History

Revision	Date	Changes
Rev. 1.0	2008-10-30	released Datasheet

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