

# DS21458DK Quad T1/E1/J1 Transceiver Design Kit Daughter Card

[www.maxim-ic.com](http://www.maxim-ic.com)

## GENERAL DESCRIPTION

The DS21458DK is an easy-to-use evaluation board for the DS21458 quad T1/E1/J1 transceiver. The DS21458DK is intended to be used as a daughter card with the DK101 motherboard or the DK2000 motherboard. The DS21458DK comes complete with a DS21458 quad SCT, transformers, termination resistors, configuration switches, line-protection circuitry, network connectors, and motherboard connectors. The DK101/DK2000 motherboard and Dallas' ChipView software give point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal and interrupt status. An on-board FPGA contains mux logic to connect framer ports to one another or to the DK2000 in a variety of configurations.

Each DS21458DK is shipped with a free DK101 motherboard. For complex applications, the DK2000 high-performance demo kit motherboard can be purchased separately.

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## DESIGN KIT CONTENTS

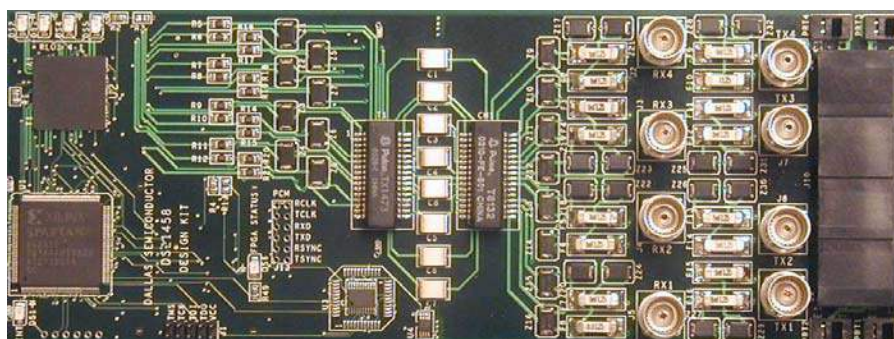
DS21458DK Design Kit Daughter Card  
 DK101 Low-Cost Motherboard  
 CD ROM  
 ChipView Software  
 DS21458DK Data Sheet  
 DK101 Data Sheet  
 DS21458 Data Sheet

## FEATURES

- Demonstrates Key Functions of DS21458 Quad T1/E1/J1 Transceiver
- Includes DS21458 Quad LIU, Transformers, BNC and RJ45 Network Connectors, and Termination Passives
- Compatible with DK101 and DK2000 Demo Kit Motherboards
- DK101/DK2000 and ChipView Software Provide Point-and-Click Access to the DS21458 Register Set
- All Equipment-Side Framer Pins are Easily Accessible for External Data Source/Sink
- Memory-Mapped FPGA Provides Flexible Clock/Data/Sync Connections Among Framer Ports and DK2000 Motherboard
- LEDs for Loss-of-Signal and Interrupt Status
- Easy-to-Read Silk Screen Labels Identify the Signals Associated with all Connectors, Jumpers, and LEDs
- Network Interface Protection for Overvoltage and Overcurrent Events

## ORDERING INFORMATION

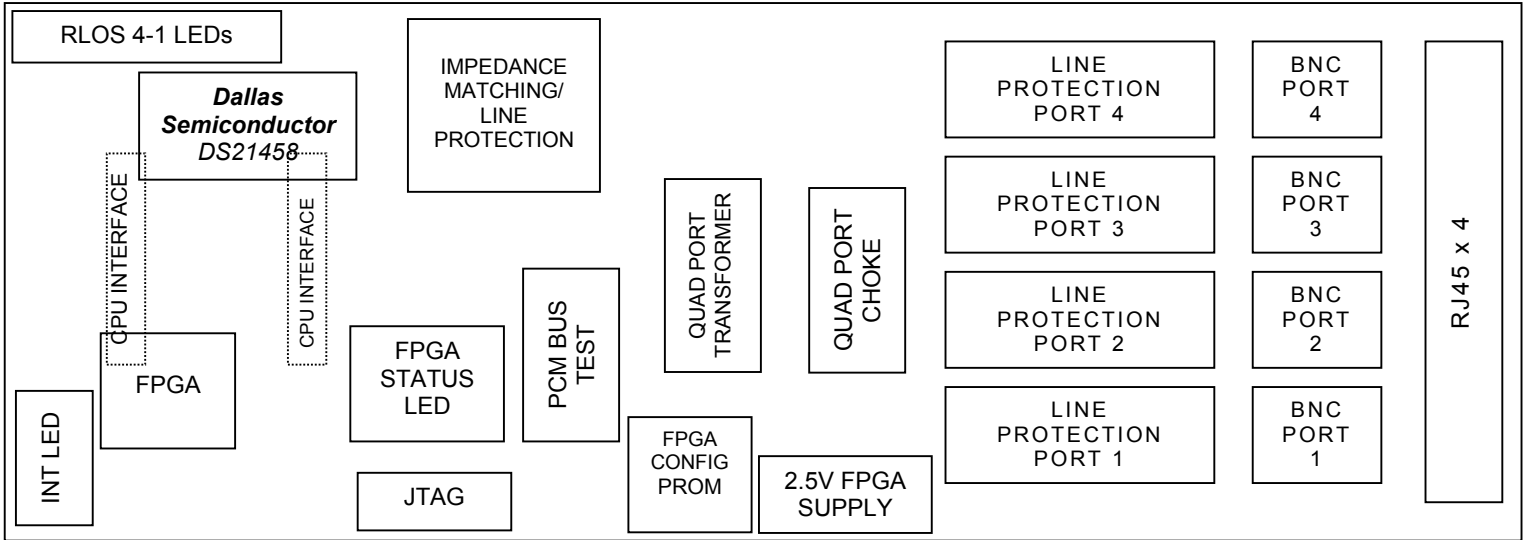
PART	DESCRIPTION
DS21458DK	DS21458 Design Kit Daughter Card (with included DK101 Motherboard)



**COMPONENT LIST**

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1–C8	8	0.22 $\mu$ F, 50V ceramic capacitors	Panasonic	PCF1152CT-ND
C9, C10, C12, C18, C22–C33, C35, C38–C43	23	0.1 $\mu$ F 10%, 16V ceramic capacitors (0603)	Phycomp	06032R104K7B20D
C11, C13–C15	4	0.1 $\mu$ F 10%, 25V ceramic capacitors (1206)	Panasonic	ECJ-3VB1E104K
C16, C17, C19– C21, C34, C36, C45, C46	9	1 $\mu$ F 10%, 16V ceramic capacitors (1206)	Panasonic	ECJ-3YB1C105K
C37, C44	2	10 $\mu$ F 20%, 10V ceramic capacitors (1206)	Panasonic	ECJ-3YB1A106M
CH1	1	Quad-port choke	Pulse Engineering	T8132
DS1	1	LED, red, SMD	Panasonic	LN1251C
DS2–DS6	5	LED, green, SMD	Panasonic	LN1351C
F1–F16	16	1.25A, 250V fuses, SMT	Teccor	F1250T
J1	1	10-pin connectors, dual row, vertical	Digi-Key	S2012-05-ND
J2–J9	8	5-pin BNC connectors, vertical	Cambridge	CP-BNCP-004
J10	1	8-pin, 4-port jack Right-angle RJ45	Molex	43223-8140
J11, J12	2	50-pin sockets, SMD, dual row, vertical	Samtec	TFM-125-02-S-D-LC
J13	1	12-pin connector, dual row, vertical Not populated	Digi-Key	S2012-06-ND
J14	1	1Mbit flash-based configuration memory	Xilinx	XCF01SV020C
PRT1–PRT4	4	6-pin through-hole slide switches DPDT	Tyco	SSA22
R1, R2, R4, R26, R39, R41, R45	7	10k $\Omega$ 5%, 1/10W resistors (0805)	Panasonic	ERJ-6GEYJ103V
R3, R27	2	1.0k $\Omega$ 5%, 1/10W resistors (0805)	Panasonic	ERJ-6GEYJ102V
R5–R12, R14– R21, R48	17	0 $\Omega$ 5%, 1/8W resistors (1206)	Panasonic	ERJ-8GEYJ0R00V
R13, R47	2	Not populated	Panasonic	Not populated
R22–R25	4	51.1 $\Omega$ 5%, 1/10W resistors (0805)	Panasonic	ERJ-6GEY51R1V
R29–R36	8	61.9 $\Omega$ 1%, 1/8W resistors (1206)	Panasonic	ERJ-8ENF61R9V
R40, R42–R44, R46, R49	6	330 $\Omega$ 5%, 1/10W MF resistors (0805)	Panasonic	ERA-6GEY331V
T1	1	SMT 32-pin octal T1/E1 transformer, transmit/receive, 1:2	Pulse Engineering	TX1473
U1	1	2.5V FPGA Spartan (Xilinx) 144-pin TQFP	Xilinx	XC2S50-5TQ144C
U2	1	3.3V T1/E1/J1 quad transceiver 0°C to +70°C, 256-pin BGA	Dallas Semiconductor	DS21458
U3	1	1M PROM for FPGA 44-pin TQFP	Xilinx	Not populated
U4	1	8-pin $\mu$ MAX, SO 2.5V or Adj	Maxim	MAX1792EUA25
Z1–Z8	8	50A, 6V Sidactor DO214 SMD	Teccor	P0080SAMC
Z9–Z16	8	500A, 25V Sidactor DO214 SMD	Teccor	P0300SCMC
Z17–Z32	16	500A, 170V Sidactor DO214 SMD	Teccor	P1800SCMC

## BOARD FLOORPLAN



## BASIC CONFIGURATION

This design kit relies upon several supporting files, which are available for downloading on our website at [www.maxim-ic.com/telecom](http://www.maxim-ic.com/telecom). See the DS21458DK QuickView data sheet for these files.

### Hardware Configuration

#### Using the DK101 Processor Board:

- Connect the daughter card to the DK101 processor board.
- Supply 3.3V to the banana-plug receptacles marked GND and VCC\_3.3V. (The external 5V connector is unused. Additionally, the TIM 5V supply headers are unused.)
- All processor board DIP switch settings should be in the ON position with exception of the flash programming switch, which should be OFF.
- From the Programs menu, launch the host application named ChipView.EXE. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs → ChipView → ChipView.

#### Using the DK2000 Processor Board:

- Connect the daughter card to the DK2000 processor board.
- Connect J1 to the power supply that is delivered with the kit. Alternately, a PC power supply may be connected to connector J2.
- From the Programs menu, launch the host application named ChipView.EXE. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs → ChipView → ChipView.

### General

- Upon power-up, the RLOS LEDs (green) will not be lit, the INT LED (red) will not be lit, but the FPGA Status LED (green) will be lit.
- When operating in E1 mode, slide SW1–SW4 to E1 Mode (grounding the BNC shell). When operating in T1 mode, slide SW1–SW4 to T1 Mode.

### Miscellaneous

- Clock frequencies and certain pin bias levels are provided by a register-mapped FPGA that is on the DS21458 daughter card.
- The definition file for this FPGA is named DS21458DC\_FPGA.def. See [Table 2](#) for the FPGA Register Map definitions. A drop-down menu on the top of the screen allows for switching between definition files.
- All files referenced above are available for download as described in the *Basic Configuration* section.

### Quick Setup (Demo Mode)

- The PC will load ChipView offering a choice among DEMO MODE, REGISTER VIEW, and TERMINAL MODE. Select Demo Mode.
- The program will request a configuration file. Select among the displayed files, which are DS2155\_E1\_DSNCOM\_DRV.R.cfg or DS2155\_T1\_DSNCOM\_DRV.R.cfg.
- The Demo Mode screen will appear. Upon external loopback the RLOS indicators will turn green.
- Note: Demo Mode interacts with the device driver, which resides in the DK101/DK2000 firmware. The current implementation of this driver is for one device. As such, the demo mode will only interact with Port 1. With minor changes, the device driver is extendible to N devices.

### Quick Setup (Register View)

- The PC will load ChipView offering a choice among DEMO MODE, REGISTER VIEW, and TERMINAL MODE. Select Register View.
- The program will request a definition file. Select DS21458DC\_FPGA.def through the Links section. This will also load DS21458DC.def.
- The Register View Screen will appear, showing the register names, acronyms, and values for the DS21458.
- Predefined Register settings for several functions are available as initialization files.
  - INI files are loaded by selecting the menu File→Reg Ini File→Load Ini File.
  - Load the INI file DS21458\_T1\_BERT\_ESF.ini.
  - After loading the INI file, the following may be observed:
    - o The RLOS LEDs turns green upon external loopback.
    - o All four ports of the DS21458 begin transmitting a Daly pattern. When external loopback is applied, the BERT bit count registers BBC1 to BBC3 and BEC1 to BEC3 may be updated by clearing and setting BC1.LC and clicking the 'Read All' button.

## ADDRESS MAP

DK101 daughter card address space begins at 0x81000000

DK2000 daughter card address space begins at:

0x30000000 for slot 0

0x40000000 for slot 1

0x50000000 for slot 2

0x60000000 for slot 3

All offsets given below are relative to the beginning of the daughter card address space (shown above).

**Table 1. Daughter Card Address Map**

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0015	FPGA	Board identification and clock/signal routing
0X1000 to 0X10ff	T1/E1/J1 Transceiver #1	DS21458 T1/E1/J1 transceiver, port 1
0X1100 to 0X11ff	T1/E1/J1 Transceiver #2	DS21458 T1/E1/J1 transceiver, port 2
0X1200 to 0X12ff	T1/E1/J1 Transceiver #3	DS21458 T1/E1/J1 transceiver, port 3
0X1300 to 0X13ff	T1/E1/J1 Transceiver #4	DS21458 T1/E1/J1 transceiver, port 4

Registers in the FPGA can be easily modified using the ChipView host-based user-interface software along with the definition file named "DS21458DC\_FPGA.def."

## FPGA REGISTER MAP

**Table 2. FPGA Register Map**

OFFSET	NAME	TYPE	DESCRIPTION
0X0000	BID	Read Only	BOARD ID
0X0002	XBIDH	Read Only	HIGH NIBBLE EXTENDED BOARD ID
0X0003	XBIDM	Read Only	MIDDLE NIBBLE EXTENDED BOARD ID
0X0004	XBIDL	Read Only	LOW NIBBLE EXTENDED BOARD ID
0X0005	BREV	Read Only	BOARD FAB REVISION
0X0006	AREV	Read Only	BOARD ASSEMBLY REVISION
0X0007	PREV	Read Only	PLD REVISION
0X0011	MCSR	Control	DS21458 MCLK Pin Source
0X0012	TCSR	Control	DS21458 TCLK Pin Source
0X0013	SYSCLKT	Control	DS21458 TSYCLK Pin Setting
0X0014	SYSCLKR	Control	DS21458 RSYCLK Pin Setting
0X0015	SYNC1	Control	DS21458 TSYNC Source
0X0016	SYNC2	Control	DS21458 TSSYNC Source
0X0017	SYNC3	Control	DS21458 RSYNC Source
0X0018	TSERS	Control	TSER Source
0X0019	PRSER	Control	PCM RSER Source
0X001A	PSYNC	Control	PCM RSYNC/TSYNC Source
0X001B	PCLK	Control	PCM RCLK/TCLK Source

## ID REGISTERS

### **BID: BOARD ID (Offset = 0X0000)**

BID is read only with a value of 0xD.

### **XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset = 0X0002)**

XBIDH is read only with a value of 0x0.

### **XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset = 0X0003)**

XBIDM is read only with a value of 0x1.

### **XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset = 0X0004)**

XBIDL is read only with a value of 0x6.

### **BREV: BOARD FAB REVISION (Offset = 0X0005)**

BREV is read only and displays the current fab revision.

### **AREV: BOARD ASSEMBLY REVISION (Offset = 0X0006)**

AREV is read only and displays the current assembly revision.

### **PREV: PLD REVISION (Offset = 0X0007)**

PREV is read only and displays the current PLD firmware revision.

## CONTROL REGISTERS

Register Name: **MCSR**

Register Description: **DS21458 MCLK Pin Source**

Register Offset: **0x0011**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	MSRCB	MSRCA
Default	—	—	—	—	—	—	1	1

### Bit 0: DS21458 Port 1 and 3 MCLK Source (MSRCA)

0 = Connect MCLK 1 (controls port 1 and 3) to the 1.544MHz clock

1 = Connect MCLK 1 (controls port 1 and 3) to the 2.048MHz clock

### Bit 1: DS21458 Port 2 and 4 MCLK Source (MSRCA)

0 = Connect MCLK 2 (controls port 2 and 4) to the 1.544MHz clock

1 = Connect MCLK 2 (controls port 2 and 4) to the 2.048MHz clock

Register Name: **TCSR**

Register Description: **DS21458 TCLK Pin Source**

Register Offset: **0x0012**

Bit #	7	6	5	4	3	2	1	0
Name	T4S1	T4S0	T3S1	T3S0	T2S1	T2S0	T1S1	T1S0
Default	0	0	0	0	0	0	0	0

### Bit 0 to 1: DS21458 Port 1 TCLK Source (T1S0, T1S1)

The source for TCLK 1 is Defined as shown in Table 3.

### Bit 2 to 3: DS21458 Port 2 TCLK Source (T2S0, T2S1)

The source for TCLK 2 is Defined as shown in Table 3.

### Bit 4 to 5: DS21458 Port 3 TCLK Source (T3S0, T3S1)

The source for TCLK 3 is Defined as shown in Table 3.

### Bit 6 to 7: DS21458 Port 4 TCLK Source (T4S0, T4S1)

The source for TCLK 3 is Defined as shown in Table 3.

**Table 3. TCLKx Source Definition**

TxS1, TxS0	TCLK CONNECTION
00	Drive TCLK <sub>x</sub> with the 1.544MHz clock
01	Drive TCLK <sub>x</sub> with the 2.048MHz clock
10	Drive TCLK <sub>x</sub> with RCLK <sub>x</sub>
11	N/A

Register Name: **SYCLKT**

Register Description: **DS21458 TSYCLK Pin Setting**

Register Offset: **0x0013**

Bit #	7	6	5	4	3	2	1	0
Name	R4S1	R4S0	R3S1	R3S0	R2S1	R2S0	R1S1	R1S0
Default	0	0	0	0	0	0	0	0

**Bit 0 to 1: DS21458 Port 1 TSYCLK Source (R1S0, R1S1)**

The source for TSYCLK 1 is Defined as shown in Table 4.

**Bit 2 to 3: DS21458 Port 2 TSYCLK Source (R2S0, R2S1)**

The source for TSYCLK 2 is Defined as shown in Table 4.

**Bit 4 to 5: DS21458 Port 3 TSYCLK Source (R3S0, R3S1)**

The source for TSYCLK 3 is Defined as shown in Table 4.

**Bit 6 to 7: DS21458 Port 4 TSYCLK Source (R4S0, R4S1)**

The source for TSYCLK 4 is Defined as shown in Table 4.

**Table 4. TSYCLK<sub>x</sub> Source Definition**

RxS1, RxS0	TSYCLK <sub>x</sub> CONNECTION
00	Drive TSYCLK <sub>x</sub> with the 1.544MHz clock
01	Drive TSYCLK <sub>x</sub> with the 2.048MHz clock
10	Drive TSYCLK <sub>x</sub> with 8.192MHz clock
11	Drive TSYCLK <sub>x</sub> with DS21458 Port <sub>x</sub> BPCLK



Register Name: **SYCLKR**Register Description: **DS21458 RSYCLK Pin Setting**Register Offset: **0x0014**

Bit #	7	6	5	4	3	2	1	0
Name	T4S1	T4S0	T3S1	T3S0	T2S1	T2S0	T1S1	T1S0
Default	0	0	0	0	0	0	0	0

**Bit 0 to 1: DS21458 Port 1 RSYCLK Source (T1S0, T1S1)**

The source for RSYCLK 1 is Defined as shown in Table 5.

**Bit 2 to 3: DS21458 Port 2 RSYCLK Source (T2S0, T2S1)**

The source for RSYCLK 2 is Defined as shown in Table 5.

**Bit 4 to 5: DS21458 Port 3 RSYCLK Source (T3S0, T3S1)**

The source for RSYCLK 3 is Defined as shown in Table 5.

**Bit 6 to 7: DS21458 Port 4 RSYCLK Source (T4S0, T4S1)**

The source for RSYCLK 4 is Defined as shown in Table 5.

**Table 5. RSYCLK<sub>x</sub> Source Definition**

TxS1, TxS0	RSYCLK <sub>x</sub> CONNECTION
00	Drive RSYCLK <sub>x</sub> with the 1.544MHz clock
01	Drive RSYCLK <sub>x</sub> with the 2.048MHz clock
10	Drive RSYCLK <sub>x</sub> with 8.192MHz clock
11	Drive RSYCLK <sub>x</sub> with DS21458 Port <sub>x</sub> BPCLK

Register Name: **SYNC1**Register Description: **DS21458 TSYNC Pin Source**Register Offset: **0x0015**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	T4SRC	T3SRC	T2SRC	T1SRC
Default	—	—	—	—	0	0	0	0

**Bit 0: DS21458 Port 1 TSYNC Source (T1SRC)**

0 = TSYNC 1 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSYNC 1 with RSYNC 1

**Bit 1: DS21458 Port 2 TSYNC Source (T2SRC)**

0 = TSYNC 2 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSYNC 2 with RSYNC 2

**Bit 2: DS21458 Port 3 TSYNC Source (T3SRC)**

0 = TSYNC 3 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSYNC 3 with RSYNC 3

**Bit 3: DS21458 Port 4 TSYNC Source (T4SRC)**

0 = TSYNC 4 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSYNC 4 with RSYNC 4

**Note:** When driving TSYNC<sub>x</sub> with RSYNC<sub>x</sub> the corresponding DS21458 port should be configured such that TSYNC<sub>x</sub> is an input (IOCR1.1 = 0) and RSYNC<sub>x</sub> is an output (IOCR1.4 = 0).

Register Name: **SYNC2**

Register Description: **DS21458 TSSYNC Pin Source**

Register Offset: **0x0016**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	T4SRC	T3SRC	T2SRC	T1SRC
Default	—	—	—	—	0	0	0	0

**Bit 0: DS21458 Port 1 TSSYNC Source (T1SRC)**

0 = Not using transmit-side elastic store, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSSYNC 1 with RSYNC 1

**Bit 1: DS21458 Port 2 TSSYNC Source (T2SRC)**

0 = Not using transmit-side elastic store, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSSYNC 2 with RSYNC 2

**Bit 2: DS21458 Port 3 TSSYNC Source (T3SRC)**

0 = Not using transmit-side elastic store, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSSYNC 3 with RSYNC 3

**Bit 3: DS21458 Port 4 TSSYNC Source (T4Source)**

0 = Not using transmit-side elastic store, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSSYNC 4 with RSYNC 4

**Note:** When driving TSSYNcx with RSYNcx the corresponding DS21458 port should be configured such that RSYNcx is an output (IOCR1.4 = 0).

Register Name: **SYNC3**Register Description: **DS21458 RSYNC Pin Setting**Register Offset: **0x0017**

Bit #	7	6	5	4	3	2	1	0
Name	RSOR1	RSOR0	—	—	R4IO	R3IO	R2IO	R1IO
Default	0	0	—	—	0	0	0	0

**Bit 0: DS21458 Port 1 RSYNC Setting (R1IO)**

0 = RSYNC 1 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive RSYNC 1 with RSYNC<sub>x</sub> as shown in Table 6**Bit 1: DS21458 Port 2 RSYNC Setting (R2IO)**

0 = RSYNC 2 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive RSYNC 2 with RSYNC<sub>x</sub> as shown in Table 6**Bit 2: DS21458 Port 3 RSYNC Setting (R3IO)**

0 = RSYNC 3 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive RSYNC 4 with RSYNC<sub>x</sub> as shown in Table 6**Bit 3: DS21458 Port 4 RSYNC Setting (R4IO)**

0 = RSYNC 4 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive RSYNC 4 with RSYNC<sub>x</sub> as shown in Table 6

**Note:** When driving RSYNC<sub>y</sub> with RSYNC<sub>x</sub> the corresponding DS21458 port should be configured such that RSYNC<sub>x</sub> is an output (IOCR1.4 = 0) and RSYNC<sub>y</sub> is an input (IOCR1.4 = 1).

**Table 6. RSYNC<sub>x</sub> Function Definition**

RSOR1, RSOR0	MASTER RSYNC DESIGNATION
00	RSYNC 1 is used to drive other RSYNC pins (providing R <sub>x</sub> IO = 1)
01	RSYNC 2 is used to drive other RSYNC pins (providing R <sub>x</sub> IO = 1)
10	RSYNC 3 is used to drive other RSYNC pins (providing R <sub>x</sub> IO = 1)
11	RSYNC 4 is used to drive other RSYNC pins (providing R <sub>x</sub> IO = 1)

Register Name: **TSERS**Register Description: **DS21458 TSER Pin Source**Register Offset: **0x0018**

Bit #	7	6	5	4	3	2	1	0
Name	T4S1	T4S0	T3S1	T3S0	T2S1	T2S0	T1S1	T1S0
Default	0	0	0	0	0	0	0	0

**Bit 0 to 1: DS21458 Port 1 TSER Source (T1S0, T1S1)**

The source for TSER 1 is Defined as shown in Table 7.

**Bit 2 to 3: DS21458 Port 2 TSER Source (T2S0, T2S1)**

The source for TSER 2 is Defined as shown in Table 7.

**Bit 4 to 5: DS21458 Port 3 TSER Source (T3S0, T3S1)**

The source for TSER 3 is Defined as shown in Table 7.

**Bit 6 to 7: DS21458 Port 4 TSER Source (T4S0, T4S1)**

The source for TSER 4 is Defined as shown in Table 7.

**Table 7. TSERx Source Definition**

TxS1, TxS0	TSER <sub>x</sub> CONNECTION
00	Tri-state TSER <sub>x</sub> (weak pulldown)
01	Drive TSER <sub>x</sub> with RSER <sub>x</sub>
10	Drive TSER <sub>x</sub> with PCM_TXD bus (DK2000 only)
11	N/A

Register Name: **PRSER**Register Description: **PCM RSER Source**Register Offset: **0x0019**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	R1EN	R1EN	R1EN	R1EN
Default	—	—	—	—	0	0	0	0

**Bit 0 to 1: PCM RSER Source (R1EN)**

0 = Do not drive DS21458 Port 1 RSER onto PCM\_RSER

1 = Logically OR DS21458 Port 1 RSER with selected other RSER pins and drive onto PCM\_RSER

**Bit 2 to 3: DS21458 Port 2 TSER Source (T2S0, T2S1)**

0 = Do not drive DS21458 Port 2 RSER onto PCM\_RSER

1 = Logically OR DS21458 Port 2 RSER with selected other RSER pins and drive onto PCM\_RSER

**Bit 4 to 5: DS21458 Port 3 TSER Source (T3S0, T3S1)**

0 = Do not drive DS21458 Port 3 RSER onto PCM\_RSER

1 = Logically OR DS21458 Port 3 RSER with selected other RSER pins and drive onto PCM\_RSER

**Bit 6 to 7: DS21458 Port 4 TSER Source (T4S0, T4S1)**

0 = Do not drive DS21458 Port 4 RSER onto PCM\_RSER

1 = Logically OR DS21458 Port 4 RSER with selected other RSER pins and drive onto PCM\_RSER

**Note:** PRSER register is for use with the DK2000 only.

Register Name: **PSYNC**Register Description: **PCM RSYNC/TSYNC Source**Register Offset: **0x001A**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	T2SR	T1SR	—	—	R2SR	R1SR
Default	—	—	0	0	—	—	0	0

**Bit 0 to 1: PCM\_RSYNC Source**

R2SR, R1SR	PCM_RSYNC SOURCE
00	PCM_RSYNC is driven by DS21458 port 1 RSYNC
01	PCM_RSYNC is driven by DS21458 port 2 RSYNC
10	PCM_RSYNC is driven by DS21458 port 3 RSYNC
11	PCM_RSYNC is driven by DS21458 port 4 RSYNC

**Bit 4 to 5: PCM\_TSYNC Source**

T2SR, T1SR	PCM_TSYNC SOURCE
00	PCM_TSYNC is driven by DS21458 port 1 TSYNC
01	PCM_TSYNC is driven by DS21458 port 2 TSYNC
10	PCM_TSYNC is driven by DS21458 port 3 TSYNC
11	PCM_TSYNC is driven by DS21458 port 4 TSYNC

**Note:** PSYNC register is for use with the DK2000 only.

Register Name: **PCLK**Register Description: **PCM RCLK/TCLK Source**Register Offset: **0x001B**

Bit #	7	6	5	4	3	2	1	0
Name	—	TCM	T2SR	T1SR	—	RCM	R2SR	R1SR
Default	—	0	0	0	—	0	0	0

**Bit 0 to 2: PCM\_RCLK Source**

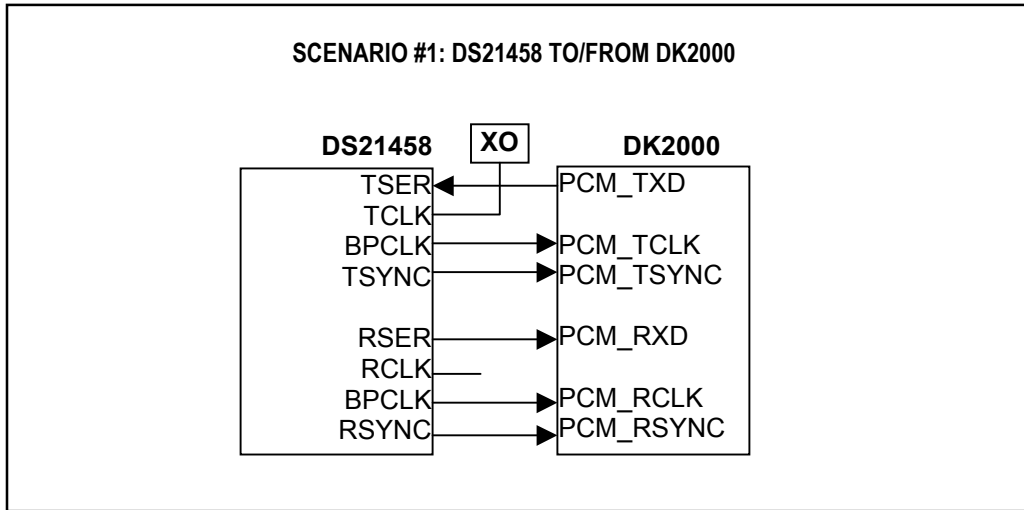
RCM,R2SR, R1SR	PCM_RCLK SOURCE
000	PCM_RCLK is driven by DS21458 port 1 RCLK
001	PCM_RCLK is driven by DS21458 port 2 RCLK
010	PCM_RCLK is driven by DS21458 port 3 RCLK
011	PCM_RCLK is driven by DS21458 port 4 RCLK
100	PCM_RCLK is driven by DS21458 port 1 BPCLK
101	PCM_RCLK is driven by DS21458 port 2 BPCLK
110	PCM_RCLK is driven by DS21458 port 3 BPCLK
111	PCM_RCLK is driven by DS21458 port 4 BPCLK

**Bit 4 to 5: PCM\_TCLK Source**

TCM,T2SR, T1SR	PCM_TCLK SOURCE
000	PCM_TCLK is driven by source used for DS21458 port 1 TCLK
001	PCM_TCLK is driven by source used for DS21458 port 2 TCLK
010	PCM_TCLK is driven by source used for DS21458 port 3 TCLK
011	PCM_TCLK is driven by source used for DS21458 port 4 TCLK
100	PCM_TCLK is driven by DS21458 port 1 BPCLK
101	PCM_TCLK is driven by DS21458 port 2 BPCLK
110	PCM_TCLK is driven by DS21458 port 3 BPCLK
111	PCM_TCLK is driven by DS21458 port 4 BPCLK

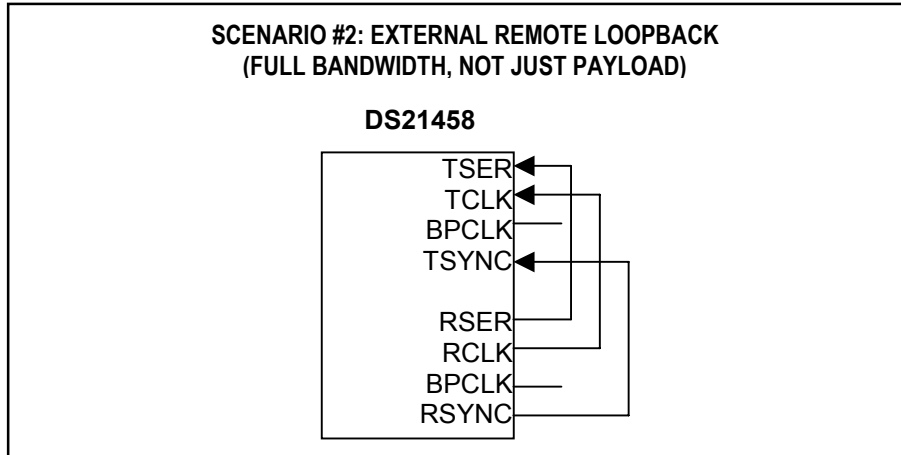
**Note:** PCLK register is for use with the DK2000 only.

## FPGA CONTROL EXAMPLES



**Table 8. FPGA Configuration for Scenario #1 (Port 1, T1 Mode)**

REGISTER	SETTING	COMMENT
MCSR	0X01	Drive DS21458 ports 1 and 3 MCLK with 2.048MHz
TCSR	0X00	Drive TCLK with 1.544MHz
SYSCLKT	0X00	Drive TSYCLK with 1.544MHz
SYSCLKR	0X00	Drive RSYCLK with 1.544MHz
SYNC1	0X00	Tri-state FPGA driver pin for DS21458 TSYNC1
SYNC2	0X01	Drive TSSYNC1 with RSYNC1
SYNC3	0X00	Tri-state FPGA driver pin for DS21458 RSYNC
TSERS	0X02	Drive DS21458 TSER1 with data from PCM bus
PRSER	0X01	Drive DS21458 RSER1 onto PCM bus
PSYNC	0X00	PCM RSYNC and PCM TSYNC are provided by DS21458 port 1 RSYNC and TSYNC (respectively)
PCLK	0X44	PCM RCLK and TCLK are driven by port 1 BPCLK

**FPGA CONTROL EXAMPLES (continued)****Table 9. FPGA Configuration for Scenario #2 (Port 1, T1 Mode)**

REGISTER	SETTING	COMMENT
MCSR	0X01	Drive DS21458 ports 1 and 3 MCLK with 2.048MHz
TCSR	0X02	Drive TCLK1 with RCLK1
SYSCLKT	0X00	Drive TSYSCLK with 1.544MHz
SYSCLKR	0X00	Drive RSYSCLK with 1.544MHz
SYNC1	0X01	Drive TSYNC1 with RSYNC1
SYNC2	0X01	Drive TSSYNC1 with RSYNC1
SYNC3	0X00	Tri-state FPGA driver pin for DS21458 RSYNC
TSERS	0X01	Drive DS21458 TSER1 with data from RSER1
PRSER	N/A	Unused
PSYNC	N/A	Unused
PCLK	N/A	Unused

**Table 10. DS21458 Partial Configuration for Scenario #2 (Port 1, T1 Mode)**

REGISTER	SETTING	COMMENT
IOCR1	TSIO = 0; RSIO = 0	TSYNC is an input, RSYNC is an output
ESCR	TESE = 0; RESE = 0	Bypass Rx and Tx elastic stores
CCR1	TCSS1 = 0; TCSS2 = 0	TCLK is driven by TCLK pin



## **DS21458 INFORMATION**

For more information about the DS21458, please consult the DS21458 data sheet available on our website at [www.maxim-ic.com/DS21458](http://www.maxim-ic.com/DS21458). Software downloads are also available for this design kit.

## **DS21458DK INFORMATION**

For more information about the DS21458DK, including software downloads, please consult the DS21458DK data sheet available on our website at [www.maxim-ic.com/DS21458DK](http://www.maxim-ic.com/DS21458DK).

## **TECHNICAL SUPPORT**

For additional technical support, please e-mail your questions to [telecom.support@dalsemi.com](mailto:telecom.support@dalsemi.com).

## **SCHEMATICS**

The DS21458DK schematics are featured at the end of this document.

# DS21458 DESIGN KIT

## REVISIONS: (MODIFICATION FROM DS21Q55 BOARD)

### CONTENTS

1. COVER PAGE
2. DS21458 CONTROL AND BACKPLANE
3. PORT 1 AND 2 TX / RX SYSTEM SIDE
4. PORT 3 AND 4 TX / RX SYSTEM SIDE
5. PORT 1 TX / RX ANALOG PATHS
6. PORT 2 TX / RX ANALOG PATHS
7. PORT 3 TX / RX ANALOG PATHS
8. PORT 4 TX / RX ANALOG PATHS
9. DAUGHTER CARD ADDRESS DATA BUS CONNECTION
10. FPGA CROSS CONNECT FOR RX / TX SIGNALS
11. FPGA AND CONFIG PROM CONTROL
12. FPGA CLOCK AND DATABUS
13. SUPPLY DECOUPLING
14. SIGNAL CROSS-REFERENCE
15. COMPONENT CROSS-REFERENCE

1. ESIBRD CONNECTIONS CHANGE FROM 4X TO 1X (ONLY PULLDOWNS REMAIN)
2. ADDED A8 AND A9 TO DS21458 AND FPGA, REMOVED CS2-4
3. REMOVED RLOS FPGA CONNECTION, RLOS LED IS NOW DRIVEN BY THE SCT
4. REMOVED SERIAL CONFIG PROM, REPLACED WITH XILINX FLASH BASED CONFIG PROM
5. RAN PIN SWAP ON XILINX PART TO ACCOMMODATE PIN DIFFERENCES BETWEEN DS21458 AND DS21Q55
6. REMOVED TEST POINTS IN JTAG CHAIN
7. REMOVED CONNECTION BETWEEN 2.5V SUPPLY MONITOR AND FPGA INIT PIN
8. REMOVED CONNECTION BETWEEN CPU RESET AND FPGA PROGRAM PIN  
-FPGA RESET IS NOW DRIVEN BY INTERNAL STATE MACHINE
9. CHANGED SWITCH NAMES FOR PORT 1-4 FROM SW PREFIX TO PRT PREFIX
10. ADDED T1 E1 DESIGNATION TO SWITCHES FOR PORT 1-4
11. CHANGED SILKSCREEN ON JTAG CONNECTOR

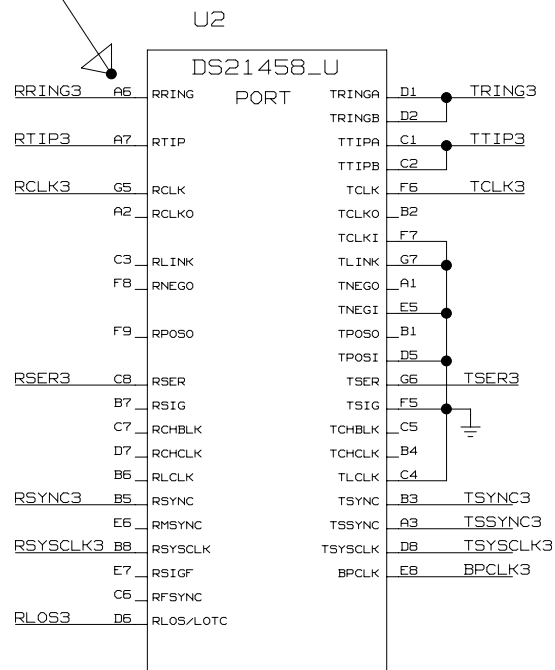
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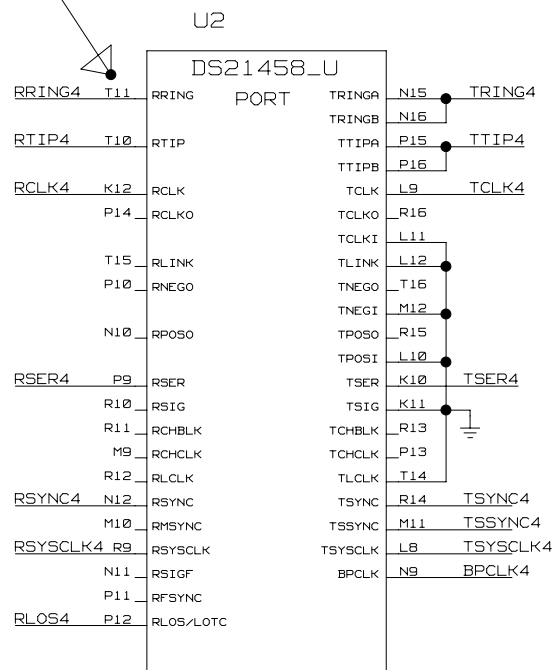




PORT3\_RRING = PIN A6

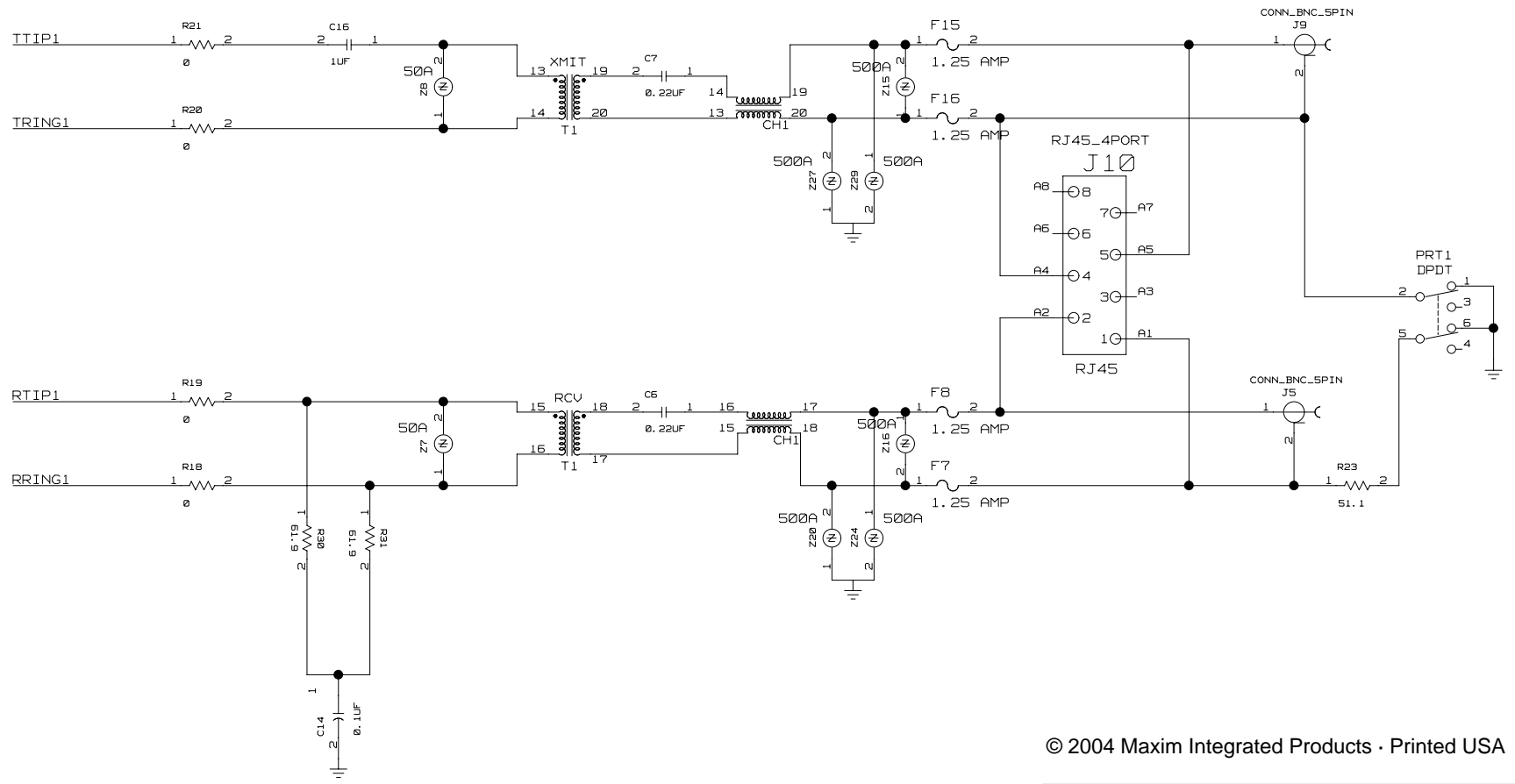


PORT4\_RRING = PIN T11



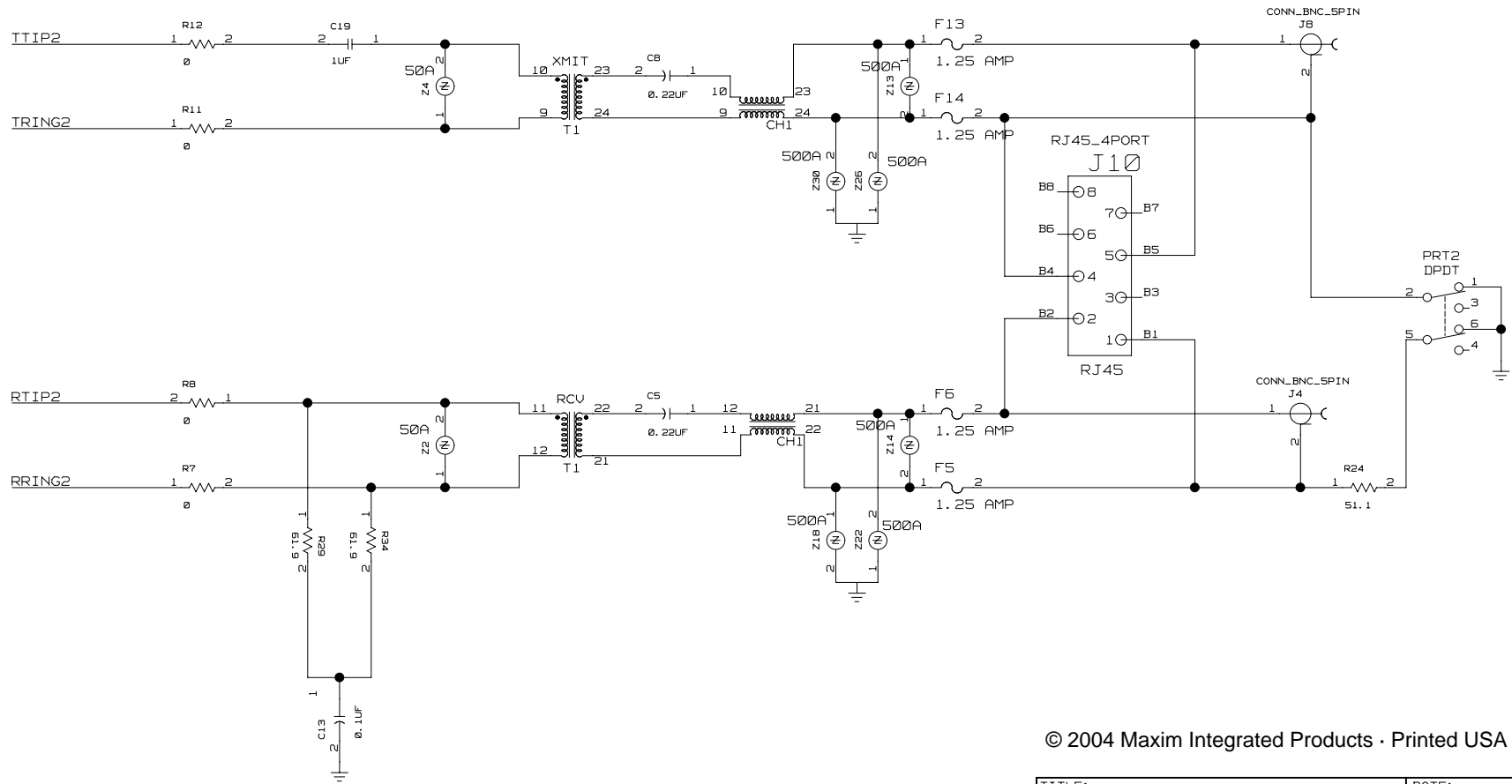
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TITLE:	DS21458DK01A0	DATE:	05/30/03
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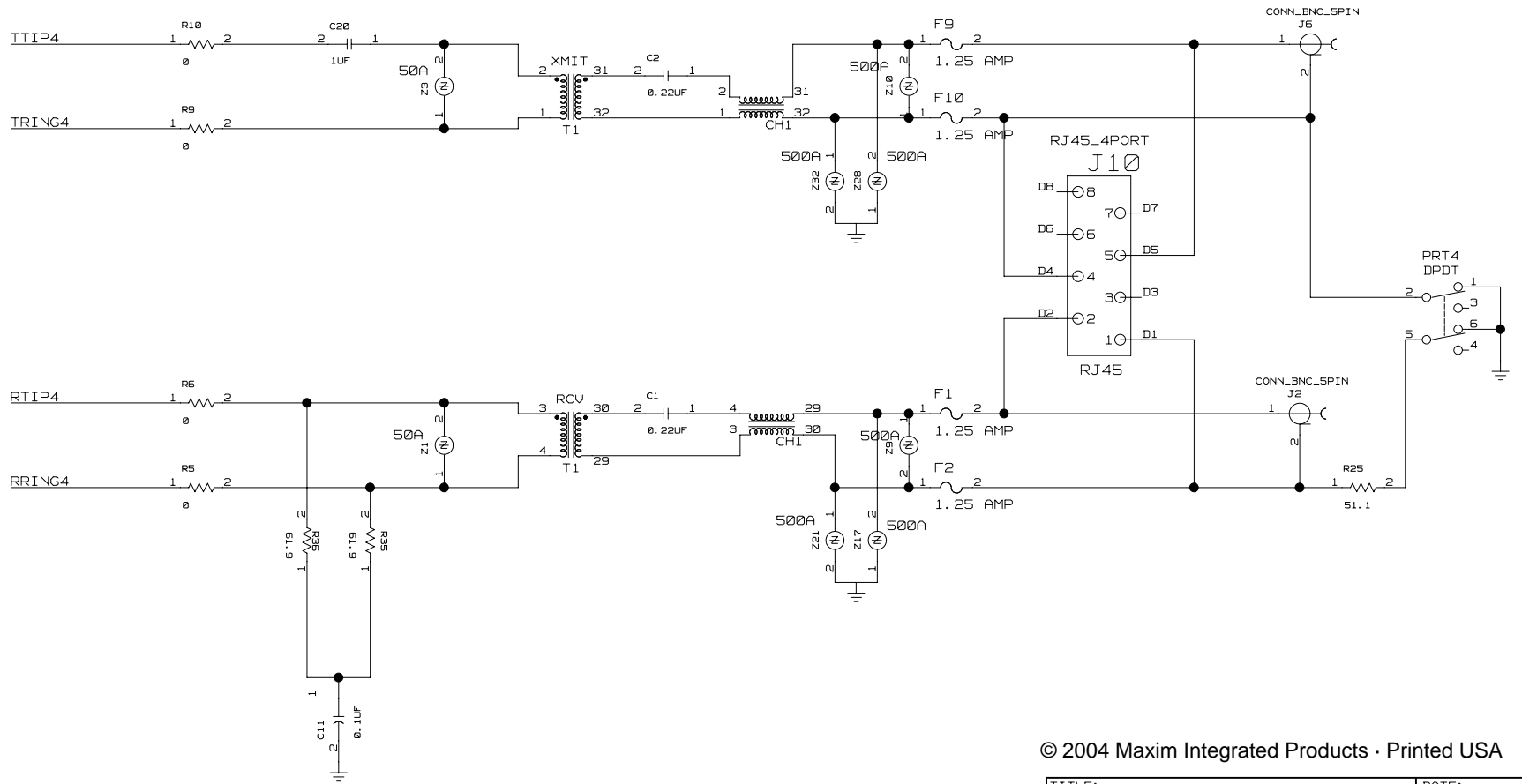


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TITLE:	DS21458DK01A0	DATE:	05/30/03
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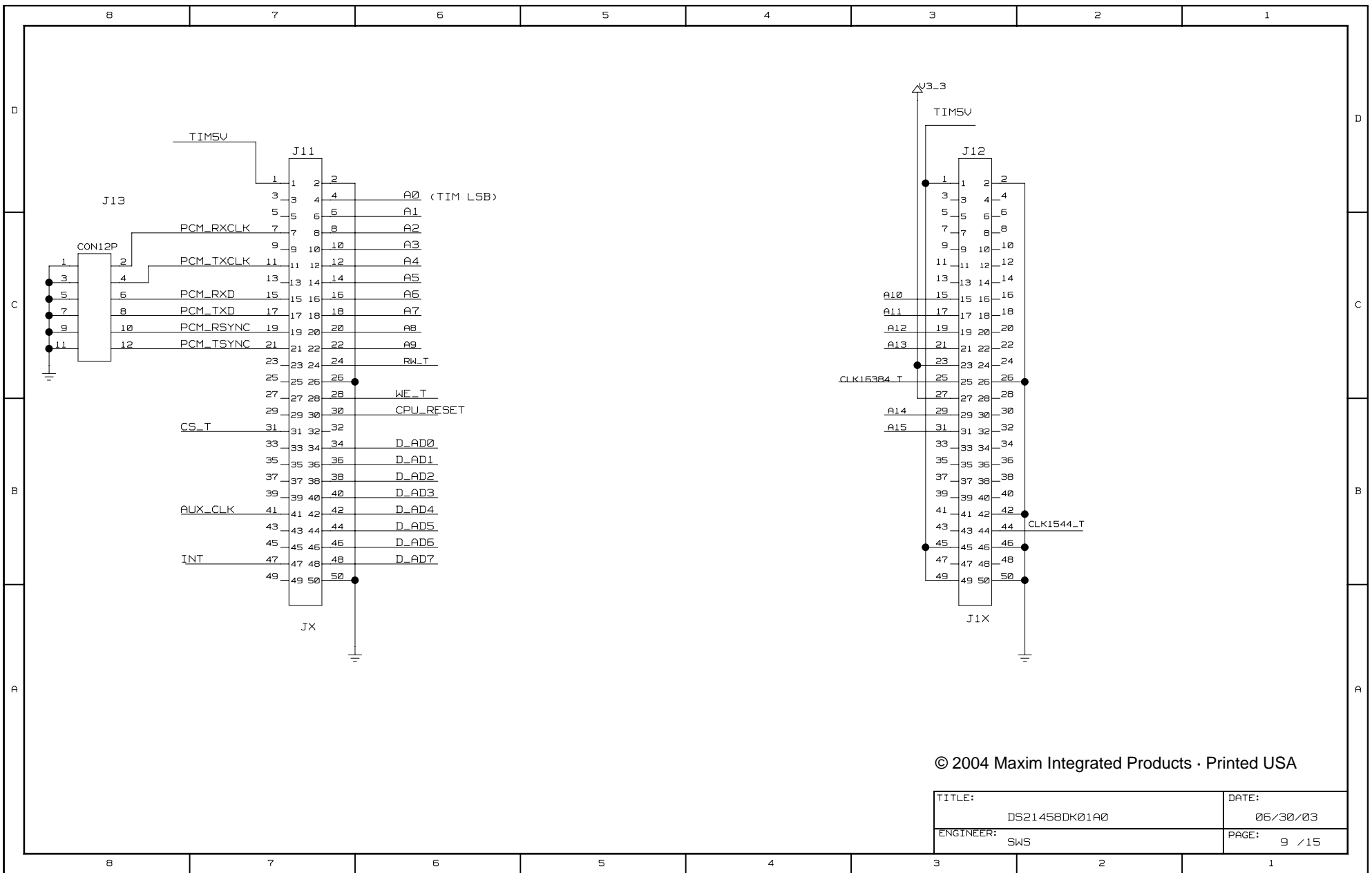






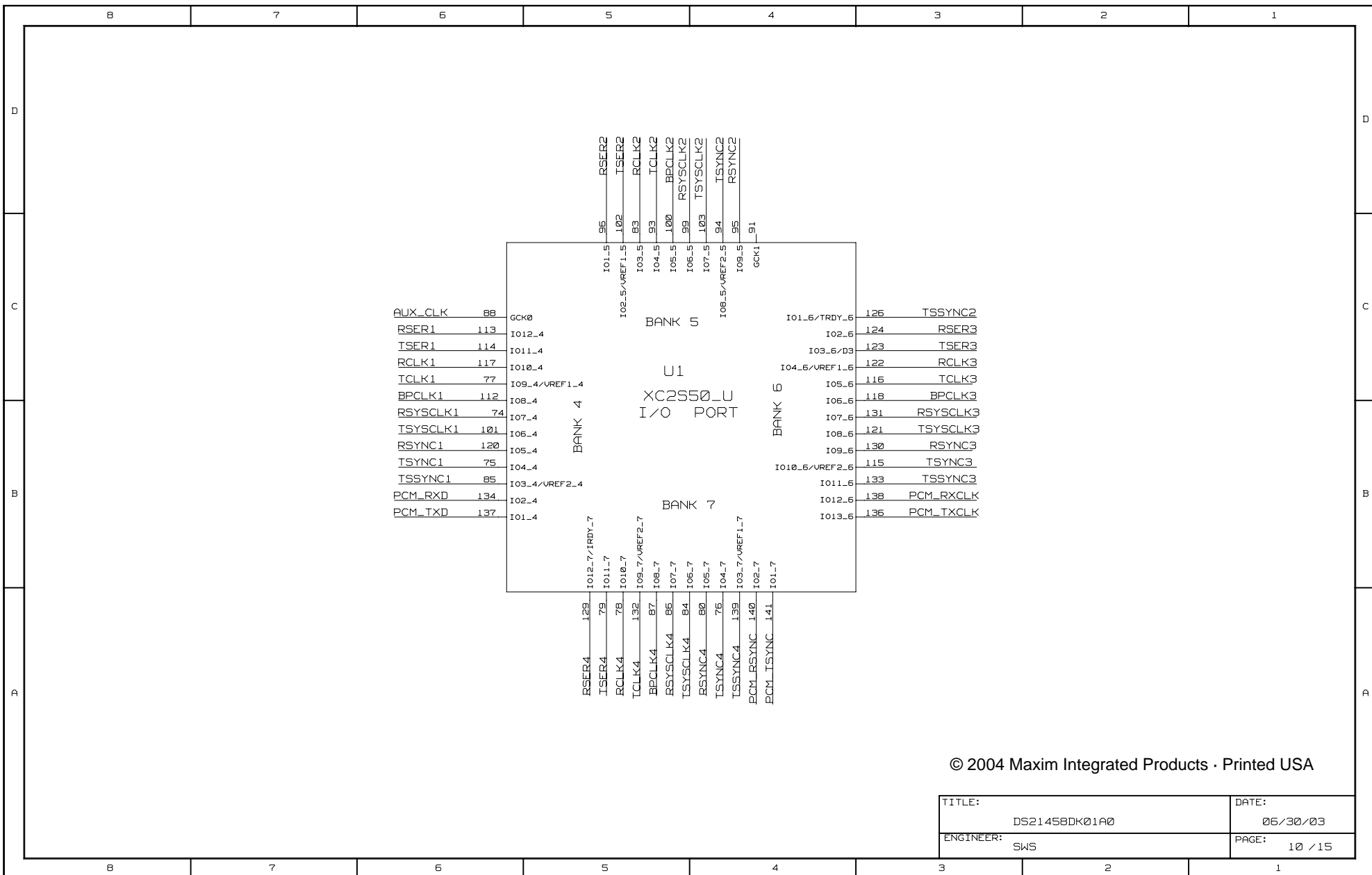
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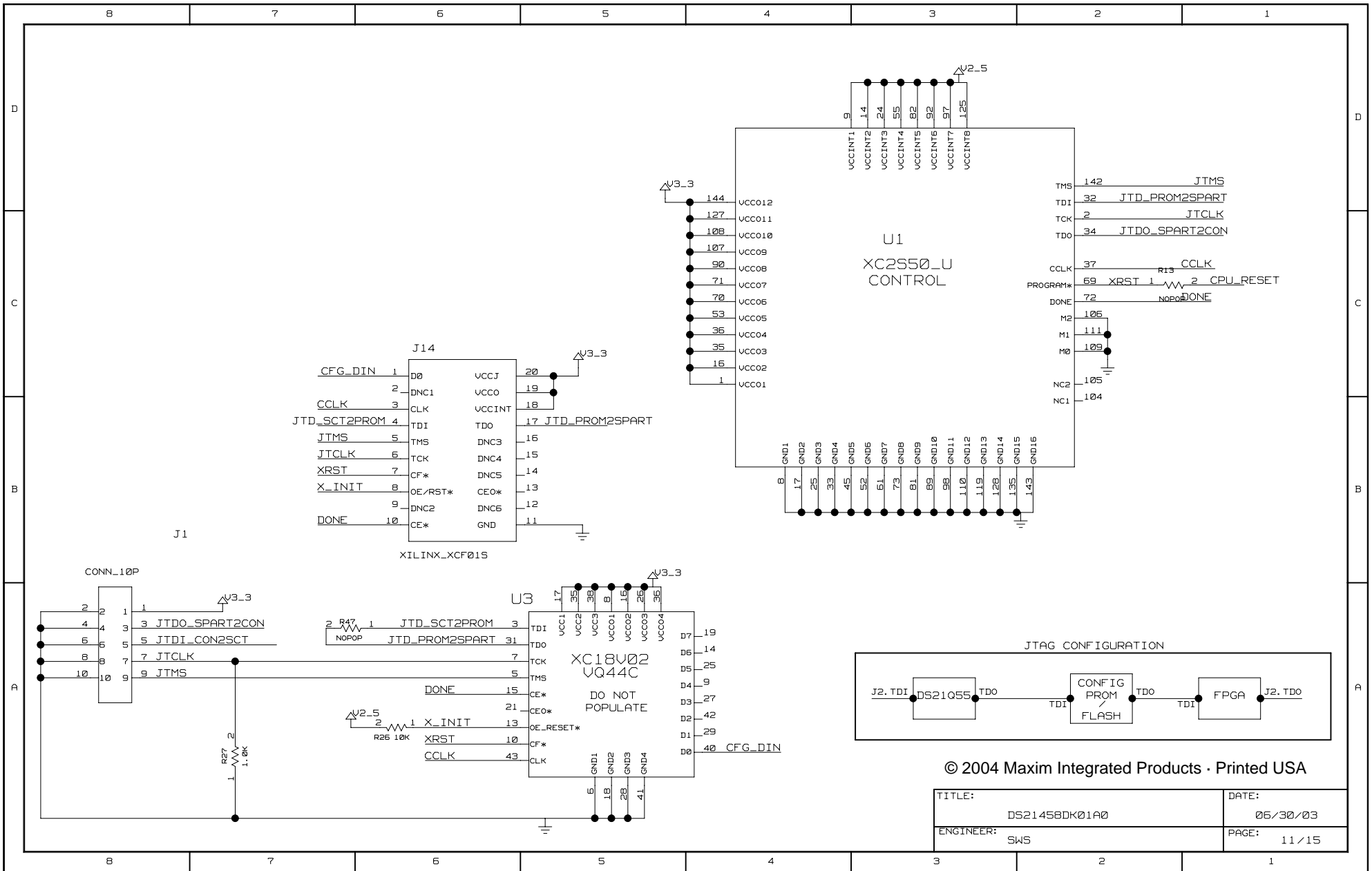
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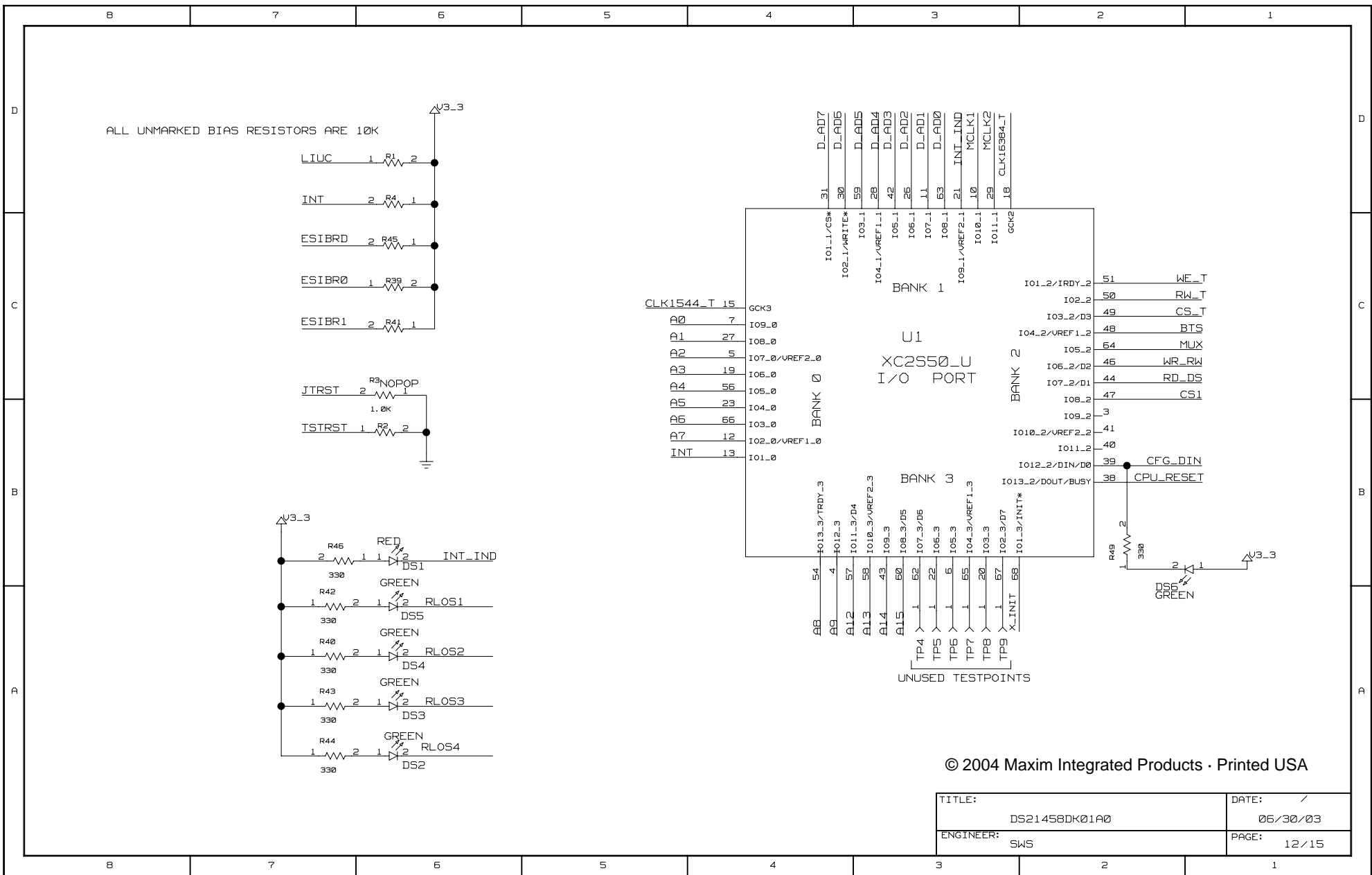
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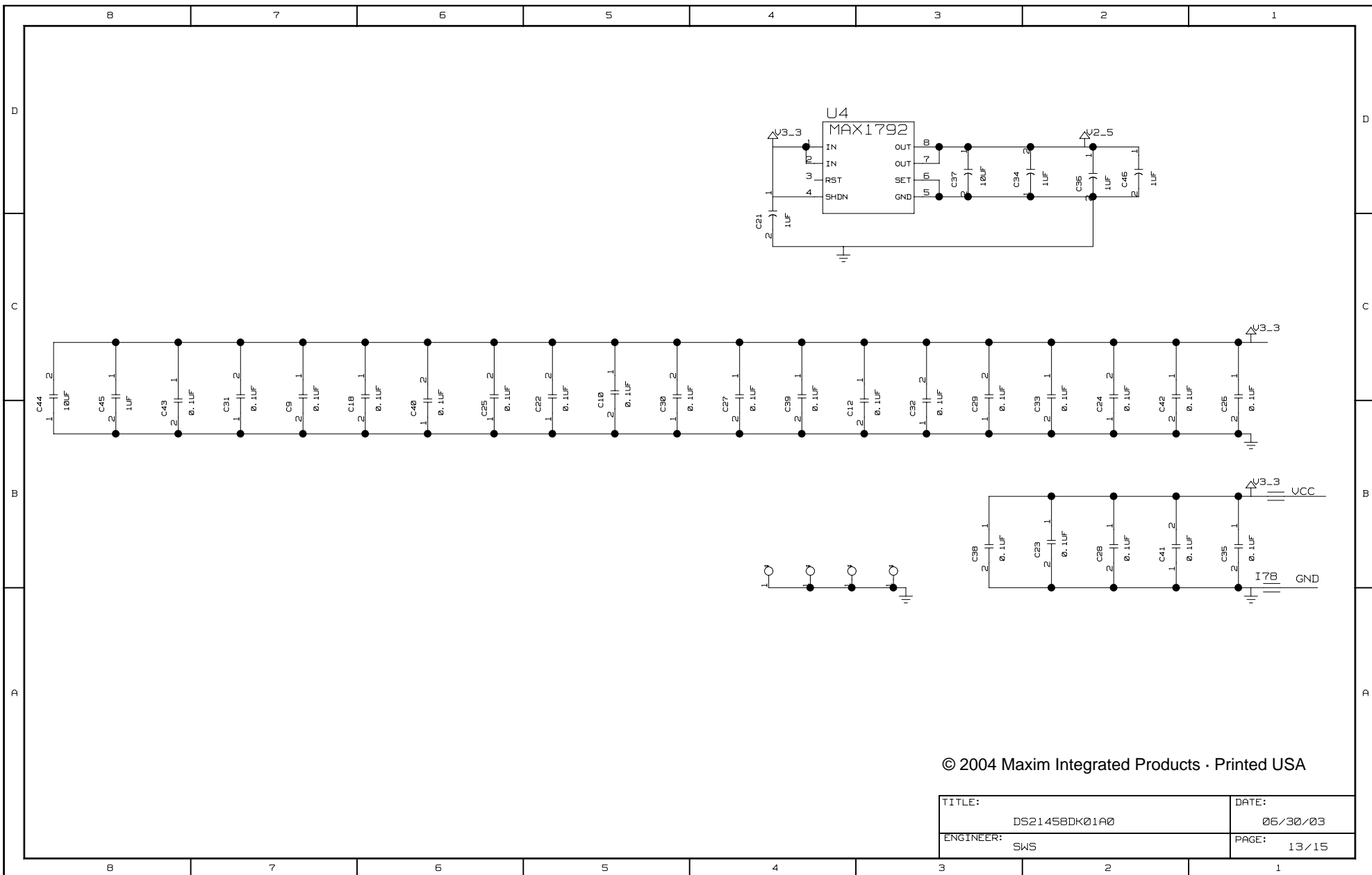
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	8	7	6	5	4	3	2	1
D	*** Signal Cross-Reference for the entire design ***		RSER3	4B8 < 10C3 <				
	A0	9D6 < 12C5 < 2D3 <	RSER4	4B4 < 10A5 <				
C	A1	9C6 < 12C5 < 2C3 <	RSYNC1	3B8 < 10B6 <				
	A2	9C6 < 12C5 < 2C3 <	RSYNC2	3B4 < 10D4 <				
	A3	9C6 < 12C5 < 2C3 <	RSYNC3	4B8 < 10B3 <				
	A4	9C6 < 12C5 < 2C3 <	RSYNC4	4B4 < 10A4 <				
	A5	9C6 < 12B5 < 2C3 <	RSYSCLK1	10B6 < 3B8 <				
	A6	9C6 < 12B5 < 2C3 <	RSYSCLK2	10D5 < 3B4 <				
	A7	9C6 < 12B5 < 2C3 <	RSYSCLK3	10B3 < 4B8 <				
	A8	9C6 < 12A4 < 2C3 <	RSYSCLK4	10A5 < 4A4 <				
	A9	9C6 < 12A4 < 2C3 <	RTIP1	3C8 < 5B8 <				
	A10	9C3 <	RTIP2	3C4 < 5B8 <				
B	A11	9C3 <	RTIP3	4C8 < 7B8 <				
	A12	9C3 < 12A4 <	RTIP4	4C4 < 8B8 <				
	A13	9C3 < 12A3 <	RW_T	9C6 < 12C1 <				
	A14	9B3 < 12A3 <	TCLK1	10C6 < 3C5 <				
	A15	9B3 < 12A3 <	TCLK2	10D5 < 3C1 <				
	ALX_CLK	9B8 < 10C6 <	TCLK3	10C3 < 4C5 <				
	BPCLK1	3A5 < 10B6 <	TCLK4	10A5 < 4C1 <				
	BPCLK2	3A1 < 10D5 <	TIMSU	9D3 < 9D8 <				
	BPCLK3	4A6 < 10B3 <	TRING1	3C5 < 5C8 <				
	BPCLK4	4A1 < 10A5 <	TRING2	3C1 < 6C8 <				
A	BTS	12C1 < 2B3 <	TRING3	4C5 < 7C8 <				
	CCLK	11B7 < 11A6 < 11C1 <	TRING4	4C1 < 8C8 <				
	CFG_DIN	11A4 < 11C7 < 12B1 <	TSER1	10C6 < 3B5 <				
	CLK1544_T	9B2 < 12C5 <	TSER2	10D5 < 3B1 <				
	CLK163B4_T	9C4 < 12D3 <	TSER3	10C3 < 4B5 <				
	CPU_RESET	9B5 < 12B1 < 11C1 <	TSER4	10A5 < 4B1 <				
	CS1	12B1 < 2B8 <	TSSYNC1	10B6 < 3B5 <				
	CS_T	9B8 < 12C1 <	TSSYNC2	10C3 < 3B1 <				
	DONE	11B7 < 11A6 < 11C1 <	TSSYNC3	10B3 < 4B5 <				
	D_AD0	2C3 < 9B6 < 12D3 <	TSSYNC4	10A4 < 4B1 <				
D_AD1	2B3 < 9B6 < 12D3 <	TSTRST	2B8 < 12B7 <					
D_AD2	2B3 < 9B6 < 12D3 <	TSYNC1	3B5 < 10B6 <					
D_AD3	2B3 < 9B6 < 12D3 <	TSYNC2	3B1 < 10D4 <					
D_AD4	2B3 < 9B6 < 12D3 <	TSYNC3	4B6 < 10B3 <					
D_AD5	2B3 < 9B6 < 12D3 <	TSYNC4	4B1 < 10A4 <					
D_AD6	2B3 < 9B6 < 12D4 <	TSYSCLK1	10B6 < 3B5 <					
D_AD7	2B3 < 9B6 < 12D4 <	TSYSCLK2	10D4 < 3B1 <					
ESIBR0	2B3 < 12C7 <	TSYSCLK3	10B3 < 4B5 <					
ESIBR1	2A3 < 12C7 <	TSYSCLK4	10A5 < 4A1 <					
ESIBRD	2B3 < 12C7 <	TTIP1	3C5 < 5C8 <					
INT	2C8 < 9B8 < 12B5 < 12D7 <	TTIP2	3C1 < 6C8 <					
INT_IND	12B6 < 12D3 <	TTIP3	4C5 < 7C8 <					
JTCLK	11A8 < 11B7 < 2C8 < 11C1 <	TTIP4	4C1 < 8C8 <					
JTD1_CON25CT	11A7 < 2C8 <	WE_T	9B6 < 12C1 <					
JTD0_SPART2CON	11A7 < 11C1 <	WR_RW	12C1 < 2B8 <					
JTD_PROM2SPART	11A6 < 11B5 < 11D1 <	XRST	11A6 < 11B7 < 11C2 <					
JTD_SCT2PROM	11B7 < 2C8 < 11A6 <	X_INIT	11A6 < 11B7 < 12A3 <					
JTMS	11A8 < 11B7 < 2C8 < 11D1 <							
JTRST	2D8 < 12C7 <							
LIUC	2C8 < 12D7 <							
MCLK1	12D3 < 2C8 <							
MCLK2	12D3 < 2C8 <							
MUX	12C1 < 2B3 <							
PCH_RSYNC	9C8 < 10A4 <							
PCH_RXCLK	9C8 < 10B3 <							
PCH_RXD	9C8 < 10B5 <							
PCH_TSYNC	9C8 < 10A4 <							
PCH_TXCLK	9C8 < 10B3 <							
PCH_TXD	9C8 < 10B6 <							
RCLK1	3C8 < 10C6 <							
RCLK2	3C4 < 10D5 <							
RCLK3	4C8 < 10C3 <							
RCLK4	4C4 < 10A5 <							
RD_D5	12C1 < 2B8 <							
RL0S1	3A8 < 12A6 <							
RL0S2	3A4 < 12A6 <							
RL0S3	4A8 < 12A6 <							
RL0S4	4A4 < 12A6 <							
RRING1	3C8 < 5B8 <							
RRING2	3C4 < 5B8 <							
RRING3	4C8 < 7B8 <							
RRING4	4C4 < 8B8 <							
RSER1	3B8 < 10C6 <							
RSER2	3B4 < 10D5 <							
	8	7	6	5	4	3	2	1

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	8	7	6	5	4	3	2	1	
D	<p>*** Part Cross-Reference for the entire design ***</p> <p>C1 CAP 8B5 C2 CAP 8C5 C3 CAP 7C5 C4 CAP 7B5 C5 CAP 6B5 C6 CAP 5B5 C7 CAP 5C5 C8 CAP 6C5 C9 CAP 13B7 C10 CAP 13B5 C11 CAP 8A6 C12 CAP 13B4 C13 CAP 6A6 C14 CAP 5A6 C15 CAP 7A6 C16 CAP 5D6 C17 CAP 7D6 C18 CAP 13B7 C19 CAP 6C5 C20 CAP 8C5 C21 CAP 13C4 C22 CAP 13B5 C23 CAP 13B2 C24 CAP 13B2 C25 CAP 13B6 C26 CAP 13B1 C27 CAP 13B4 C28 CAP 13B2 C29 CAP 13B3 C30 CAP 13B5 C31 CAP 13B7 C32 CAP 13B3 C33 CAP 13B2 C34 CAP 13D3 C35 CAP 13B1 C36 CAP 13D2 C37 CAP 13D3 C38 CAP 13B3 C39 CAP 13B4 C40 CAP 13B6 C41 CAP 13B2 C42 CAP 13B2 C43 CAP 13B8 C44 CAP 13B8 C45 CAP 13B8 CH1 CHOKE_QUADPORT_T1 5B4 5C4 6B4 6C4 7B4 7C4 8B4 8C4 DS1 LED 12B6 DS2 LED 12A6 DS3 LED 12A6 DS4 LED 12A6 DS5 LED 12B6 DS6 LED 12B2 F1 FUSE 8B4 F2 FUSE 8B4 F3 FUSE 7B4 F4 FUSE 7B4 F5 FUSE 6B3 F6 FUSE 6B3 F7 FUSE 5B4 F8 FUSE 5B4 F9 FUSE 8D4 F10 FUSE 8C4 F11 FUSE 7D4 F12 FUSE 7C4 F13 FUSE 6D3 F14 FUSE 6C3 F15 FUSE 5D4 F16 FUSE 5C4 J1 CONN_10P 11B8 J2 CONN_BNC_SPIN 8B2 J3 CONN_BNC_SPIN 7B2 J4 CONN_BNC_SPIN 6B2 J5 CONN_BNC_SPIN 5B2 J6 CONN_BNC_SPIN 8D2</p>		<p>J7 CONN_BNC_SPIN 7D2 J8 CONN_BNC_SPIN 6D2 J9 CONN_BNC_SPIN 5D2 J10 RJ45_8 5C3 6C3 7C3 8C3 J11 CONN_50P2 9D7 J12 CONN_50P2 9D3 J13 CON12P 9D6 J14 XILINX_XCF01S 11C6 PRT1 SWITCH_DPDT_SLIDE_6P 5C1 PRT2 SWITCH_DPDT_SLIDE_6P 6C1 PRT3 SWITCH_DPDT_SLIDE_6P 7C1 PRT4 SWITCH_DPDT_SLIDE_6P 8C1 R1 RES1 12D6 R2 RES1 12B6 R3 RES 12C6 R4 RES1 12D6 R5 RES 8B7 R6 RES 8B7 R7 RES 6B7 R8 RES 6B7 R9 RES 8C7 R10 RES 8D7 R11 RES 6C7 R12 RES 6D7 R13 RES1 11C2 R14 RES 7C7 R15 RES 7D7 R16 RES 7B7 R17 RES 7B7 R18 RES 5B7 R19 RES 5B7 R20 RES 5C7 R21 RES 5D7 R22 RES 7B2 R23 RES 5B2 R24 RES 6B2 R25 RES 8B2 R26 RES 11A6 R27 RES1 11A7 R29 RES1 6A6 R30 RES1 5A6 R31 RES1 5A6 R32 RES1 7A6 R33 RES1 7A6 R34 RES1 6A6 R35 RES1 8A6 R36 RES1 8A6 R39 RES 12C6 R40 RES1 12A7 R41 RES 12C6 R42 RES1 12A7 R43 RES1 12A7 R44 RES1 12A7 R45 RES 12C6 R46 RES1 12B7 R47 RES1 11A7 R48 RES 2C7 R49 RES1 12B2 T1 XFMR_QUADPORT_T1 5B5 5C5 6B5 6C5 7B5 7C5 8B5 8C5 TP1 TSTPNT_SNG 13B3 TP4 TESTPOINT 12A3 TP5 TESTPOINT 12A3 TP6 TESTPOINT 12A3 TP7 TESTPOINT 12A3 TP8 TESTPOINT 12A3 TP9 TESTPOINT 12A3 TP24 TSTPNT_SNG 13B4 TP25 TSTPNT_SNG 13B4 TP26 TSTPNT_SNG 13B4 U1 XC28S0_U 10C5 11C3 12C3 U2 DS2145B_U 2C5 3C3 3C7 4C3 4C7 U3 XC18V02V044C_U 11A6 U4 MAX1792 13D4 Z1 SIDACTOR_2 8B6 Z2 SIDACTOR_2 6B6 Z3 SIDACTOR_2 8C6</p>		<p>Z4 SIDACTOR_2 6C6 Z5 SIDACTOR_2 7B6 Z6 SIDACTOR_2 7C6 Z7 SIDACTOR_2 5B6 Z8 SIDACTOR_2 5C6 Z9 SIDACTOR_2 8B4 Z10 SIDACTOR_2 8C4 Z11 SIDACTOR_2 7C4 Z12 SIDACTOR_2 7B4 Z13 SIDACTOR_2 6C4 Z14 SIDACTOR_2 6B4 Z15 SIDACTOR_2 5C4 Z16 SIDACTOR_2 5B4 Z17 SIDACTOR_2 8A4 Z18 SIDACTOR_2 6A4 Z19 SIDACTOR_2 7A4 Z20 SIDACTOR_2 5A4 Z21 SIDACTOR_2 8A4 Z22 SIDACTOR_2 6A4 Z23 SIDACTOR_2 7A4 Z24 SIDACTOR_2 5A4 Z25 SIDACTOR_2 7C4 Z26 SIDACTOR_2 6C4 Z27 SIDACTOR_2 5C4 Z28 SIDACTOR_2 8C4 Z29 SIDACTOR_2 5C4 Z30 SIDACTOR_2 6C4 Z31 SIDACTOR_2 7C4 Z32 SIDACTOR_2 8C4</p>				
C									
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A									
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