EVALUATION KIT AVAILABLE

*Click **here** to ask an associate for production status of specific part numbers.*

MAX16151

High Voltage Pushbutton On/Off Controller

General Description

The MAX16151 is a high voltage, pushbutton on/off controller with a switch debouncer and built-in latch. This device accepts a noisy input from a mechanical switch and produces a clean, latched output, as well as a one-shot interrupt output, in response to a switch closure exceeding the debounce period at $\overline{PB\_IN}$. A switch closure longer than the shutdown period at $\overline{PB\_IN}$ results in a longer one-shot interrupt output. The MAX16151 family has two sets of devices: one in which a longer switch closure greater than the shutdown period deasserts the latched output, and another in which the latched output stays asserted. See Table 1 for more information.

The MAX16151 operates from a supply range of +5V to +36V and consumes less than 15µA of supply current to ensure minimal battery current in low-power applications. The robust switch input ($\overline{PB\_IN}$) handles ±60V levels and is ±10kV electrostatic discharge (ESD) protected for use in harsh industrial environments. The 3V regulated latched output can serve as a logic signal to control a pass transistor or voltage regulator. A separate $\overline{INT}$ output provides a system interrupt whenever a valid pushbutton signal is detected. An asynchronous $\overline{CLR}$ input allows an external signal to force the latched output to the OFF state. The MAX16151 operates over the -40°C to +125°C temperature range and is available in a 1.23mm x 0.83mm, 6-bump wafer-level package (WLP), and a 6-pin thin SOT23 package.

Applications

- Portable Instruments
- Industrial Equipment
- Desktop and Notebook Computers
- Telecommunication and Servers

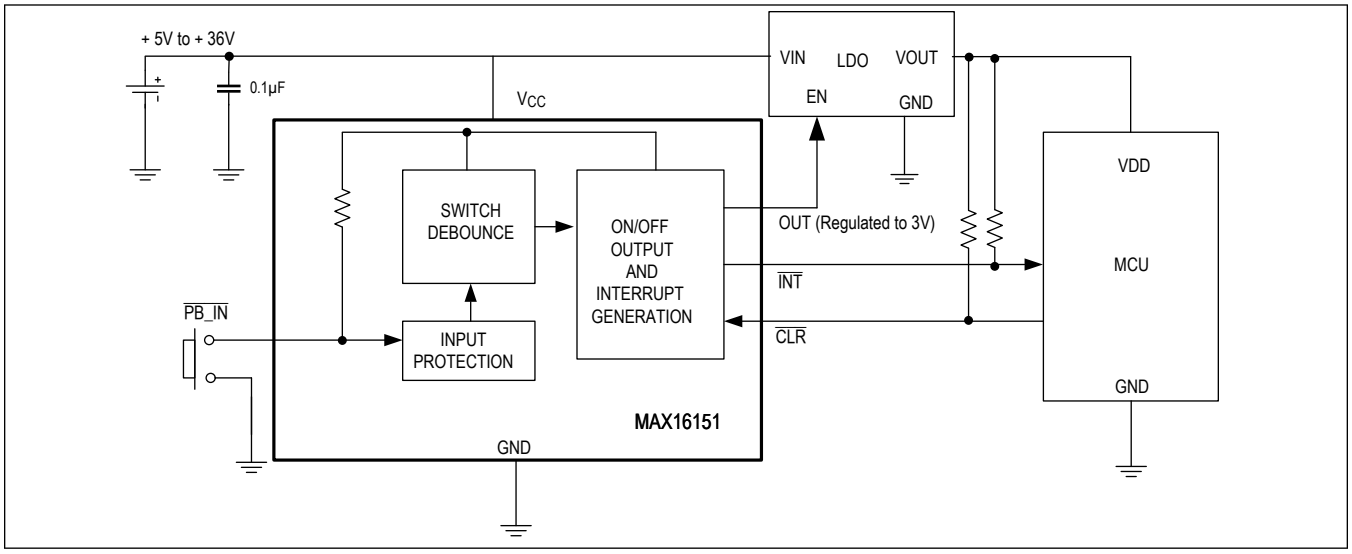
Benefits and Features

- Up to +36V Operating Range
- 3.0V Regulated Latched Output
- 10µA Standby Current (ISB)
- Debounces Noisy Switches
  - 50ms and 2s Debounce Timing Options
  - 8s and 16s Shutdown Periods
- One-shot $\overline{INT}$ Output on Each Switch Closure
- 32ms $\overline{INT}$ Duration
- Pushbutton Input Handle Up to ±60V
- ±10kV HMB ESD Protection
- 6-pin SOT23 and 1.23mm x 0.83mm, 6-bump WLP
- -40°C to +125°C Operating Temperature Range

***Ordering Information** appears at end of data sheet.*

19-100988, Rev 0; 7/21

Typical Application Circuit



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Absolute Maximum Ratings

V_{CC} to GND ..... -0.3V to +40V
PB_IN to GND ..... -60V to +60V
CLR, INT, OUT to GND ..... -0.3V to 6V
Continuous Power Dissipation (6 SOT23, Single Layer Board) (T_A = +70°C, derate 8.70mW/°C above +70°C.) 696mW
Continuous Power Dissipation (6 WLP, Multilayer Board) (T_A = +70°C, derate 10.50mW/°C above +70°C.) 840mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -40°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

6 SOT23

Package Code	U6+1
Outline Number	21-0058
Land Pattern Number	90-0175
Thermal Resistance, Single Layer Board:	
Junction to Ambient (θ_{JA})	N/A
Junction to Case Thermal Resistance (θ_{JC})	80°C/W
Thermal Resistance, Four Layer Board:	
Junction to Ambient (θ_{JA})	115°C/W
Junction to Case Thermal Resistance (θ_{JC})	80°C/W

6 WLP

Package Code	W60C1+2
Outline Number	21-100258
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	95.15°C/W
Junction to Case Thermal Resistance (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

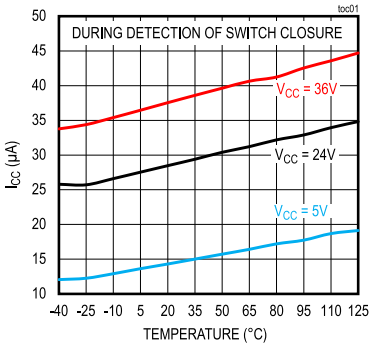
(V_{CC} = V_{MIN} to V_{MAX}, T_A = -40°C to +125°C, Typical values are at T_A = +25°C and V_{CC} = +24V. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design, test, and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}		5		36	V
Power Supply Current	I_{SB}	V_{CC} = 36V, OUT not asserted, PB_IN not connected. -40°C ≤ T_A ≤ +125°C		10	15	µA
	I_{CC}	V_{CC} = 36V, I_{OUT} = 0; During $\overline{PB\_IN}$ detection or $\overline{INT}$ assertion		40		µA
Timing Accuracy		Deviation from nominal value of debounce time (t_{DB}), shutoff time (t_{SO}), and interrupt time (t_{INT})	-20	±5	+20	%
Input High Voltage	V_{IH}	$\overline{CLR}$ and $\overline{PB\_IN}$	1.7			V
Input Low Voltage	V_{IL}	$\overline{CLR}$ and $\overline{PB\_IN}$			0.7	V
Minimum Input High Time Detected		$\overline{PB\_IN}$		600		µs
$\overline{PB\_IN}$ Hysteresis				100		mV
$\overline{PB\_IN}$ Pullup Resistance			500	1000	1500	kΩ
$\overline{PB\_IN}$ Input Current	I_{IN}	$V_{\overline{PB\_IN}}$ = ±60V	-170		+170	µA
$\overline{PB\_IN}$ Voltage Range		Continuous; 0V ≤ V_{CC} ≤ 36V	-60		+60	V
		Transient; 0V ≤ V_{CC} ≤ 36V	-60		+60	
$\overline{CLR}$ Input Current	I_{CLR}		-100		+100	nA
$\overline{CLR}$ Falling Edge to OUT Low Propagation Delay	t_{CO}	R_L = 10kΩ, C_L = 100pF			200	ns
$\overline{CLR}$ Lockout Time		Period following rising edge of OUT during which transitions on $\overline{CLR}$ are ignored.	1.6x tINT	2x tINT	2.4x tINT	ms
OUT Output Voltage	V_{OL}	I_{SINK} = 1.6mA			0.4	V
	V_{OH}	I_{SOURCE} = 50uA	2.7			
OUT Output Voltage (DC)	V_{OH}	+5 ≤ V_{CC} ≤+36, I_{OUT} = 0		3		V
$\overline{INT}$ Output Voltage	V_{OL_INT}	I_{SINK} = 1mA			0.2	V
$\overline{INT}$ Leakage Current			-100		+100	nA
Interrupt Pulse Duration	t_{INT}	Beginning at t_{DB}	25.6	32	38.4	ms
		Beginning at end of t_{SO}	102.4	128	153.6	
$\overline{PB\_IN}$ ESD Protection		Human Body Model		±10		kV

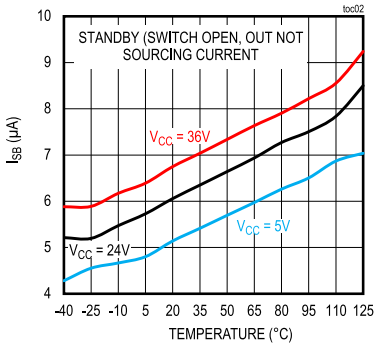
Typical Operating Characteristics

(V_{CC} = +24V, T_A = +25°C, unless otherwise noted.)

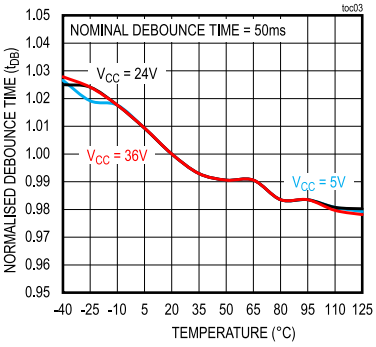
SUPPLY CURRENT (I_{CC}) vs. TEMPERATURE



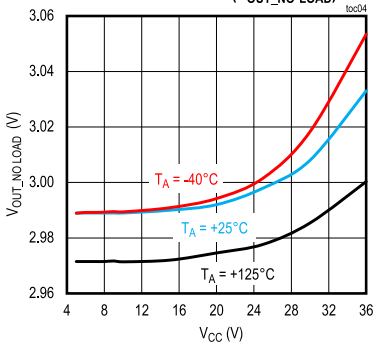
SUPPLY CURRENT (I_{SB}) vs. TEMPERATURE



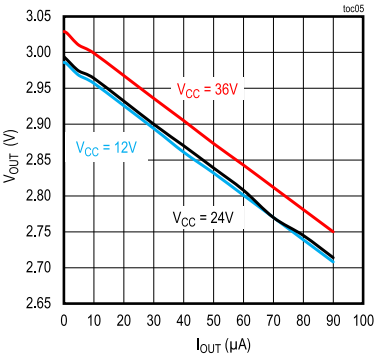
DEBOUNCE TIME vs. TEMPERATURE



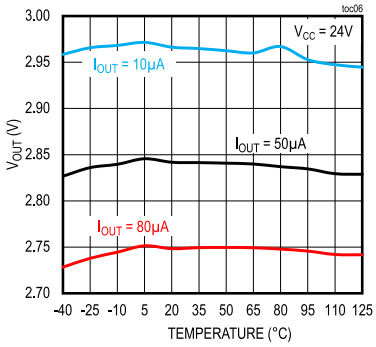
SUPPLY VOLTAGE (V_{CC}) vs. OUTPUT VOLTAGE ($V_{OUT\_NO\ LOAD}$)



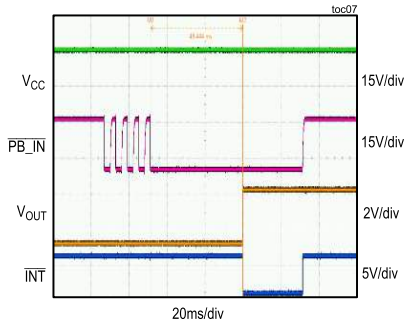
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



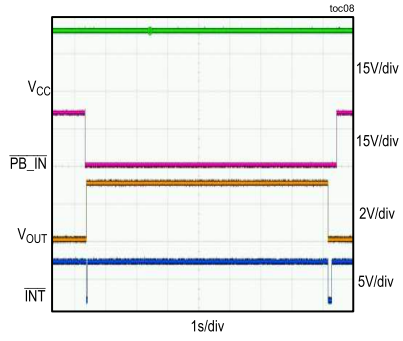
OUTPUT VOLTAGE (V_{OUT}) vs. TEMPERATURE



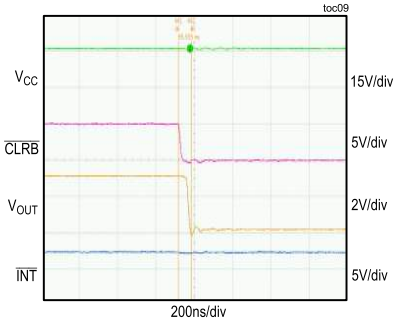
SWITCH DEBOUNCE TO OUT ASSERTION



SWITCH DEBOUNCE TO OUT DEASSERTION

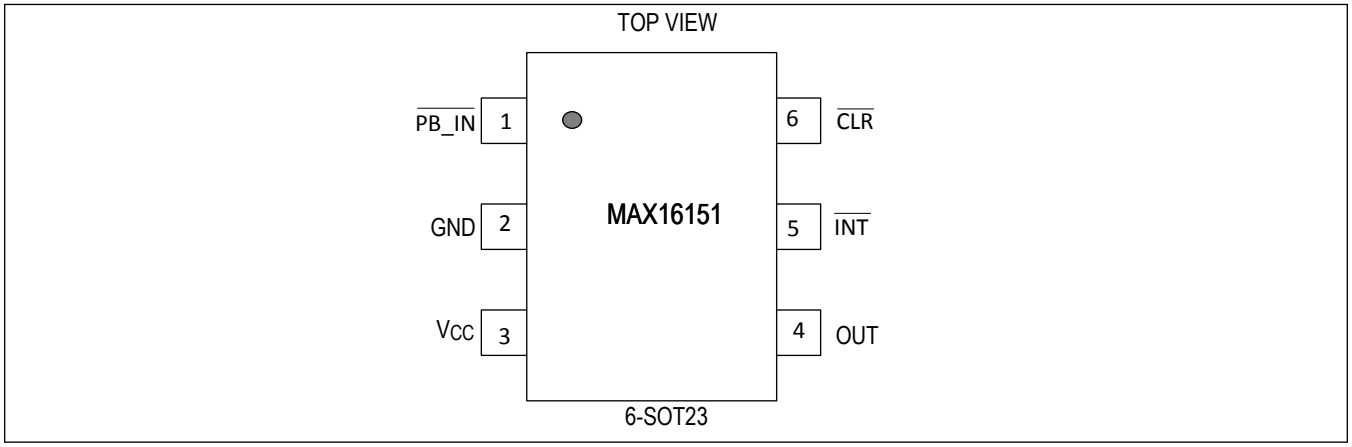


CLR TO OUT PROPAGATION DELAY

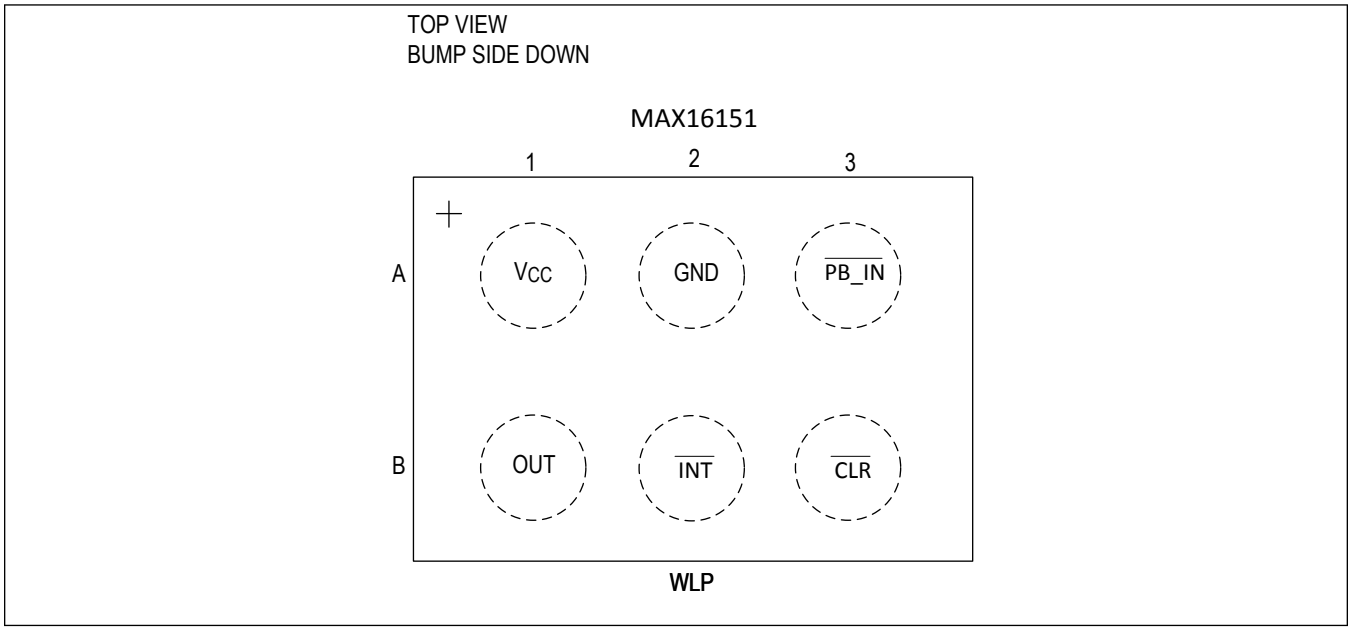


Pin Configurations

SOT23-6



6 WLP

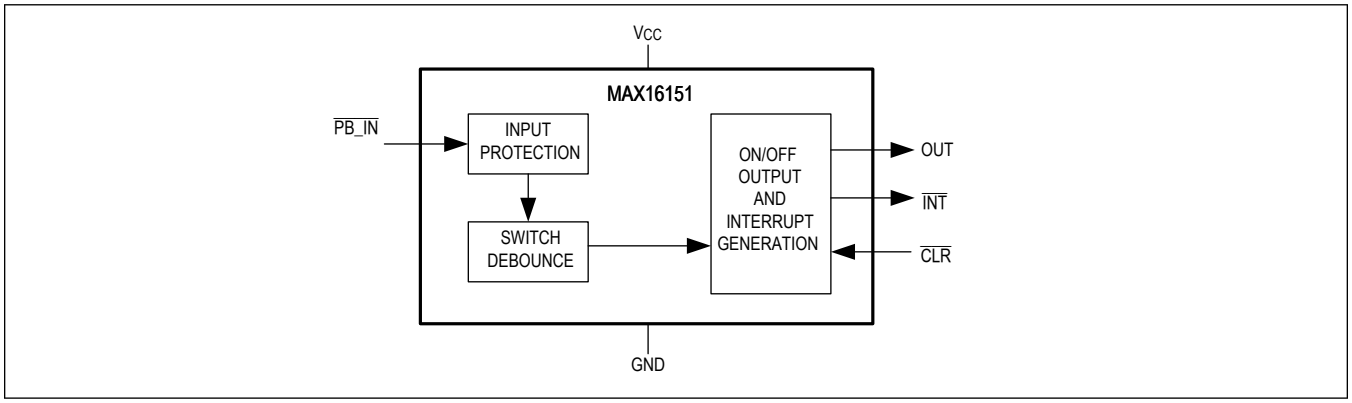


Pin Description

PIN		NAME	FUNCTION
SOT23-6	6 WLP		
3	A1	V_{CC}	Power supply input. Bypass with a 0.1µF capacitor to ground.
2	A2	GND	Ground.
1	A3	$\overline{PB\_IN}$	Pushbutton Input. $\overline{PB\_IN}$ is internally pulled up to V_{CC}. Holding $\overline{PB\_IN}$ low for a period greater than the debounce time (t_{DB}) forces OUT to latch high and generate a one-shot pulse at $\overline{INT}$. A MAX16151 $\overline{PB\_IN}$ switch closure longer than the shutdown period results in a longer one-shot pulse at $\overline{INT}$. The MAX16151A deasserts the latched output when the switch closure period exceeds the shutdown period, while the MAX16151B does not deassert the latched output.
6	B3	$\overline{CLR}$	Clear input. Pulling $\overline{CLR}$ low deasserts the latched OUT signal. If OUT is deasserted, pulling $\overline{CLR}$ does not change OUT's state.
5	B2	$\overline{INT}$	Active-Low, Open-Drain Interrupt Output. $\overline{INT}$ is a one-shot output pulse. $\overline{INT}$ asserts for the interrupt timeout period when $\overline{PB\_IN}$ is held low for a period greater than the debounce time (t_{DB}). $\overline{INT}$ is high impedance when deasserted, even when pulled up to external voltage.
4	B1	OUT	Active-High, Push-Pull Latch Output. The OUT is internally connected to a 3V regulator.

Functional Diagrams

Block Diagram



Detailed Description

The MAX16151 is a pushbutton on/off controller with a switch debouncer and latched output for controlling system power. A switch closure that pulls PB_IN low and is stable for a period greater than or equal to the debounce time (t_{DB}) causes OUT to assert high. Driving CLR low causes OUT to deassert. For the MAX16151A, a switch closure period greater than or equal to the shutdown period (t_{SO}) causes OUT to deassert. Each debounced switch closure also initiates a one-shot INT output. See Table 1 for details on the values of t_{DB}, t_{SO}, and other timing intervals.

Table 1. MAX16151 Input Timing Characteristics

VERSION*	DEBOUNCE TIME (t_{DB})	SHUTDOWN PERIOD (t_{SO})	INTERRUPT PERIOD (SWITCH CLOSURE > t_{DB})	INTERRUPT PERIOD (SWITCH CLOSURE > t_{SO})	SWITCH CLOSURE > t_{SO}
MAX16151A	50ms	8s	32ms	128ms	OUT de-asserts
MAX16151B	2s	16s	32ms	128ms	OUT stays asserted

*Versions with different combinations of timing parameters are available. Contact factory for availability.

MAX16151 Operation

The MAX16151 operates from supply voltages between +5V and +36V. The pushbutton input is active-low. While awaiting a switch closure when OUT is deasserted, the power supply current is less than 15µA. After asserting OUT, CLR continues to be ignored for CLR lockout time (2x of the INT period). If OUT is already deasserted when CLR is pulled low the state of OUT is unchanged. CLR input will not affect the INT. Each debounced switch closure causes INT to assert a switch closure longer than t_{SO} results in INT, asserting for a period that is 4 times longer than the nominal INT period. This longer INT can be used to signal the system to perform a specific function or to initiate a shutdown process. Closing the switch longer than this extended INT period does not cause further assertion of INT.

The MAX16151A deasserts OUT when PB_IN is held low for a period equal to or greater than the shutdown time, t_{SO}. Holding PB_IN low for a duration less than t_{SO} does not deassert OUT. In the MAX16151B, holding PB_IN low for a period of equal to or greater than tSO does not deassert OUT.

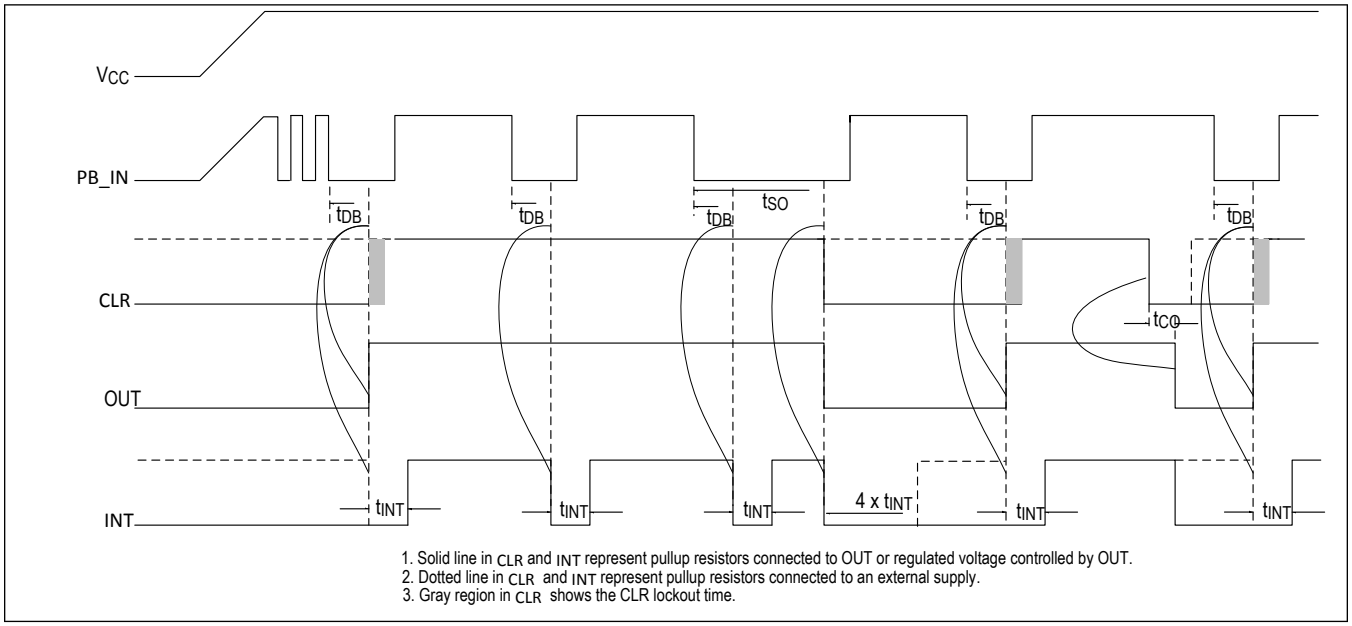


Figure 1. MAX16151A Timing Diagram with Long Pushbutton (tSO) Causes OUT to Deassert

In the MAX16151A diagram above (Figure 1), a switch closure of a duration greater than t_{DB} causes OUT to assert. A switch closure of a duration greater than t_{SO} causes OUT to deassert. Typically, $\overline{INT}$ and $\overline{CLR}$ are pulled up either to OUT or to a regulated voltage controlled by OUT, as depicted in the MAX16151B diagram below (Figure 2). As such, $\overline{INT}$ and $\overline{CLR}$ are pulled low while OUT is deasserted. If $\overline{INT}$ and $\overline{CLR}$ are pulled up to a constant supply voltage, they behave as shown by the horizontal dashed lines while OUT is deasserted.

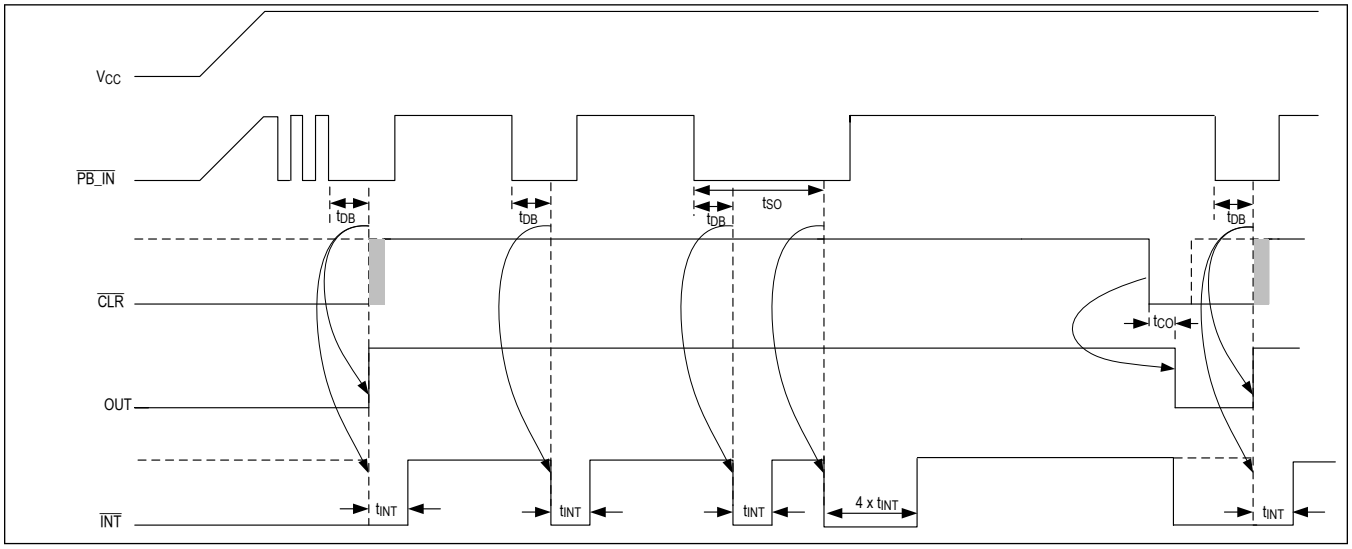


Figure 2. MAX16151B Timing Diagram with Long Pushbutton (tSO) Keeps OUT Asserted

In the MAX16151B diagram above (Figure 2), a switch closure of a duration greater than t_{DB} causes OUT to assert. A switch closure of a duration greater than t_{SO} does not cause OUT to deassert but does cause an extended interrupt.

Robust Switch Input

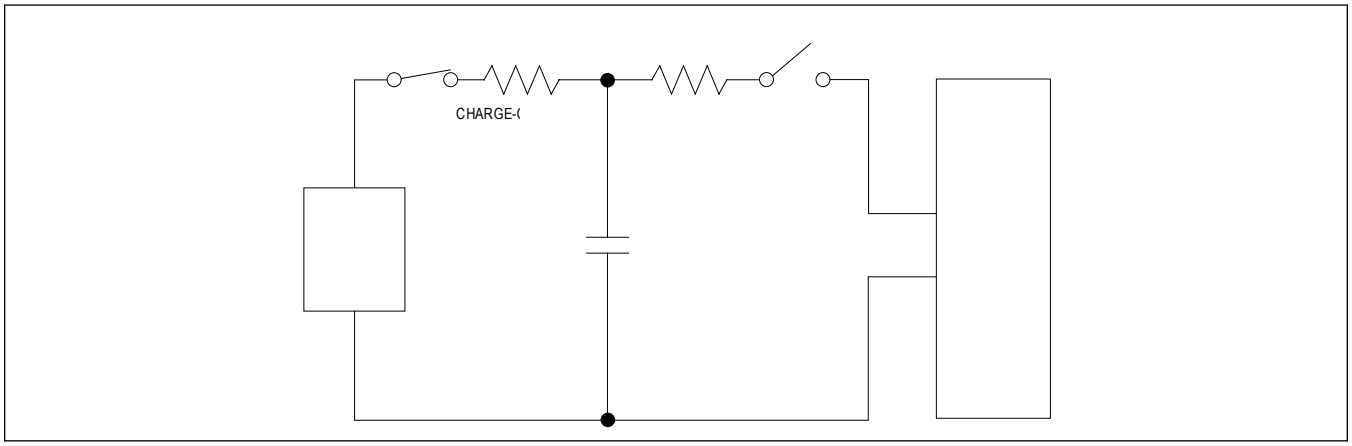
The switch input ($\overline{PB\_IN}$) includes overvoltage clamping diodes to protect against damaging fault conditions. Switch input voltages can safely swing ±60V relative to ground.

±10kV ESD Protection

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The MAX16151 includes additional protection against static electricity to protect against ESD of ±10kV at the switch input. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. A design advantage of these devices is that they continue working without latchup after an ESD event, which eliminates the need to power-cycle the device. ESD protection can be tested in various ways; this product is characterized for protection of ±10kV using the Human Body Model.

Human Body Model

Figure 3 shows the Human Body Model, while Figure 4 shows the current waveform it generates when discharged into a low-impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

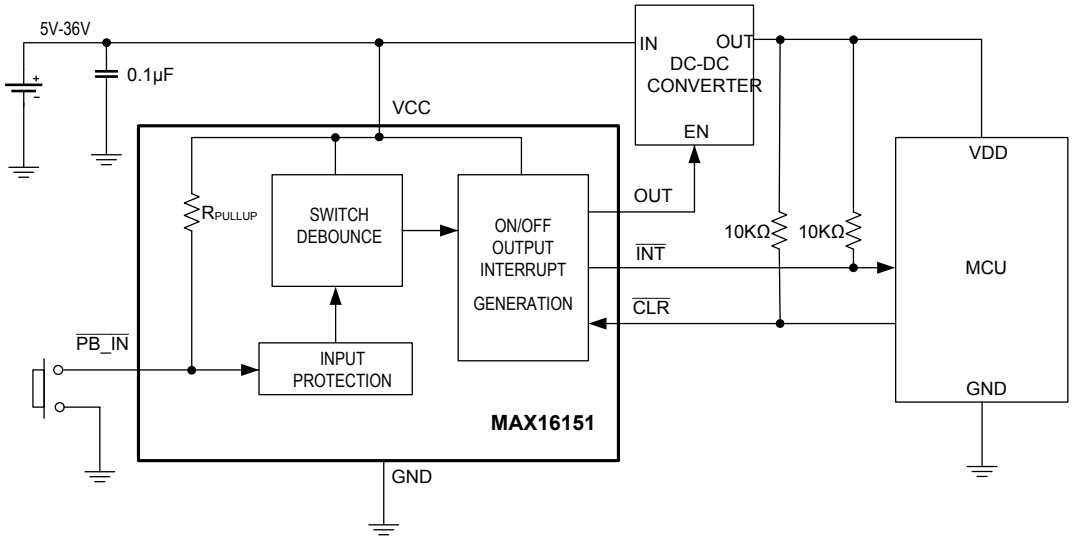

CHARGE-(

Applications Information

Powering the Load

The MAX16151 OUT has an internal 3V regulator that can be directly connected to a light load (typical 50uA). For a system requiring higher power, the output of the MAX16151 can be used as an enable signal for the voltage regulator powering the system. This Typical Application Circuit shows an LDO providing power to the load. The LDO's enable input is driven by OUT of the MAX16151. A debounced pushbutton at PB_IN of the MAX16151 causes OUT to assert high, thereby enabling the LDO.

Typical Application Circuits



SWITCH DEBOUNCER/FRESHNESS SEAL PROVIDING ENABLE SIGNAL TO DC-DC CONVERTER

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX16151AWT+T	-40ºC to +125ºC	6-WLP
MAX16151BWT+T*	-40ºC to +125ºC	6-WLP
MAX16151_WT+T*	-40ºC to +125ºC	6-WLP
MAX16151_UT+T*	-40ºC to +125ºC	6 SOT23

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

** Denotes future products*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/21	Release for Market Intro.	—