1 MSPS, Ultralow Power, 12-Bit ADC in 10-Lead LFCSP and MSOP

Data Sheet **AD7091R**

FEATURES

- Fast throughput rate of 1 MSPS
- Specified for V_{DD} of 2.7 V to 5.25 V
- Logic voltage V_{DRIVE} of 1.65 V to 5.25 V
- INL of ±1 LSB maximum
- Analog input range of 0 V to V_{REF}
- Ultralow power
  - 349 µA typical at 3 V and 1 MSPS
  - 264 nA typical at 3 V in power-down mode
- Internal 2.5 V reference, ±4.5 ppm/°C typical drift
- Wide input bandwidth
- Flexible power/throughput rate management
- High speed serial interface
  - SPI®/QSPI™/MICROWIRE™/DSP compatible
- BUSY indicator
- Power-down mode
- 10-lead, 3 mm × 2 mm LFCSP and 10-lead MSOP packages
- Temperature range of −40°C to +125°C

APPLICATIONS

- Battery-powered systems
  - Handheld meters
  - Medical instruments
  - Mobile communications
- Instrumentation and control systems
- Data acquisition systems
- Optical sensors
- Diagnostic/monitoring functions
- Energy harvesting

GENERAL DESCRIPTION

The AD7091R is a 12-bit successive approximation analog-to-digital converter (ADC) that offers ultralow power consumption (typically 349 µA at 3 V and 1 MSPS) while achieving fast throughput rates (1 MSPS with a 50 MHz SCLK). Operating from a single 2.7 V to 5.25 V power supply, the part contains a wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 7 MHz. The AD7091R also features an on-chip conversion clock, accurate reference, and high speed serial interface.

The conversion process and data acquisition are controlled using a $\overline{\text{CONVST}}$ signal and an internal oscillator. The AD7091R has a serial interface that allows data to be read after the conversion while achieving a 1 MSPS throughput rate.

FUNCTIONAL BLOCK DIAGRAM

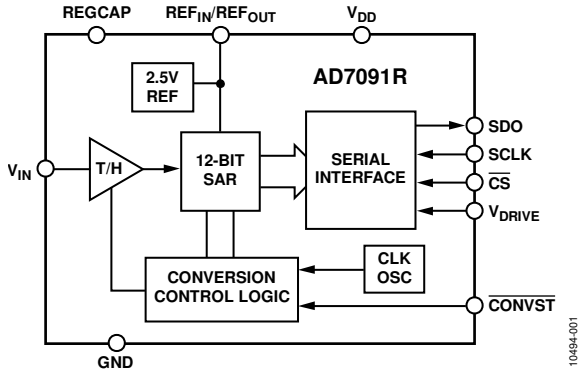

Figure 1.

The AD7091R uses advanced design and process techniques to achieve very low power dissipation at high throughput rates. An on-chip, accurate 2.5 V reference is available.

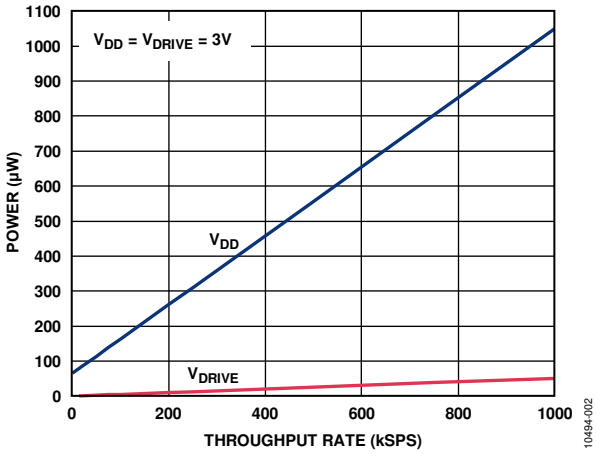

Figure 2. Power vs. Throughput Rate

PRODUCT HIGHLIGHTS

1. Lowest Power 12-Bit SAR ADC Available.
2. On-Chip, Accurate 2.5 V Reference.
3. High Throughput Rate with Ultralow Power Consumption.
4. Flexible Power/Throughput Rate Management.
   Average power scales with the throughput rate. Power-down mode allows the average power consumption to be reduced when the device is not performing a conversion.
5. Single Supply Operation with V_{DRIVE} Function.
   The AD7091R operates from a single 2.7 V to 5.25 V supply. The V_{DRIVE} function allows the serial interface to connect directly to 1.8 V to 3.3 V processors.

Rev. B Document Feedback

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REVISION HISTORY

9/2016—Rev. A to Rev. B

Changes to Signal-to-Noise Ratio (SNR) Parameter and Integral Nonlinearity Parameter, Table 1 ... 3
Deleted Note 3, Table 1 ... 3

5/2015—Rev. 0 to Rev. A

Changes to Serial Interface Section ... 16

8/2012—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.25 V, V_{DRIVE} = 1.65 V to 5.25 V, V_{REF} = 2.5 V internal reference, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 50 MHz, T_A = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE[1]	f_{IN} = 10 kHz sine wave				
Signal-to-Noise Ratio (SNR)[2]		66.5	69		dB
	f_{SAMPLE} = 500 kSPS	67.0	70		dB
Signal-to-Noise-and-Distortion Ratio (SINAD)[2]		66	69		dB
Total Harmonic Distortion (THD)[2]			−84	−79	dB
Spurious Free Dynamic Range (SFDR)[2]			−85	−78	dB
Aperture Delay[2]			5		ns
Aperture Jitter[2]			40		ps
Full Power Bandwidth[2]	At −3 dB		7.5		MHz
	At −0.1 dB		1.2		MHz
DC ACCURACY					
Resolution		12			Bits
Integral Nonlinearity (INL)[2]			±0.8	±1	LSB
Differential Nonlinearity (DNL)[2]	Guaranteed no missing codes to 12 bits		±0.3	±0.9	LSB
Offset Error[2]			±0.6	±2	LSB
Gain Error[2]			±0.8	±3	LSB
Total Unadjusted Error (TUE)[2]			−2		LSB
ANALOG INPUT					
Input Voltage Range		0		V_{REF}	V
DC Leakage Current				±1	µA
Input Capacitance[3]					
	During acquisition phase		7		pF
	Outside acquisition phase		1		pF
VOLTAGE REFERENCE INPUT/OUTPUT					
REF_{OUT}		2.485	2.5	2.525	V
REF_{IN}		2.7		V_{DD}	V
Drift			±4.5	±25	ppm/°C
LOGIC INPUTS					
Input High Voltage (V_{INH})		0.7 × V_{DRIVE}			V
Input Low Voltage (V_{INL})				0.3 × V_{DRIVE}	V
Input Current (I_{IN})	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}			±1	µA
Input Capacitance (C_{IN})[3]				5	pF
LOGIC OUTPUTS					
Output High Voltage (V_{OH})	I_{SOURCE} = 200 µA	V_{DRIVE} − 0.2			V
Output Low Voltage (V_{OL})	I_{SINK} = 200 µA			0.4	V
Floating State Leakage Current				±1	µA
Floating State Output Capacitance[3]				5	pF
Output Coding			Straight binary		
CONVERSION RATE					
Conversion Time				650	ns
Track-and-Hold Acquisition Time[2, 3]	Full-scale step input			350	ns
Throughput Rate				1	MSPS
POWER REQUIREMENTS					
V_{DD}		2.7		5.25	V
V_{DRIVE}		1.65		5.25	V
I_{DD}	V_{IN} = 0 V				
Normal Mode—Static[4]					

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	V_{DD} = 5.25 V		22	60	µA
	V_{DD} = 3 V		21.6	33	µA
Normal Mode—Operational					
	V_{DD} = 5.25 V, f_{SAMPLE} = 1 MSPS		388	449	µA
	V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS		349	408	µA
	V_{DD} = 3 V, f_{SAMPLE} = 100 kSPS		55		µA
Power-Down Mode					
	V_{DD} = 5.25 V		0.334	4.4	µA
	V_{DD} = 5.25 V, T_A = −40°C to +85°C		0.334	1.4	µA
	V_{DD} = 3 V		0.264	4.2	µA
	V_{DD} = 3 V, T_A = −40°C to +85°C		0.264	1.2	µA
I_{DRIVE}	V_{IN} = 0 V				
Normal Mode—Static[5]					
	V_{DRIVE} = 5.25 V		32	500	nA
	V_{DRIVE} = 3 V		28	500	nA
Normal Mode—Operational					
	V_{DRIVE} = 5.25 V, f_{SAMPLE} = 1 MSPS		42	86	µA
	V_{DRIVE} = 3 V, f_{SAMPLE} = 1 MSPS		17	20	µA
Power-Down Mode					
	V_{DRIVE} = 5.25 V		7	41	nA
	V_{DRIVE} = 3 V		2	28	nA
Total Power Dissipation (P_{DD} + P_{DRIVE})	V_{IN} = 0 V				
Normal Mode—Static[4]					
	V_{DD} = V_{DRIVE} = 5.25 V		116	318	µW
	V_{DD} = V_{DRIVE} = 3 V		65	101	µW
Normal Mode—Operational					
	V_{DD} = V_{DRIVE} = 5.25 V, f_{SAMPLE} = 1 MSPS		2.3	2.9	mW
	V_{DD} = V_{DRIVE} = 3 V, f_{SAMPLE} = 1 MSPS		1	1.3	mW
Power-Down Mode					
	V_{DD} = V_{DRIVE} = 5.25 V		1.8	24	µW
	V_{DD} = V_{DRIVE} = 3 V		0.8	13	µW

[1] Dynamic performance is achieved with a burst SCLK. Operating a free running SCLK during acquisition phase degrades dynamic performance.
[2] See the Terminology section.
[3] Sample tested during initial release to ensure compliance.
[4] SCLK is operating in burst mode and $\overline{CS}$ is idling high. With a free running SCLK and $\overline{CS}$ pulled low, the I_{DD} static current is increased by 30 µA typical at V_{DD} = 5.25 V.
[5] SCLK is operating in burst mode and $\overline{CS}$ is idling high. With a free running SCLK and $\overline{CS}$ pulled low, the I_{DRIVE} static current is increased by 32 µA typical at V_{DRIVE} = 5.25 V.

TIMING SPECIFICATIONS

V_{DD} = 2.75 V to 5.25 V, V_{DRIVE} = 1.65 V to 5.25 V, T_A = −40°C to +125°C, unless otherwise noted.[1]

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCLK}	50	MHz max	Frequency of serial read clock
t_1	8	ns max	Delay from the end of a conversion until SDO three-state is disabled
t_2	7	ns max	Data access time after SCLK falling edge
t_3	0.4 t_{SCLK}	ns min	SCLK high pulse width
t_4	3	ns min	SCLK to data valid hold time
t_5	0.4 t_{SCLK}	ns min	SCLK low pulse width
t_6	15	ns max	SCLK falling edge to SDO high impedance
t_7	10	ns min	$\overline{CONVST}$ pulse width
t_8	650	ns max	Conversion time
t_9	6	ns min	$\overline{CS}$ low time before the end of a conversion
t_{10}	18	ns max	Delay from $\overline{CS}$ until SDO three-state is disabled
t_{11}	8	ns min	$\overline{CS}$ high time before the end of a conversion
t_{12}	8	ns min	Delay from the end of a conversion until $\overline{CS}$ falling edge
t_{13}	50	ms typ	Power-up time with internal reference[2]
	100	µs max	Power-up time with external reference
t_{QUIET}	50	ns min	Time between last SCLK edge and next $\overline{CONVST}$ pulse

[1] Sample tested during initial release to ensure compliance.
[2] With a 2.2 µF reference capacitor.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{DRIVE} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to V_{REF} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DRIVE} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
ESD	
HBM	±2.5 kV
FICDM	±1.5 kV

[1] Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

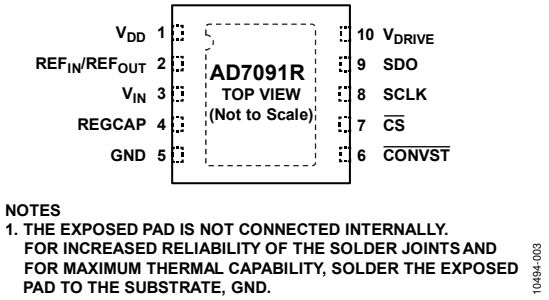
Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
10-Lead LFCSP	33.2	4	°C/W
10-Lead MSOP	25.67	1.67	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD IS NOT CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND FOR MAXIMUM THERMAL CAPABILITY, SOLDER THE EXPOSED PAD TO THE SUBSTRATE, GND.

Figure 3. Pin Configuration, 10-Lead LFCSP

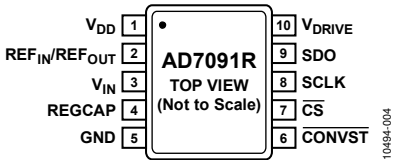


Figure 4. Pin Configuration, 10-Lead MSOP

Table 5. Pin Function Descriptions

Pin No.			
LFCSP	**MSOP**	**Mnemonic**	**Description**
1	1	V_{DD}	Power Supply Input. The V_{DD} range is from 2.7 V to 5.25 V. This supply pin should be decoupled to GND. The typical recommended values are 10 µF and 0.1 µF.
2	2	REF_{IN}/REF_{OUT}	Voltage Reference Input Output. Decouple this pin to GND. The typical recommended decoupling capacitor value is 2.2 µF. The user can either access the internal 2.5 V reference or overdrive the internal reference with an externally applied voltage. The reference voltage range for an externally applied reference is 2.7 V to V_{DD}.
3	3	V_{IN}	Analog Input. The single-ended analog input range is from 0 V to V_{REF}.
4	4	REGCAP	Decoupling Capacitor Pin for Voltage Output from Internal Regulator. This output pin should be decoupled separately to GND using a 1 µF capacitor. The voltage at this pin is 1.8 V typical.
5	5	GND	Analog Ground. This pin is the ground reference point for all circuitry on the AD7091R. The analog input signal should be referred to this GND voltage.
6	6	$\overline{CONVST}$	Convert Start. Active low edge triggered logic input. The falling edge of $\overline{CONVST}$ places the track-and-hold into hold mode and initiates a conversion.
7	7	$\overline{CS}$	Chip Select. Active low logic input. The serial bus is enabled when $\overline{CS}$ is held low, and in this mode $\overline{CS}$ is used to frame the output data on the SPI bus.
8	8	SCLK	Serial Clock. This pin acts as the serial clock input.
9	9	SDO	Serial Data Output. The conversion output data is supplied to this pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data is provided MSB first.
10	10	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines the operating voltage of the interface. Decoupling capacitors should be connected between V_{DRIVE} and GND. The typical recommended values are 10 µF and 0.1 µF. The voltage range of this pin is 1.65 V to 5.25 V.
11	N/A	EPAD	Exposed Pad. The exposed pad is not connected internally. For increased reliability of the solder joints and for maximum thermal capability, solder the exposed pad to the substrate, GND.

TYPICAL PERFORMANCE CHARACTERISTICS

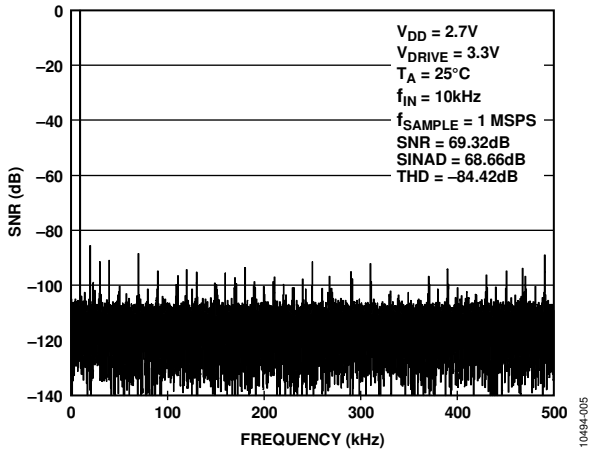


Figure 5. Typical Dynamic Performance

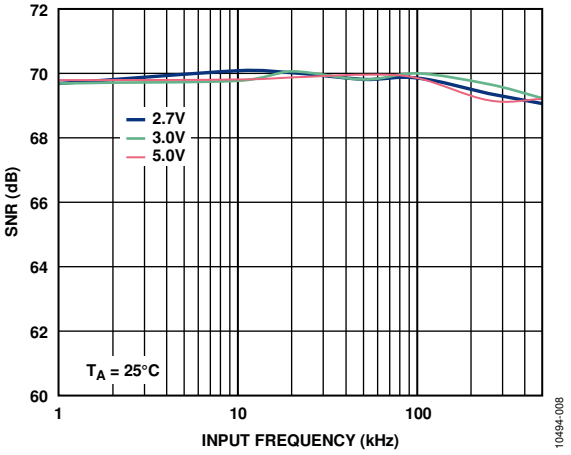


Figure 8. SNR vs. Analog Input Frequency for Various Supply Voltages

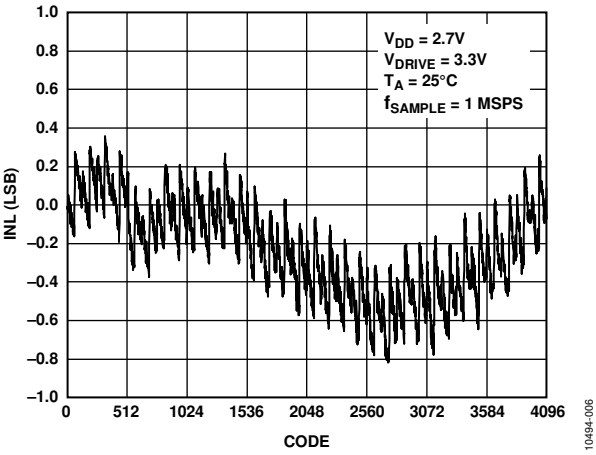


Figure 6. Typical INL Performance

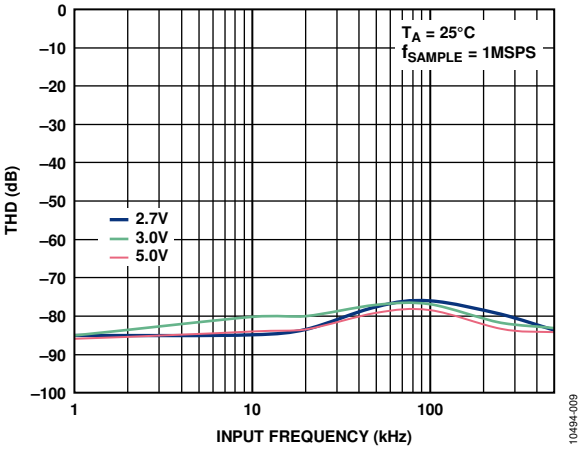


Figure 9. THD vs. Analog Input Frequency for Various Supply Voltages

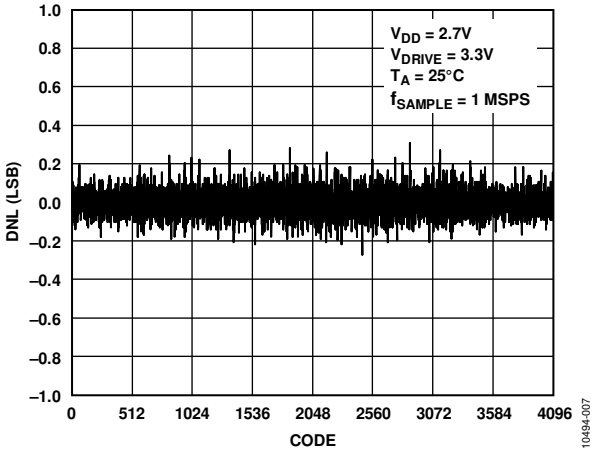


Figure 7. Typical DNL Performance

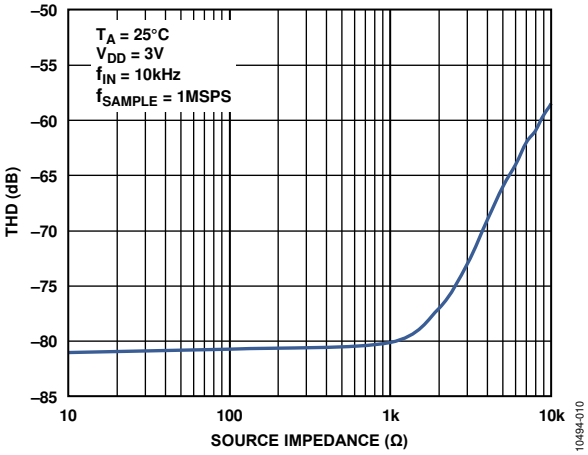


Figure 10. THD vs. Source Impedance

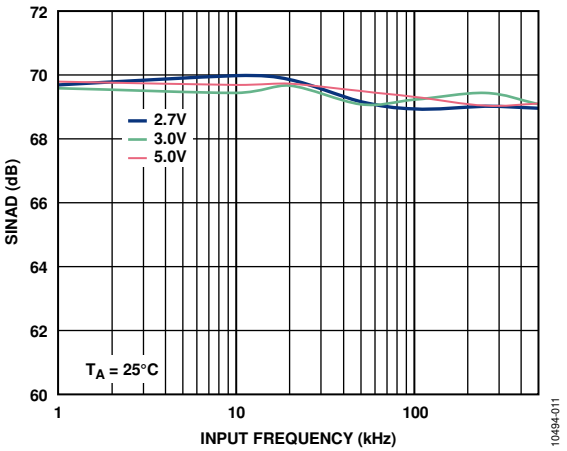


Figure 11. SINAD vs. Analog Input Frequency for Various Supply Voltages

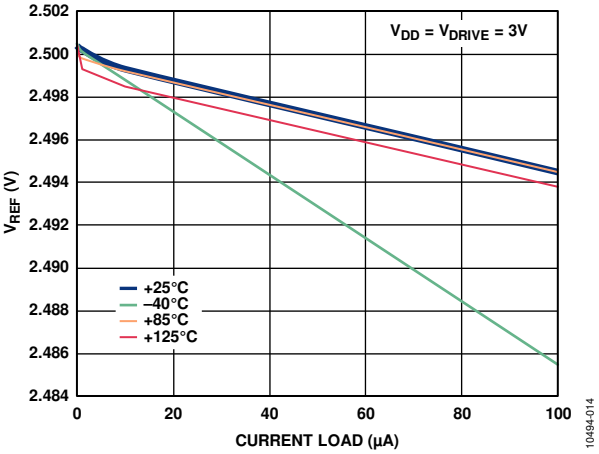


Figure 14. Reference Voltage Output vs. Current Load for Various Temperatures

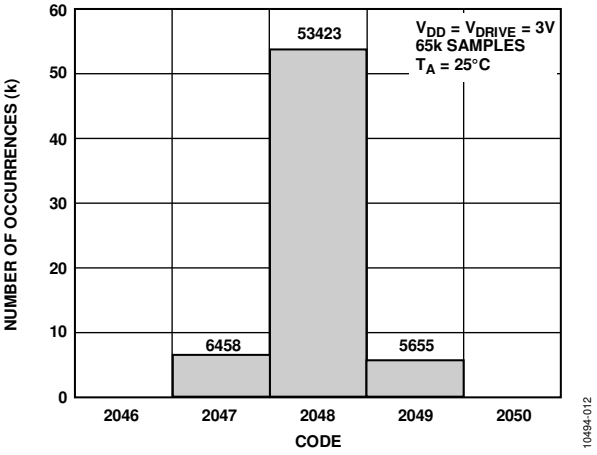


Figure 12. Histogram of Codes at Code Center (V_{REF}/2)

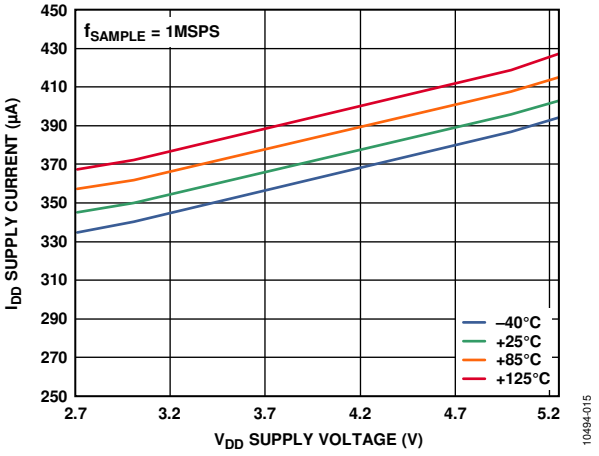


Figure 15. Operational I_{DD} Supply Current vs. V_{DD} Supply Voltage for Various Temperatures

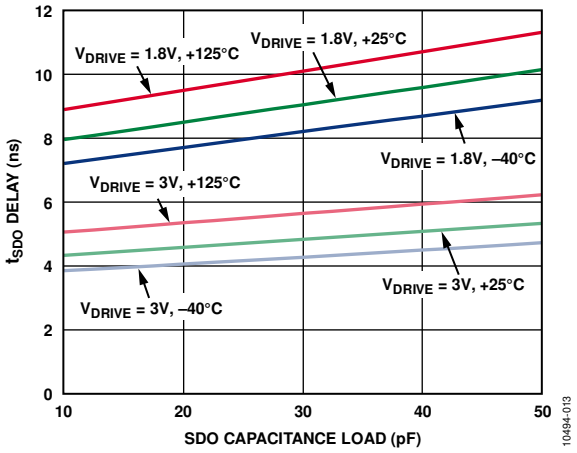


Figure 13. t_{SDO} Delay vs. SDO Capacitance Load and V_{DRIVE}

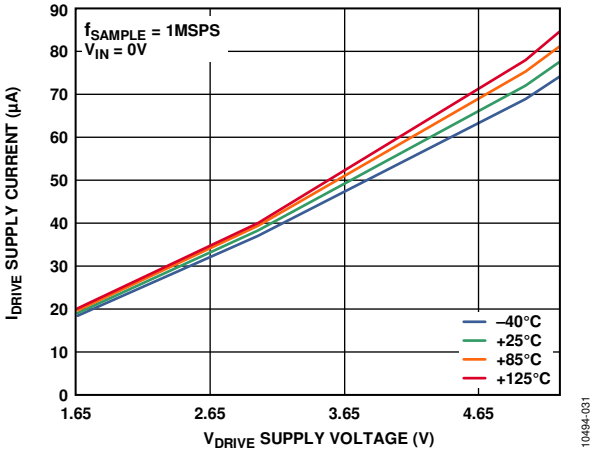


Figure 16. Operational I_{DRIVE} Supply Current vs. V_{DRIVE} Supply Voltage for Various Temperatures

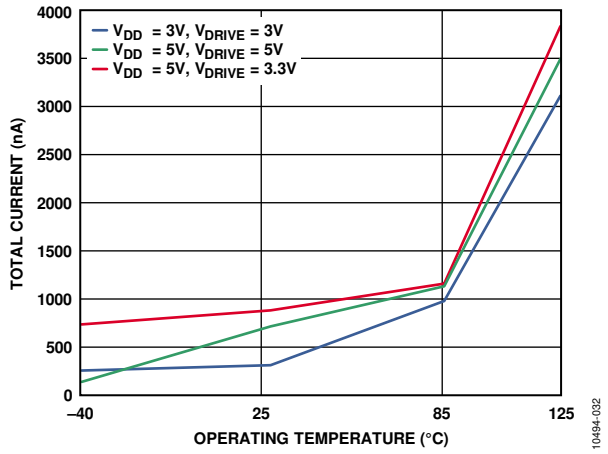


Figure 17. Total Power-Down Supply Current (I_{DD} and I_{DRIVE}) vs. Temperature for Various Supply Voltages

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. For the AD7091R, the endpoints of the transfer function are zero scale (a point 0.5 LSB below the first code transition) and full scale (a point 0.5 LSB above the last code transition).

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
Offset error is the deviation of the first code transition (00 ... 000) to (00 ... 001) from the ideal (such as GND + 0.5 LSB).

Gain Error
Gain error is the deviation of the last code transition (111 ... 110) to (111 ... 111) from the ideal (such as V_{REF} − 1.5 LSB) after the offset error has been adjusted out.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode after the end of a conversion. The track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±0.5 LSB, after a conversion (see the Serial Interface section for more details).

Signal-to-Noise Ratio (SNR)
SNR is the measured ratio of signal to noise at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_{SAMPLE}/2$), excluding dc.

The ratio is dependent on the number of quantization levels in the digitization process: the more levels, the smaller the quantization noise. The theoretical signal-to-noise ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}Noise\ Ratio = (6.02N + 1.76)\ \text{dB}$$

Therefore, for a 12-bit converter, the SNR is 74 dB.

Signal-to-Noise-and-Distortion Ratio (SINAD)
SINAD is the measured ratio of signal to noise and distortion at the output of the ADC. The signal is the rms value of the sine wave, and noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_{SAMPLE}/2$), including harmonics, but excluding dc.

Total Unadjusted Error (TUE)
TUE is a comprehensive specification that includes the gain, linearity, and offset errors.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7091R, THD is defined as

$$THD\ (\text{dB}) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Spurious Free Dynamic Range (SFDR)
SFDR, also known as peak harmonic or spurious noise, is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_{SAMPLE}/2$ and excluding dc) to the rms value of the fundamental. Usually, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, the largest harmonic would be a noise peak.

Aperture Delay
Aperture delay is the measured interval between the leading edge of the sampling clock and the point at which the ADC samples data.

Aperture Jitter
Aperture jitter is the sample-to-sample variation in the effective point in time at which the data is sampled.

Full Power Bandwidth
Full power bandwidth is the input frequency at which the amplitude of the reconstructed fundamental is reduced by 0.1 dB or 3 dB for a full-scale input.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7091R is a 12-bit successive approximation analog-to-digital converter (ADC) that offers ultralow power consumption (typically 349 µA at 3 V and 1 MSPS) while achieving fast throughput rates (1 MSPS with a 50 MHz SCLK). The part can be operated from a single power supply in the range of 2.7 V to 5.25 V.

The AD7091R provides an on-chip track-and-hold ADC with a serial interface housed in a tiny 10-lead LFCSP and 10-lead MSOP packages. These packages offer considerable space-saving advantages compared with alternative solutions. The serial clock input accesses data from the part. The clock for the successive approximation ADC is generated internally. The reference voltage for the AD7091R is generated internally by an accurate on-chip reference source. The analog input range for the AD7091R is 0 V to V_{REF}.

The AD7091R also features a power-down option to save power between conversions. The power-down feature is implemented across the standard serial interface as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7091R is a successive approximation ADC based around a charge redistribution DAC. Figure 18 and Figure 19 show simplified schematics of the ADC. Figure 18 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A, the comparator is held in a balanced condition, and the sampling capacitor acquires the signal on V_{IN}.

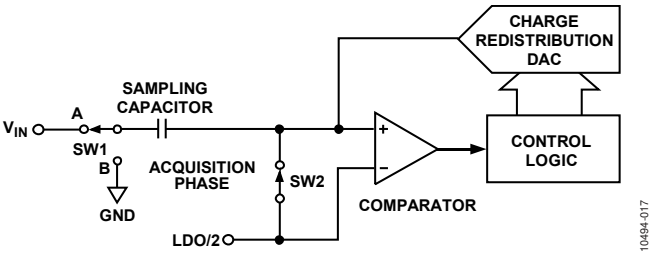


Figure 18. ADC Acquisition Phase

When the ADC starts a conversion, SW2 opens and SW1 moves to Position B (see Figure 19), causing the comparator to become unbalanced. The control logic and the charge redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 20 show the ideal ADC transfer function.

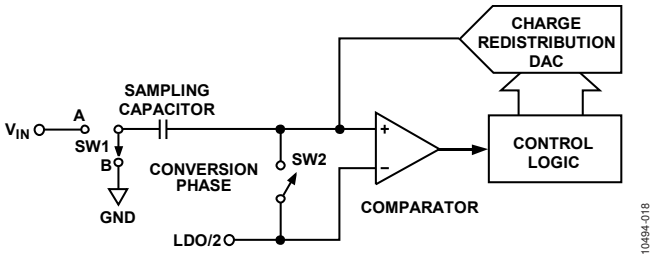


Figure 19. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding of the AD7091R is straight binary. The designed code transitions occur midway between successive integer LSB values, such as 0.5 LSB, 1.5 LSB, and so on. The LSB size for the AD7091R is $V_{REF}/4096$. The ideal transfer characteristics for the AD7091R are shown in Figure 20.

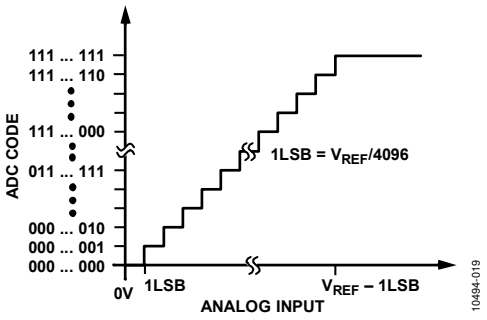


Figure 20. AD7091R Ideal Transfer Characteristics

INTERNAL/EXTERNAL VOLTAGE REFERENCE

The AD7091R allows the choice of an internal voltage reference or an external voltage reference.

The internal reference provides an accurate 2.5 V low temperature drift voltage reference. The internal reference is available at the REF_{IN}/REF_{OUT} pin. When using the internal reference, this pin should be decoupled using a capacitor with a typical value of 2.2 µF to achieve the specified performance. With a fully discharged 2.2 µF reference capacitor, the internal reference requires 50 ms typically to fully charge to the 2.5 V REF_{OUT} voltage level.

In power-down mode, the internal voltage reference is shut down. After exiting power-down mode, adequate time should be allowed for the reference capacitor to recharge before performing a conversion. The time required to recharge the reference capacitor is dependent on the amount of charge remaining on the capacitor when exiting power-down mode.

If the on-chip reference is used externally to the AD7091R, it is recommended to buffer this reference before supplying the external circuitry.

Alternatively, the AD7091R reference voltage can be applied externally. If an external reference is applied to the device, the internal reference is automatically overdriven. An externally applied reference voltage should be in the range of 2.7 V to 5.25 V and should be connected to the REF_{IN}/REF_{OUT} pin.

TYPICAL CONNECTION DIAGRAM

Figure 22 shows a typical connection diagram for the AD7091R.

A positive power supply in the range of 2.7 V to 5.25 V should be connected to the V_{DD} pin, with typical values for decoupling capacitors being 100 nF and 10 µF. These capacitors should be placed as close as possible to the device pins. With the power supply connected to the V_{DD} pin, the AD7091R operates with the internal 2.5 V reference, and the REF_{IN}/REF_{OUT} pin should be decoupled using a capacitor with a typical value of 2.2 µF to achieve the specified performance and provide an analog input range of 0 V to V_{REF}. The typical value for the regulator bypass decoupling capacitor (REGCAP) is 1 µF. The voltage applied to the V_{DRIVE} input controls the voltage of the serial interface; therefore, this pin should be connected to the supply voltage of the microprocessor. V_{DRIVE} can be set in the range of 1.65 V to 5.25 V. Typical values for the V_{DRIVE} decoupling capacitors are 100 nF and 10 µF. The conversion result is output in a 12-bit word with the MSB first.

The AD7091R requires the user to initiate a software reset upon power-up (see the Software Reset section).

If an external reference is applied to the device, the internal reference is automatically overdriven. An externally applied reference voltage should be in the range of 2.7 V to 5.25 V and should be connected to the REF_{IN}/REF_{OUT} pin.

If the BUSY indicator feature is required, a pull-up resistor of typically 100 kΩ to V_{DRIVE} should be connected to the SDO pin. In addition, for applications in which power consumption is a concern, the power-down mode can be used to improve the power performance of the ADC (see the Modes of Operation section for more details).

ANALOG INPUT

Figure 21 shows an equivalent circuit of the AD7091R analog input structure. The D1 and D2 diodes provide ESD protection for the analog input. The D3 diode is a parasitic diode between V_{IN} and V_{REF}. To prevent the diodes from becoming forward-biased and from starting to conduct current, ensure that the analog input signal never exceeds V_{REF} or V_{DD} by more than 300 mV. These diodes can conduct a maximum of 10 mA without causing irreversible damage to the part.

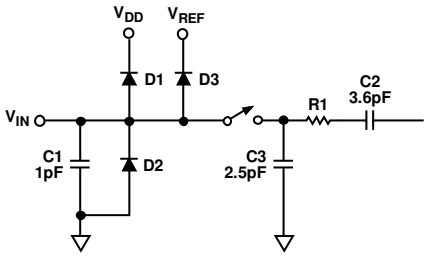


Figure 21. Equivalent Analog Input Circuit

Capacitor C1 in Figure 21 is typically about 1 pF and can primarily be attributed to pin capacitance. Resistor R1 is a lumped component made up of the on resistance of a switch. This resistor is typically about 500 Ω. Capacitor C2 is the ADC sampling capacitor and typically has a capacitance of 3.6 pF.

In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This may necessitate using an input buffer amplifier as shown in Figure 22. The choice of the op amp is a function of a particular application.

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD increases as the source impedance increases and performance degrades. Figure 10 shows a graph of THD vs. source impedance when using a supply voltage of 3 V and a sampling rate of 1 MSPS.

Use an external filter—such as a one-pole, low-pass RC filter, or similar, as shown in Figure 22—on the analog input connected to the AD7091R to achieve the specified performances.

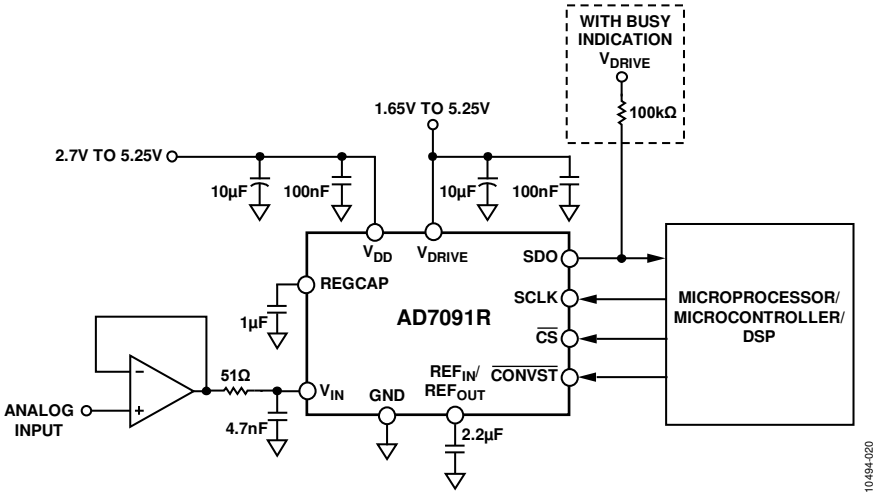


Figure 22. AD7091R Typical Connection Diagram

MODES OF OPERATION

The mode of operation of the AD7091R is selected by controlling the logic state of the $\overline{\text{CONVST}}$ signal when a conversion is complete.

The logic level of the $\overline{\text{CONVST}}$ pin at the end of a conversion determines whether the AD7091R remains in normal mode or enters power-down mode (see the Normal Mode and Power-Down Mode sections). Similarly, if the device is already in power-down mode, $\overline{\text{CONVST}}$ controls whether the device returns to normal mode or remains in power-down mode. These modes of operation provide flexible power management options, allowing optimization of the ratio of the power dissipation to the throughput rate for different application requirements.

Normal Mode

The normal mode of operation is intended to achieve the fastest throughput rate performance. Users do not have to worry about power-up times because the AD7091R remains fully powered at all times. Figure 29 shows the general timing diagram of the AD7091R in normal mode.

In this mode, the conversion is initiated on the falling edge of $\overline{\text{CONVST}}$, as described in the Serial Interface section. To ensure that the part remains fully powered up at all times, $\overline{\text{CONVST}}$ must return high after t_7 and remain high until the conversion is complete. At the end of a conversion (denoted as EOC in Figure 27), the logic state of $\overline{\text{CONVST}}$ is tested.

To read back data stored in the conversion result register, wait until the conversion is complete, and then pull $\overline{\text{CS}}$ low. The conversion data is subsequently clocked out on the SDO pin (see Figure 29). Because the output shift register is 12 bits wide, data is shifted out of the device as a 12-bit word under the control of the serial clock input (SCLK). After reading back the data, the user can pull $\overline{\text{CONVST}}$ low again to start another conversion after the t_{QUIET} time has elapsed.

Power-Down Mode

The power-down mode of operation is intended for use in applications where slower throughput rates and lower power consumption are required. In this mode, the ADC can be powered down either between each conversion or between a series of conversions performed at a high throughput rate, with the ADC powered down for relatively long durations between these bursts of several conversions. When the AD7091R is in power-down mode, the serial interface remains active even though all analog circuitry, including the internal voltage reference, is powered down.

To enter power-down mode, pull $\overline{\text{CONVST}}$ low and keep it low until the end of a conversion (denoted as EOC in Figure 30). After the conversion is complete, the logic level of the $\overline{\text{CONVST}}$ pin is tested. If the $\overline{\text{CONVST}}$ signal is logic low at this point, the part enters power-down mode.

The serial interface of the AD7091R is functional in power-down mode; therefore, users can read back the conversion result after the part enters power-down mode.

To exit this mode of operation and power up the AD7091R, pull $\overline{\text{CONVST}}$ high at any time. On the rising edge of $\overline{\text{CONVST}}$, the device begins to power up. The internal circuitry of the AD7091R requires 100 µs to power up from power-down mode. If the internal reference is used, the reference capacitor must be fully recharged before accurate conversions are possible.

To start the next conversion after exiting power-down mode, operate the interface as described in the Normal Mode section.

POWER CONSUMPTION

The two modes of operation for the AD7091R—normal mode and power-down mode (see the Modes of Operation section for more information)—produce different power vs. throughput rate performances. Using a combination of normal mode and power-down mode achieves the optimum power performance.

To calculate the overall power consumption, the I_{DRIVE} current should also be taken into consideration. Figure 16 shows the I_{DRIVE} current at various supply voltages. Figure 23 and Figure 24 show the power consumption for V_{DRIVE} with various throughput rates.

Improved power consumption for the AD7091R can be achieved by carefully selecting the V_{DD} and V_{DRIVE} supply voltages and the SDO line capacitance (see Figure 15 and Figure 16).

Normal Mode

With a 3 V V_{DD} supply and a throughput rate of 1 MSPS, the I_{DD} current consumption for the part in normal operational mode is 349 µA (composed of 21.6 µA of static current and 327.4 µA of dynamic current during conversion). The dynamic current consumption is directly proportional to the throughput rate.

The following example calculates the power consumption of AD7091R when operating in normal mode with a 500 kSPS throughput rate and a 3 V supply.

The dynamic conversion time contributes 491 µW to the overall power dissipation as follows:

$$((500 \text{ kSPS}/1 \text{ MSPS}) \times 327.4 \text{ µA}) \times 3 \text{ V} = 491 \text{ µW}$$

The contribution to the total power dissipated by the normal mode static operation is

$$21.6 \text{ µA} \times 3 \text{ V} = 65 \text{ µW}$$

Therefore, the total power dissipated at 500 kSPS is

$$491 \text{ µW} + 65 \text{ µW} = 556 \text{ µW}$$

Normal and Power-Down Mode Combination

A combination of normal mode and power-down mode achieves the optimum power performance.

The internal circuitry of the AD7091R requires 100 µs to power up from power-down mode. Power-down mode can therefore be performed at sampling rates of less than 10 kSPS.

Recharging the reference capacitor should also be considered when using the on-chip reference. The AD7091R can fully charge a 2.2 µF reference capacitor in typically 50 ms. However, the time to charge the reference capacitor is dependent on the amount of charge remaining on the capacitor when exiting power-down mode. The reference capacitor loses charge very slowly, resulting in much faster recharge times.

Figure 25 shows the AD7091R conversion sequence with a combination of normal mode and power-down mode with a throughput of 5 kSPS when using an external reference. With a V_{DD} supply voltage of 3 V, the static current is 21.6 µA. The dynamic current is 327.4 µA at 1 MSPS. The current consumption during power-down mode is 264 nA. A conversion requires 650 ns to complete, and the AD7091R requires 100 µs to power up from power-down mode when using an external reference.

The dynamic conversion time contributes 4.9 µW to the overall power dissipation as follows:

((5 kSPS/1 MSPS) × 327.4 µA) × 3 V = 4.9 µW

The contribution to the total power dissipated by the normal mode static operation and power-down mode is

((100.6 µs/200 µs) × 21.6 µA) × 3 V +

((99.4 µs/200 µs) × 264 nA) × 3 V = 33 µW

The conversion time of 650 ns is included in the static operation time.

The total power dissipated at 5 kSPS is

4.9 µW + 33 µW = 37.9 µW

Figure 23 and Figure 24 show the typical power vs. throughput rate for the AD7091R at 3 V for the V_{DD} supply and for the V_{DRIVE} supply. Power consumption for the V_{DRIVE} supply can be calculated by the same principles as those for the V_{DD} supply.

Additionally, Figure 24 shows the reduction in power consumption that can be achieved when power-down mode is used compared with using only normal mode at lower throughput rates.

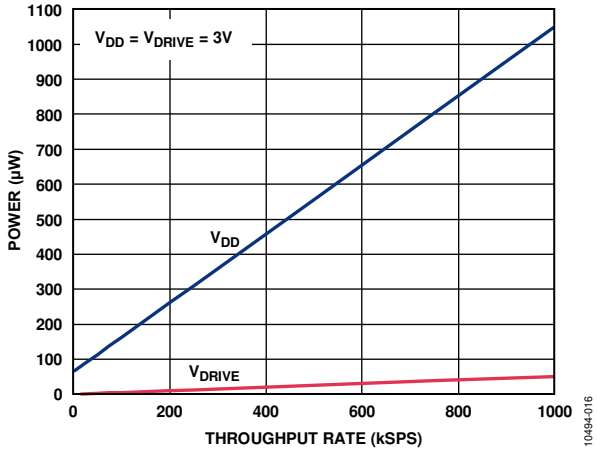


Figure 23. Power Dissipation vs. Throughput Rate (Full Range)

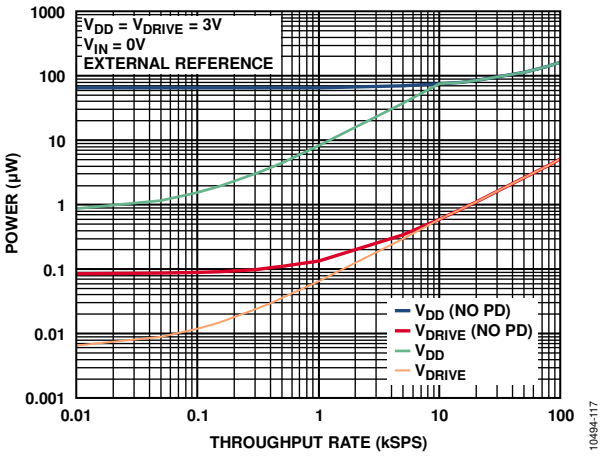


Figure 24. Power Dissipation vs. Throughput Rate (Lower Range)

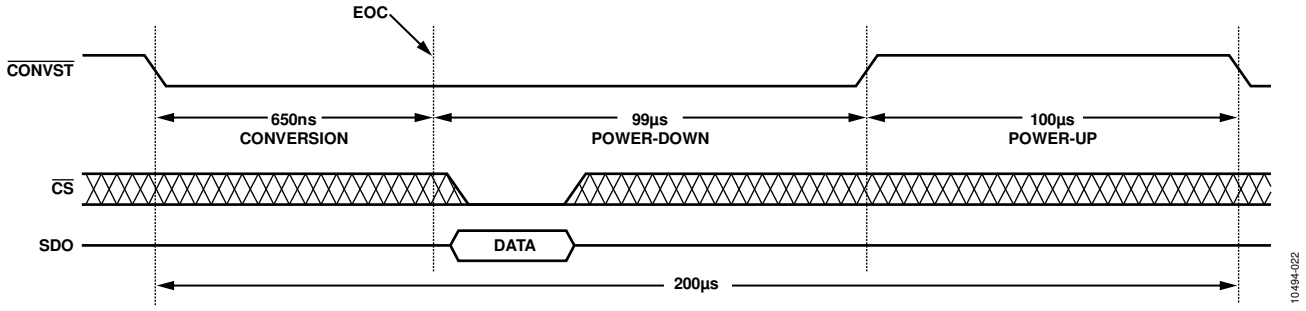


Figure 25. 10 SPS with Normal and Power-Down Mode

SERIAL INTERFACE

The AD7091R serial interface consists of four signals: SDO, SCLK, $\overline{\text{CONVST}}$, and $\overline{\text{CS}}$. The serial interface is used for accessing data from the result register and controlling the modes of operation of the device. SCLK is the serial clock input for the device, and SDO data transfers take place with respect to this SCLK. The $\overline{\text{CONVST}}$ signal is used to initiate the conversion process and to select the mode of operation of the AD7091R (see the Modes of Operation section). $\overline{\text{CS}}$ is used to frame the data. The falling edge of $\overline{\text{CS}}$ takes the SDO line out of a high impedance state. A rising edge on $\overline{\text{CS}}$ returns the SDO to a high impedance state.

The logic level of $\overline{\text{CS}}$ at the end of a conversion determines whether the BUSY indicator feature is enabled. This feature affects the propagation of the MSB with respect to $\overline{\text{CS}}$ and SCLK.

WITH BUSY INDICATOR

When the BUSY indicator feature is enabled, the SDO pin can be used as an interrupt signal to indicate that a conversion is complete. The connection diagram for this configuration is shown in Figure 26. Note that a pull-up resistor to V_{DRIVE} is required on the SDO pin. This allows the host to detect when the SDO pin exits the three-state condition after the end of a conversion. In this mode, 13 SCLK cycles are required: 12 clock cycles to propagate out the data and an additional clock cycle to return the SDO pin to the three-state condition.

To enable the BUSY indicator feature, a conversion should first be started. A high-to-low transition on $\overline{\text{CONVST}}$ initiates a conversion. This puts the track-and-hold into hold mode and samples the analog input at this point. If the user does not want the AD7091R to enter power-down mode, $\overline{\text{CONVST}}$ should be taken high before the end of the conversion. A conversion requires 650 ns to complete. When the conversion process is finished, the track-and-hold goes back to track mode. Before the end of a conversion, pull $\overline{\text{CS}}$ low to enable the BUSY indicator feature. The busy indicator is not valid for this first conversion, only on subsequent conversions. The user must ensure that $\overline{\text{CS}}$ is pulled low before the end of each conversion to keep the busy indicator enabled.

The conversion result is shifted out of the device as a 12-bit word under the control of SCLK and the logic state of $\overline{\text{CS}}$ at the end of a conversion. At the end of a conversion, SDO is driven low. SDO remains low until the MSB (DB11) of the conversion result is clocked out on the first falling edge of SCLK. DB10 to DB0 are shifted out on the subsequent falling edges of SCLK. The 13th SCLK falling edge returns SDO to a high impedance state. Data is propagated on SCLK falling edges and is valid on both the rising and falling edges of the next SCLK. The timing diagram for this mode is shown in Figure 27.

If another conversion is required, pull $\overline{\text{CONVST}}$ low again and repeat the read cycle.

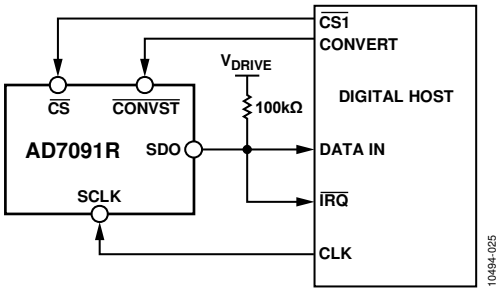
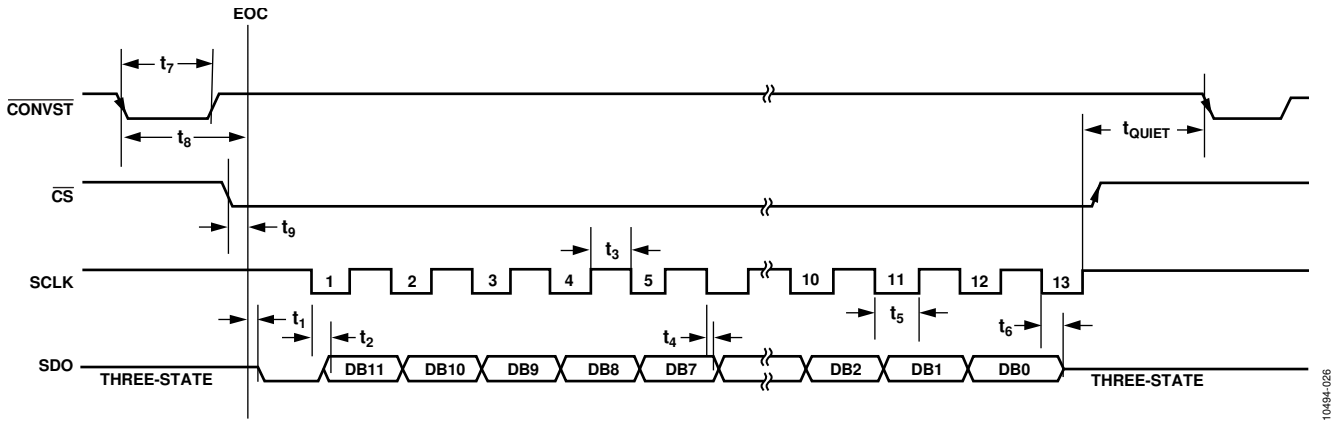


Figure 26. Connection Diagram with BUSY Indicator



NOTES
1. EOC IS THE END OF A CONVERSION.

Figure 27. Serial Port Timing with BUSY Indicator

WITHOUT BUSY INDICATOR

To operate the AD7091R without the BUSY indicator feature enabled, a conversion should first be started. A high-to-low transition on $\overline{\text{CONVST}}$ initiates a conversion. This puts the track-and-hold into hold mode and samples the analog input at this point. If the user does not want the AD7091R to enter power-down mode, $\overline{\text{CONVST}}$ should be taken high before the end of the conversion. A conversion requires 650 ns to complete. When the conversion process is finished, the track-and-hold goes back to track mode. To prevent the BUSY indicator feature from becoming enabled, ensure that $\overline{\text{CS}}$ is pulled high before the end of the conversion.

The data is shifted out of the device as a 12-bit word under the control of SCLK and $\overline{\text{CS}}$. The MSB (Bit DB11) is clocked out on the falling edge of $\overline{\text{CS}}$. DB10 to DB0 are shifted out on the subsequent falling edges of SCLK. The 12th falling SCLK edge returns SDO to a high impedance state. After all the data is clocked out, pull $\overline{\text{CS}}$ high again. SCLK should idle low in this mode to ensure that the MSB is not lost. Data is propagated on SCLK falling edges and is valid on both the rising and falling edges of the next SCLK. The timing diagram for this operation is shown in Figure 28.

If another conversion is required, pull $\overline{\text{CONVST}}$ low and repeat the read cycle.

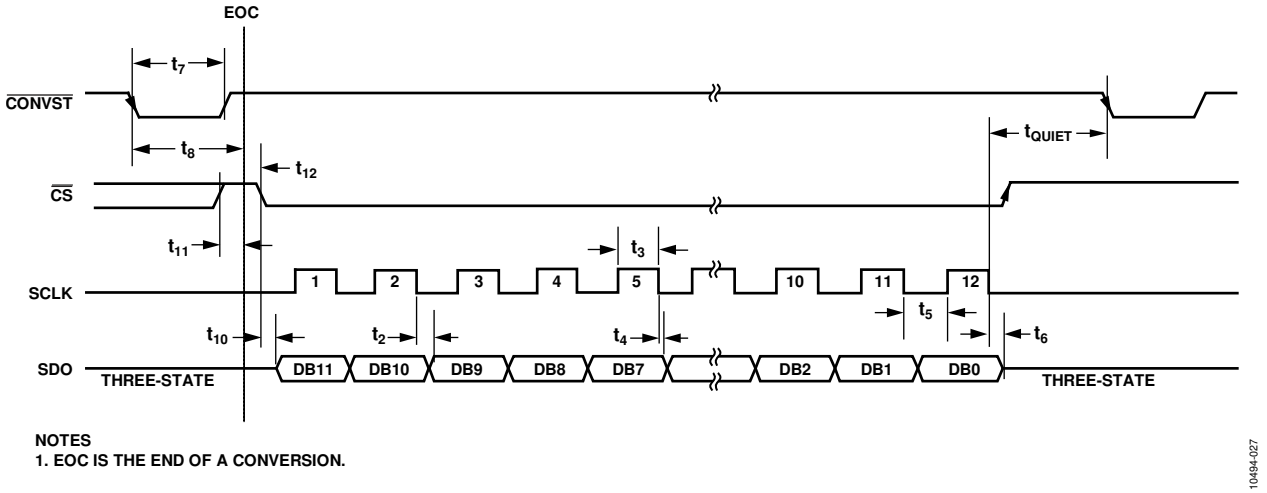


Figure 28. Serial Port Timing Without BUSY Indicator

SOFTWARE RESET

The AD7091R requires the user to initiate a software reset when power is first applied. It should be noted that failure to apply the correct software reset command may result in a device malfunction.

To issue a software reset,

1. Start a conversion.
2. Read back the conversion result by pulling $\overline{CS}$ low after the conversion is complete.
3. Between the second and eighth SCLK cycles, pull $\overline{CS}$ high to short cycle the read operation.
4. At the end of the next conversion, the software reset is executed.

If using the on-chip internal reference, the user should wait until the reference capacitor is fully charged to meet the specified performance.

The timing diagram for this operation is shown in Figure 31.

INTERFACING WITH 8-/16-BIT SPI

It is also possible to interface the AD7091R with a conventional 8-/16-bit SPI bus.

Performing conversions and reading results can be achieved by configuring the host SPI interface to 16 bits, which results in providing an additional four SCLK cycles to complete a conversion compared with the standard interface methods (see the With BUSY Indicator and Without BUSY Indicator sections). After the 13th SCLK falling edge with the BUSY indicator feature enabled or the 12th SCLK falling edge with the BUSY indicator feature disabled, SDO returns to a high impedance state. The additional four bits should be treated as don't cares by the host. All other timings are as outlined in Figure 27 and Figure 28, with t_{QUIET} starting after the 16th SCLK cycle.

A software reset can be performed by configuring the SPI bus to eight bits and performing the operation outlined in the Software Reset section.

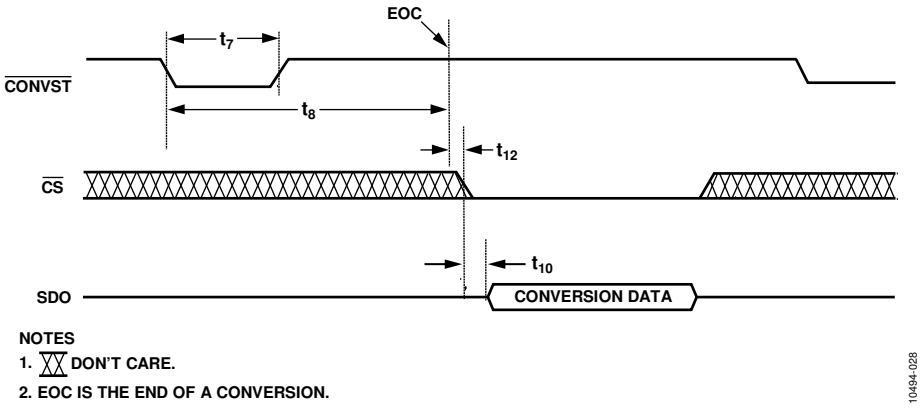


Figure 29. Serial Interface Read Timing—Normal Mode

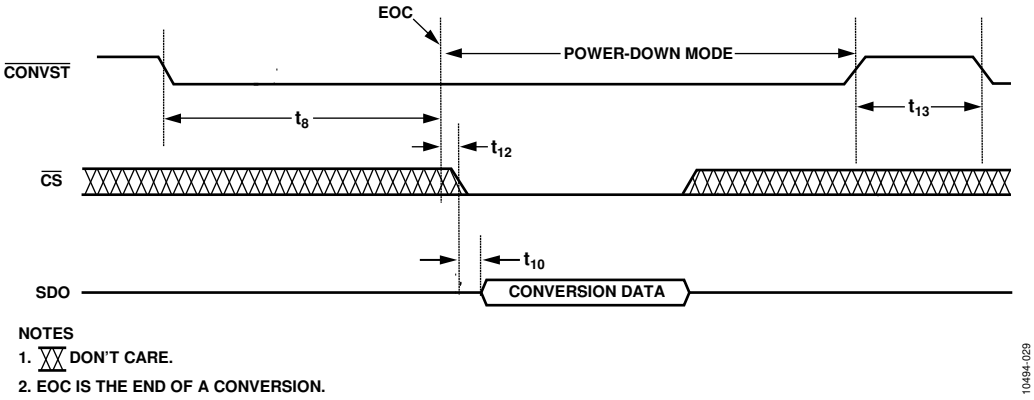
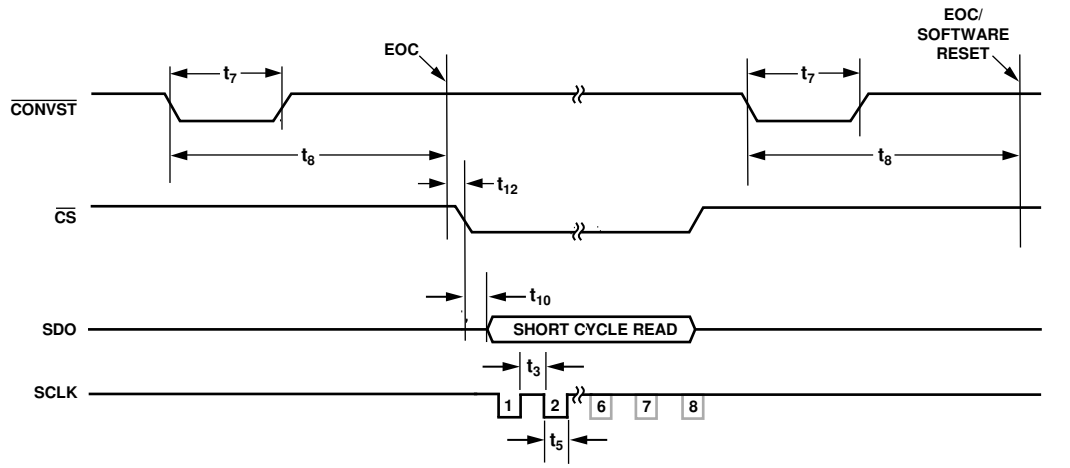


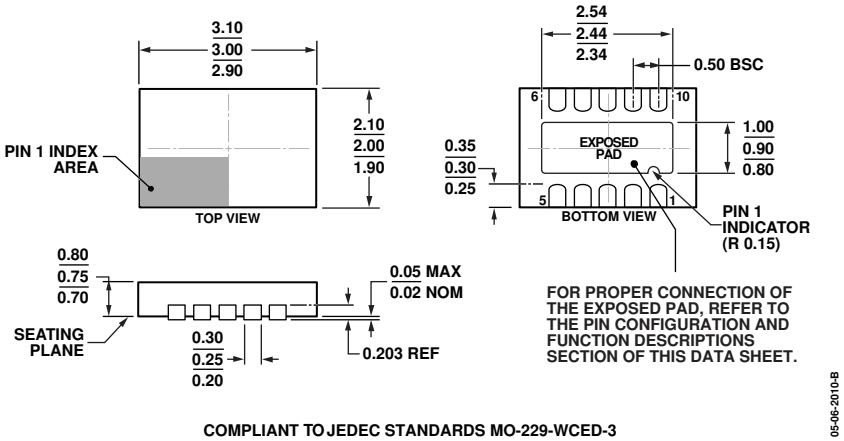
Figure 30. Entering/Exiting Power-Down Mode



NOTES
1. ⧖ DON'T CARE.
2. EOC IS THE END OF A CONVERSION.

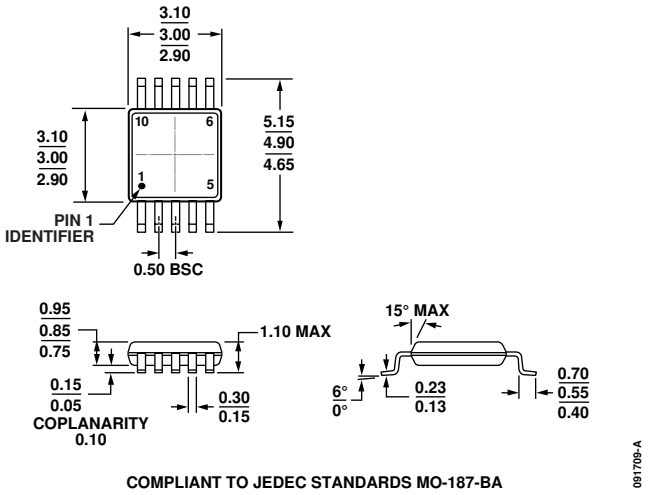
Figure 31. Software Reset Timing

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-229-WCED-3

Figure 32. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 2 mm Body, Very Very Thin, Dual Lead
(CP-10-12)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 33. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD7091RBCPZ-RL	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-12	C7P
AD7091RBCPZ-RL7	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-12	C7P
AD7091RBRMZ	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	DRQ
AD7091RBRMZ-RL7	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	DRQ
EVAL-AD7091RSDZ		Evaluation Board		
EVAL-SDP-CB1Z		Evaluation Controller Board		

[1] Z = RoHS Compliant Part.