



High-Speed CMOS Bus Interface 8-Bit Latches

QS54/74FCT573T
QS54/74FCT2573T

FEATURES/BENEFITS

- Pin and function compatible to the 74F573, 74FCT573 and 74FCT573T
- Industrial temperature -40°C to 85°C
- CMOS power levels: $<7.5\text{mW}$ static
- Available in DIP, SOIC, QSOP, ZIP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883, Class B

FCT-T 573T

- JEDEC-FCT spec compatible
- Std, A, and C speed grades with 4.2ns t_{PD} for C
- $I_{\text{OL}} = 48\text{mA}$ Ind., 32mA Mil.

FCT-T 2573T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std, A, and C speed grades with 4.2ns t_{PD} for C
- $I_{\text{OL}} = 12\text{mA}$ Ind.

DESCRIPTION

The QSFCT573T and QSFCT2573T are 8-bit high-speed CMOS TTL-compatible buffered latches with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The 2573 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2573 series parts can replace the 573 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V_{CC} is removed from the device.

Figure 1. Functional Block Diagram

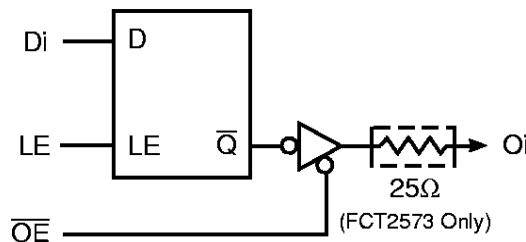


Figure 2. Pin Configurations (All Pins Top View)

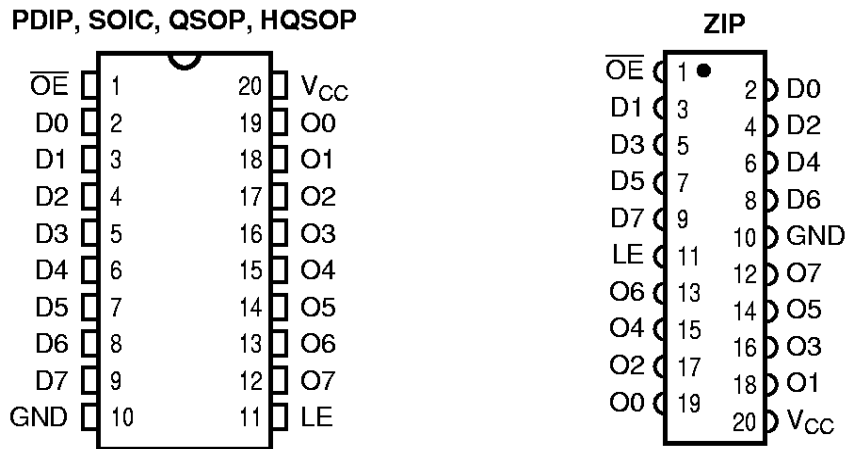


Table 1. Pin Description

| Name | I/O | Description |
|-----------------|-----|---------------|
| D_i | I | Data Inputs |
| O_i | O | Data Outputs |
| LE | I | Latch Enable |
| \overline{OE} | I | Output Enable |

Table 2. Function Table

| \overline{OE} | Inputs LE | D_i | Internal Q Value | Outputs O_i | Function |
|-----------------|--------------|-------|------------------------|------------------|-----------------|
| H | X | X | X | Hi-Z | Disable Outputs |
| L | L | X | L | L | Enable Outputs |
| L | L | X | H | H | Enable Outputs |
| L | H | L | L | L | Pass Inputs |
| L | H | H | H | H | Pass Inputs |
| L | L | X | Q | Q | Hold Prior Data |

Table 3. Absolute Maximum Ratings

| | |
|---|---------------|
| Supply Voltage to Ground | -0.5V to 7.0V |
| DC Output Voltage V_{OUT} | -0.5V to 7.0V |
| DC Input Voltage V_{IN} | -0.5V to 7.0V |
| AC Input Voltage (for a pulse width ≤ 20 ns) | -3.0V |
| DC Input Diode Current with $V_{IN} < 0$ | -20mA |
| DC Output Diode Current with $V_{OUT} < 0$ | -50mA |
| DC Output Current Max. Sink Current/Pin | 120mA |
| Maximum Power Dissipation | 0.5 watts |
| T_{STG} Storage Temperature | -65° to 150°C |

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 4. Capacitance⁽¹⁾

$T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$, $V_{IN} = 0\text{V}$, $V_{OUT} = 0\text{V}$

| Pins ⁽²⁾ | SOIC | QSOP | PDIP | ZIP | Unit |
|---------------------|------|------|------|-----|------|
| 1-9, 11 | 4 | 4 | 5 | 7 | pF |
| 12-19 | 6 | 6 | 7 | 9 | pF |

Notes:

1. Capacitance is characterized but not tested.
2. Pin reference for 20-pin package.

Table 5. Power Supply Characteristics

| Symbol | Parameter | Test Conditions ⁽¹⁾ | Min | Max | Unit |
|-----------------|-------------------------------------|--|-----|------|------------|
| I_{CC} | Quiescent Power Supply Current | $V_{CC} = \text{Max.}$, freq = 0 $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC}-0.2\text{V} \leq V_{IN} \leq V_{CC}$ | — | 1.5 | mA |
| ΔI_{CC} | Supply Current per Input @ TTL HIGH | $V_{CC} = \text{Max.}$, $V_{IN} = 3.4\text{V}$, freq = 0 ⁽²⁾ | — | 2.0 | mA |
| Q_{CCD} | Supply Current per Input per MHz | $V_{CC} = \text{Max.}$, Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or V_{CC} ^(3,4) | — | 0.25 | mA/ MHz |

Notes:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_{IN} = 3.4\text{V}$).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_C can be computed using the above parameters as explained in the Technical Overview section.

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Table 6. DC Electrical Characteristics Over Operating Range

Industrial $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 5\%$

Military $T_A = -55^{\circ}\text{C}$ to 125°C , $V_{CC} = 5.0\text{V} \pm 10\%$

| Symbol | Parameter | Test Conditions | Min | Typ ⁽¹⁾ | Max | Unit |
|--------------------------|---|--|------------|--------------------|--------------|---------------|
| V_{IH} | Input HIGH Voltage | Logic HIGH for All Inputs | 2.0 | — | — | V |
| V_{IL} | Input LOW Voltage | Logic LOW for All Inputs | — | — | 0.8 | V |
| ΔV_T | Input Hysteresis | $V_{TLH} - V_{THL}$ for All Inputs | — | 0.2 | — | V |
| $ I_{IH} $ $ I_{IL} $ | Input Current Input HIGH or LOW | $V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$ | — | — | 5 | μA |
| $ I_{OZ} $ | Off-State Output Current (Hi-Z) | $V_{CC} = \text{Max.}, 0 \leq V_{IN} \leq V_{CC}$ | — | — | 5 | μA |
| I_{OS} | Short Circuit Current (FCT573) | $V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$ | -60 | — | — | mA |
| I_{OR} | Current Drive (FCT2573 - 25 Ω) | $V_{CC} = \text{Min.}, V_{OUT} = 2.0\text{V}^{(3)}$ | 50 | — | — | mA |
| V_{IC} | Input Clamp Voltage | $V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}, T_A = 25^{\circ}\text{C}^{(3)}$ | — | -0.7 | -1.2 | V |
| V_{OH} | Output HIGH Voltage | $V_{CC} = \text{Min.}, I_{OH} = -12\text{mA (MIL)}$ $I_{OH} = -15\text{mA (IND)}$ | 2.4 2.4 | — — | — — | V |
| V_{OL} | Output LOW Voltage (FCT573) | $V_{CC} = \text{Min.}, I_{OL} = 32\text{mA (MIL)}$ $I_{OL} = 48\text{mA (IND)}$ | — — | — — | 0.50 0.50 | V |
| V_{OL} | Output LOW Voltage (FCT2573 - 25 Ω) | $V_{CC} = \text{Min.}, I_{OL} = 12\text{mA (MIL)}$ $I_{OL} = 12\text{mA (IND)}$ | — — | — — | 0.50 0.50 | V |
| R_{OUT} | Output Resistance (FCT2573 - 25 Ω) | $V_{CC} = \text{Min.}, I_{OL} = 12\text{mA (MIL)}$ $I_{OL} = 12\text{mA (IND)}$ | — 20 | 25 28 | — 40 | Ω |

Notes:

1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

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Table 7. Switching Characteristics Over Operating Range

Industrial $T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 5\%$

Military $T_A = -55^\circ\text{C}$ to 125°C , $V_{CC} = 5.0\text{V} \pm 10\%$

$C_{LOAD} = 50\text{pF}$, $R_{LOAD} = 500\Omega$ unless otherwise noted.

| Symbol | Description ⁽¹⁾ | | 573 2573 | | 573A 2573A | | 573C 2573C | | Unit |
|--------------------------|---|------------|-------------|------------|---------------|------------|---------------|------------|------|
| | | | Min | Max | Min | Max | Min | Max | |
| t_{PHL} t_{PLH} | Propagation Delay Data to Oi, 573 | IND MIL | 1.5 2 | 8 8.5 | 1.5 1.5 | 5.2 5.6 | 1.5 1.5 | 4.2 5.1 | ns |
| t_{PHL} t_{PLH} | Propagation Delay Data to Oi, 2573 | IND MIL | 1.5 2 | 8 8.5 | 1.5 1.5 | 5.2 5.6 | 1.5 1.5 | 4.2 5.1 | ns |
| t_{PHLE} t_{PLHE} | Propagation Delay LE to Oi, 573 | IND MIL | 2 2 | 13 14 | 2 2 | 8.5 9.8 | 2 2 | 5.5 8 | ns |
| t_{PHLE} t_{PLHE} | Propagation Delay LE to Oi, 2573 | IND MIL | 2 2 | 13 14 | 2 2 | 8.5 9.8 | 2 2 | 5.5 8 | ns |
| t_{PZH} t_{PZL} | Output Enable Time \overline{OE} to Yi, 573 | IND MIL | 1.5 1.5 | 11 12.5 | 1.5 1.5 | 6.5 7.5 | 1.5 1.5 | 5.5 6.3 | ns |
| t_{PZH} t_{PZL} | Output Enable Time \overline{OE} to Yi, 2573 | IND MIL | 1.5 1.5 | 11 12.5 | 1.5 1.5 | 6.5 7.5 | 1.5 1.5 | 6.5 7.5 | ns |
| t_{PLZ} t_{PHZ} | Output Disable Time ⁽²⁾ \overline{OE} to Yi | IND MIL | 1.5 1.5 | 7 8.5 | 1.5 1.5 | 5.5 6.5 | 1.5 1.5 | 5.0 5.9 | ns |
| t_S | Data Setup Time Di to LE HIGH to LOW | IND MIL | 2 2 | | 2 2 | | 2 | | ns |
| t_H | Data Hold Time Di to LE HIGH to LOW | IND MIL | 1.5 1.5 | | 1.5 1.5 | | 1.5 | | ns |
| t_W | LE Pulse Width ⁽²⁾ HIGH to LOW | IND MIL | 6 6 | | 5 6 | | 4 | | ns |

Notes:

1. Minimums guaranteed but not tested for all parameters except t_S and t_H .
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.