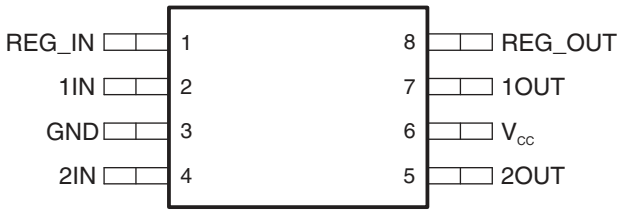
DUAL HIGH-SPEED MOSFET DRIVER

Check for Samples: TPS2811-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Industry-Standard Driver Replacement**
- **25-ns Max Rise/Fall Times and 40-ns Max Propagation Delay With 1-nF Load, V_{CC} = 14 V**
- **2-A Peak Output Current, V_{CC} = 14 V**
- **5-µA Supply Current With Input High or Low**
- **4-V to 14-V Supply-Voltage Range; Internal Regulator Extends Range to 40 V**
- **−40°C to 125°C Ambient-Temperature Operating Range**

PW PACKAGE
(TOP VIEW)



DESCRIPTION

The TPS2811 dual high-speed MOSFET driver is capable of delivering peak currents of 2 A into highly capacitive loads. This performance is achieved with a design that inherently minimizes shoot-through current and consumes an order of magnitude less supply current than competitive products.

The TPS2811 driver include a regulator to allow operation with supply inputs between 14 V and 40 V. The regulator output can power other circuitry, provided power dissipation does not exceed package limitations. When the regulator is not required, REG_IN and REG_OUT can be left disconnected or both can be connected to V_{CC} or GND.

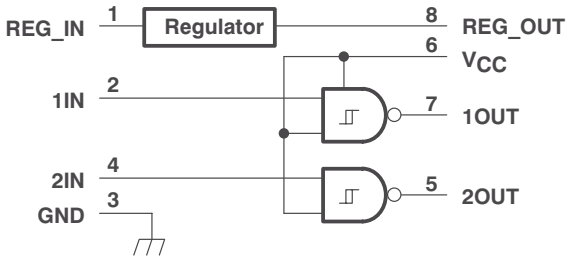
TPS2811 driver is available in an 8-pin TSSOP package and operates over a ambient temperature range of −40°C to 125°C.

ORDERING INFORMATION(1)

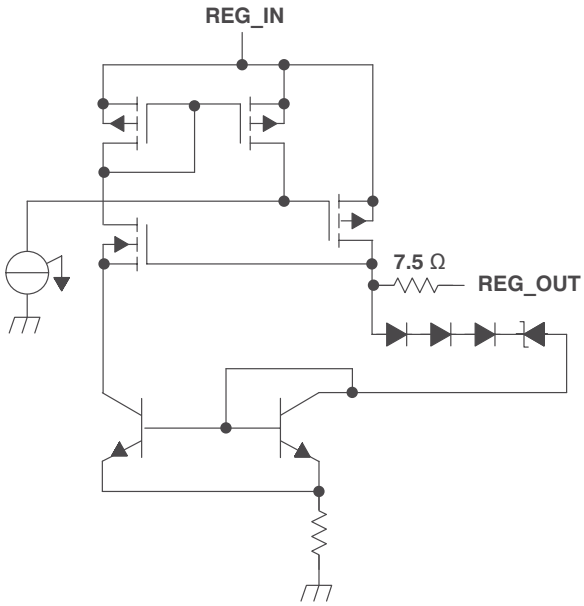
T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	TSSOP – PW	Reel of 2000	TPS2811QPWRQ1	2811Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

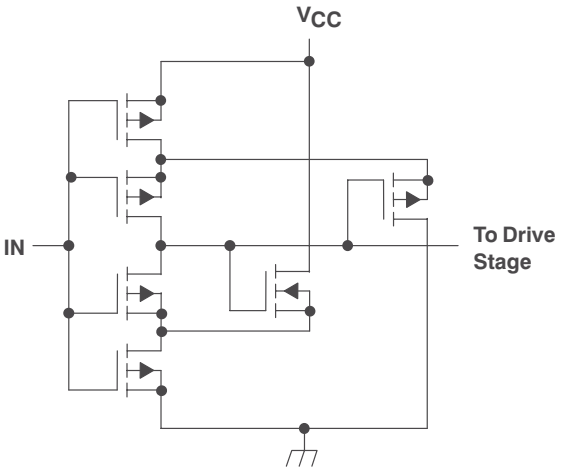
FUNCTIONAL BLOCK DIAGRAM



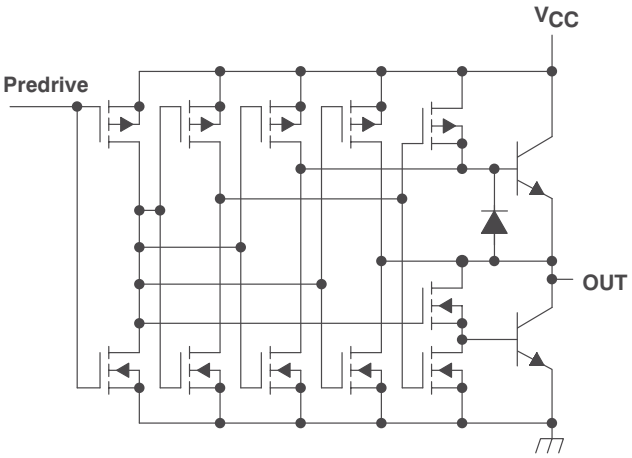
REGULATOR DIAGRAM



INPUT STAGE DIAGRAM



OUTPUT STAGE DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
REG_IN	1	Regulator input
1IN	2	Input 1
GND	3	Ground
2IN	4	Input 2
2OUT	5	Output 2; 2OUT = $\overline{2IN}$
V_{CC}	6	Supply voltage
1OUT	7	Output 1; 1OUT = $\overline{1IN}$
REG_OUT	8	Regulator output

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage		−0.3 V to 15 V
	Regulator input voltage range	REG_IN	VCC −0.3 V to 42 V
	Input voltage range	1IN, 2IN	−0.3 V to VCC +0.5 V
	Output voltage range	1OUT, 2OUT	–0.5 < V < VCC +0.5 V
	Continuous regulator output current	REG_OUT	25 mA
	Continuous output current	1OUT, 2OUT	±100 mA
T_A	Operating ambient temperature range		−40°C to 125°C
T_{stg}	Storage temperature range		−65°C to 150°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to device GND pin.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
	Regulator input voltage		8	40	V
V_{CC}	Supply voltage		4	14	V
	Input voltage	1IN, 2IN	-0.3	V_{CC}	V
	Continuous regulator output current	REG_OUT	0	20	mA
T_A	Operating ambient temperature range		-40	125	°C

ELECTRICAL CHARACTERISTICS

over recommended operating ambient temperature range, V_{CC} = 10 V, REG_IN open, C_L = 1 nF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
INPUTS						
V_{T+}	Positive-going input threshold voltage	V_{CC} = 5 V		3.3	4	V
		V_{CC} = 10 V		5.8	9	
		V_{CC} = 14 V		8.3	13	
V_{T-}	Negative-going input threshold voltage	V_{CC} = 5 V	1	1.6		V
		V_{CC} = 10 V	1	4.2		
		V_{CC} = 14 V	1	6.2		
	Input hysteresis	V_{CC} = 5 V		1.6		V
I_I	Input current	Inputs = 0 V or V_{CC}	-1	0.2	1	µA
C_I	Input capacitance			5	10	pF
OUTPUTS						
V_{OH}	High-level output voltage	I_O = −1 mA	9.75	9.9		V
		I_O = −100 mA	8	9.1		
V_{OL}	Low-level output voltage	I_O = 1 mA		0.18	0.25	V
		I_O = 100 mA		1	2	
I_O	Peak output current	V_{CC} = 10 V		2		A
REGULATOR						
V_O	Output voltage	14 ≤ REG_IN ≤ 40 V, 0 ≤ I_O ≤ 20 mA	10	11.5	13	V
	Output voltage in dropout	I_O = 10 mA, REG_IN = 10 V	9	9.6		V
SUPPLY CURRENT						
I_{CC}	Supply current into V_{CC}	Inputs high or low		0.2	5	µA
	Supply current into REG_IN	REG_IN = 20 V, REG_OUT open		40	100	µA

(1) Typical values are at T_A = 25°C unless otherwise noted.

SWITCHING CHARACTERISTICS

over recommended operating ambient temperature range, REG_IN open, C_L = 1 nF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_r	Rise time	V_{CC} = 14 V		14	25	ns
		V_{CC} = 10 V		15	30	
		V_{CC} = 5 V		20	35	
t_f	Fall time	V_{CC} = 14 V		15	25	ns
		V_{CC} = 10 V		15	30	
		V_{CC} = 5 V		18	35	
t_{PHL}	Propagation delay time, high-to-low-level output	V_{CC} = 14 V		25	40	ns
		V_{CC} = 10 V		25	45	
		V_{CC} = 5 V		34	50	
t_{PLH}	Propagation delay time low-to-high-level output	V_{CC} = 14 V		24	40	ns
		V_{CC} = 10 V		26	45	
		V_{CC} = 5 V		36	50	

(1) Typical values are at T_A = 25°C unless otherwise noted.

PARAMETER MEASUREMENT INFORMATION

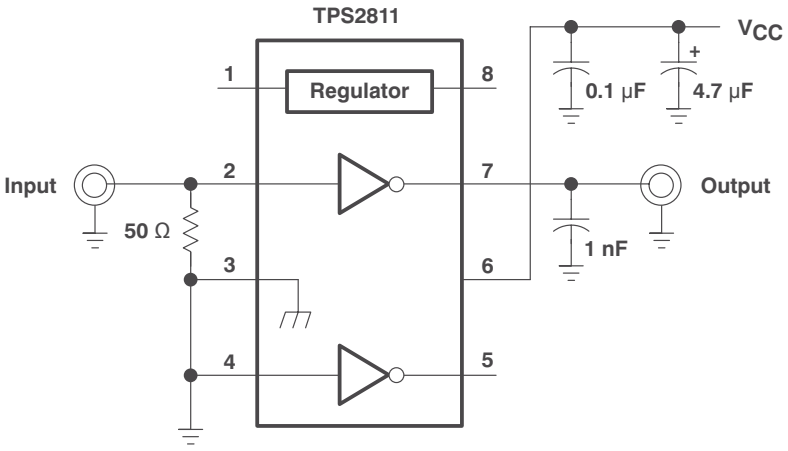


Figure 1. Test Circuit For Measurement of Switching Characteristics

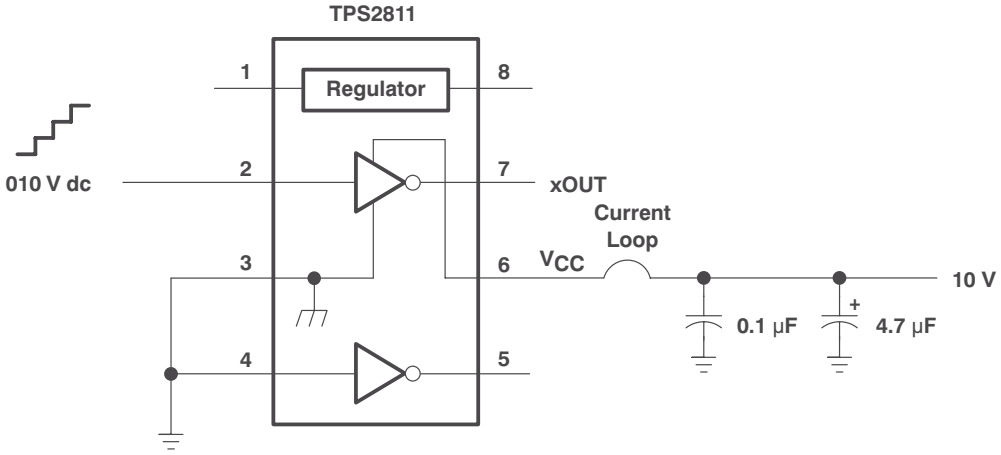


Figure 2. Shoot-Through Current Test Setup

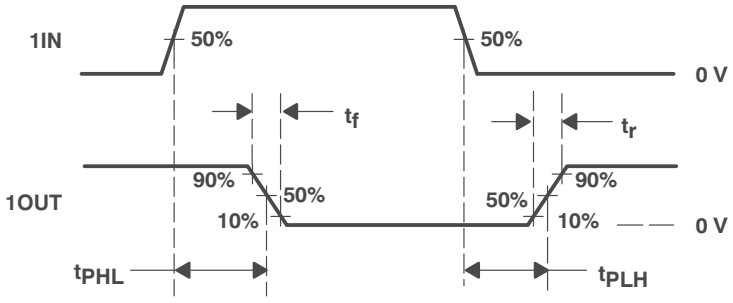


Figure 3. Typical Timing Diagram

TYPICAL CHARACTERISTICS

Table 1. Characteristics Graphs and Application Information

PARAMETER	vs PARAMETER 2		FIGURE
Typical Characteristics			
Rise time	Supply voltage		4
Fall time	Supply voltage		5
Propagation delay time	Supply voltage		6, 7
Supply current	Supply voltage		8
	Load capacitance		9
	Ambient temperature		0
Input threshold voltage	Supply voltage		11
Regulator output voltage	Regulator input voltage		12, 13
Regulator quiescent current	Regulator input voltage		14
Peak source current	Supply voltage		15
Peak sink current	Supply voltage		16
Shoot-through current	Input voltage, high-to-low		17
	Input voltage, low-to-high		18
General Applications			
Switching test circuits and application information			19, 20
Voltage of 1OUT vs 2OUT	Time	Low-to-high	21, 22, 23
		High-to-low	24, 25, 26
Circuit for Measuring Paralleled Switching Characteristics			
Switching test circuits and application information			27
Input voltage vs output voltage	Time	Low-to-high	28, 30
		High-to-low	29, 31
Hex-1 to Hex-4 Application Information			
Driving test circuit and application information			32
Drain-source voltage vs drain current	Time	Hex-1 size	33
		Hex-2 size	36
		Hex-3 size	39
		Hex-4 size	41
		Hex-4 size parallel drive	45
	Time	Hex-1 size	34
		Hex-2 size	37
		Hex-3 size	40
		Hex-4 size	43
		Hex-4 size parallel drive	46
	Time	Hex-1 size	35
		Hex-2 size	38
		Hex-3 size	42
		Hex-4 size	44
		Hex-4 size parallel drive	47
Synchronous Buck Regulator Application			
3.3-V 3-A Synchronous-Rectified Buck Regulator Circuit			48
Q1 drain voltage vs gate voltage at turn-on	Time		49
Q1 drain voltage vs gate voltage at turn-off	Time		50
Q1 drain voltage vs Q2 gate-source voltage	Time		51, 52, 53
Output ripple voltage vs inductor current	Time	3 A	54
		5 A	55

RISE TIME
vs
SUPPLY VOLTAGE

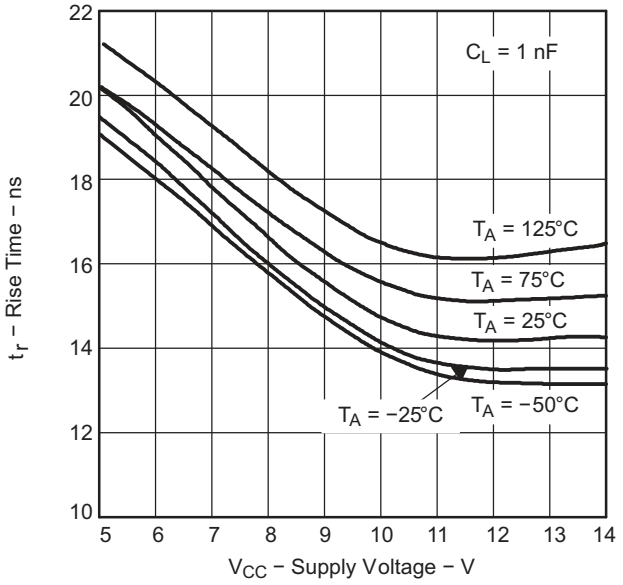


Figure 4.

FALL TIME
vs
SUPPLY VOLTAGE

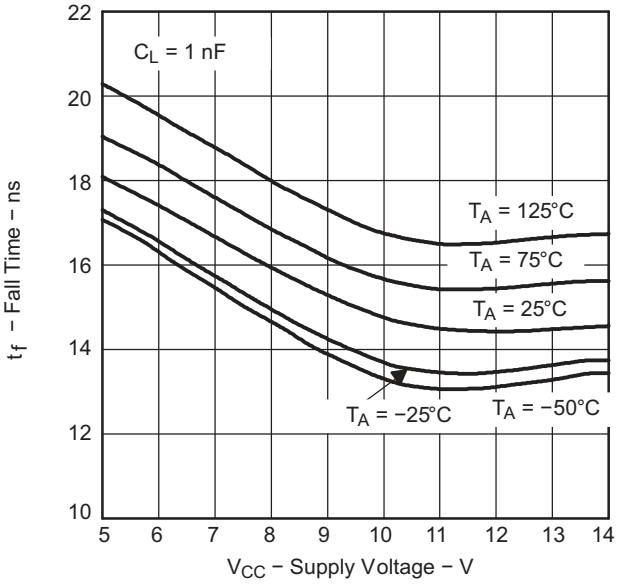


Figure 5.

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

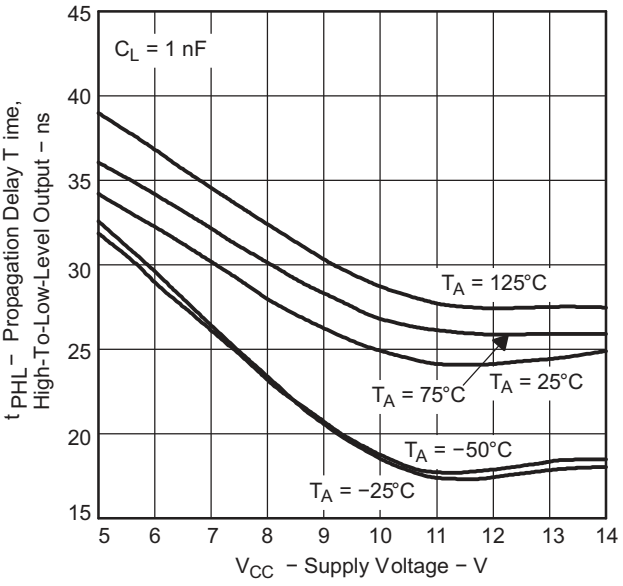


Figure 6.

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

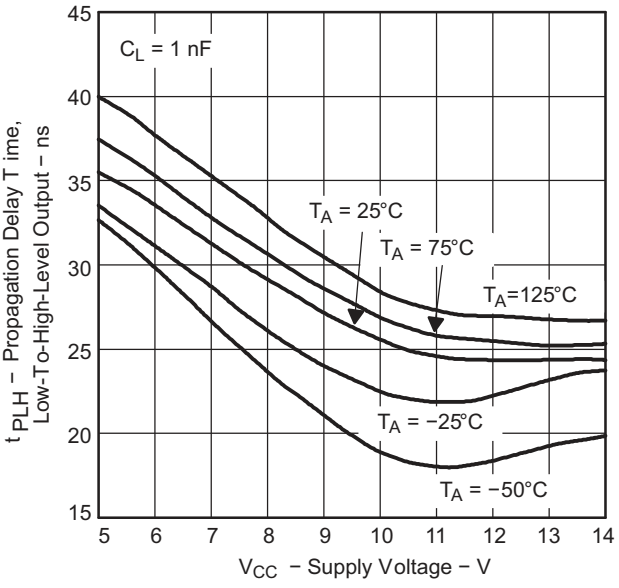


Figure 7.

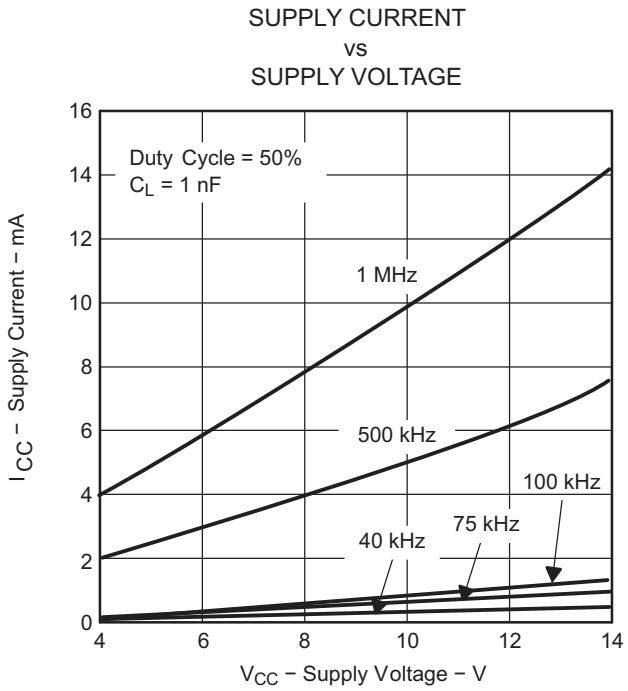


Figure 8.

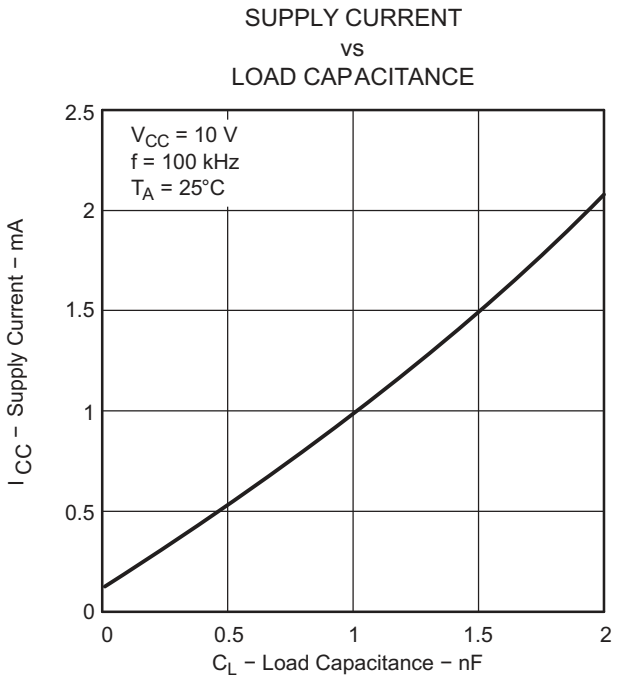


Figure 9.

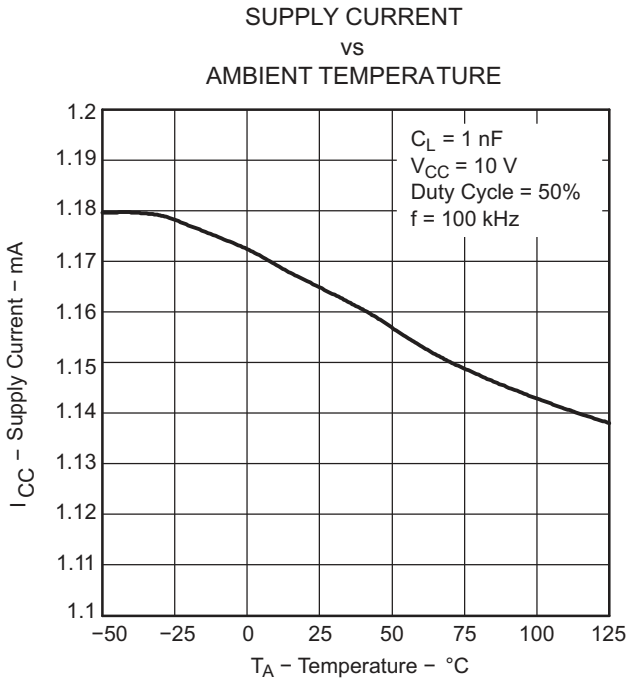


Figure 10.

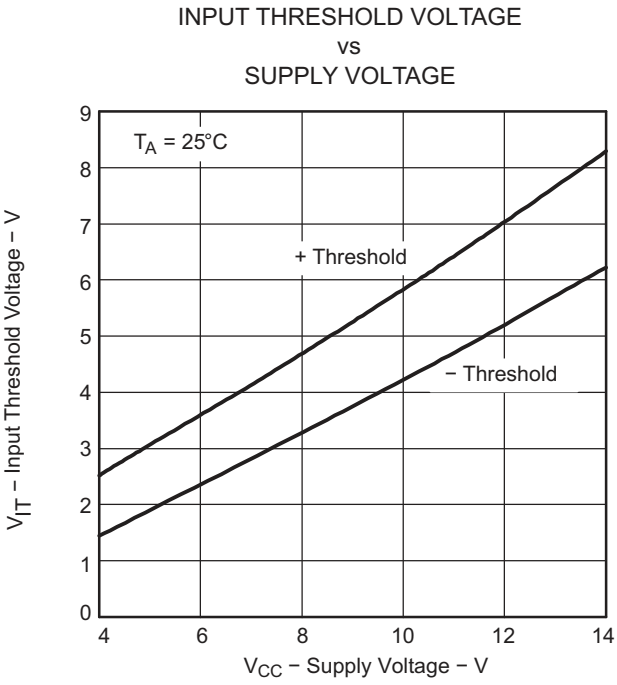


Figure 11.

REGULATOR OUTPUT VOLTAGE
vs
REGULATOR INPUT VOLTAGE

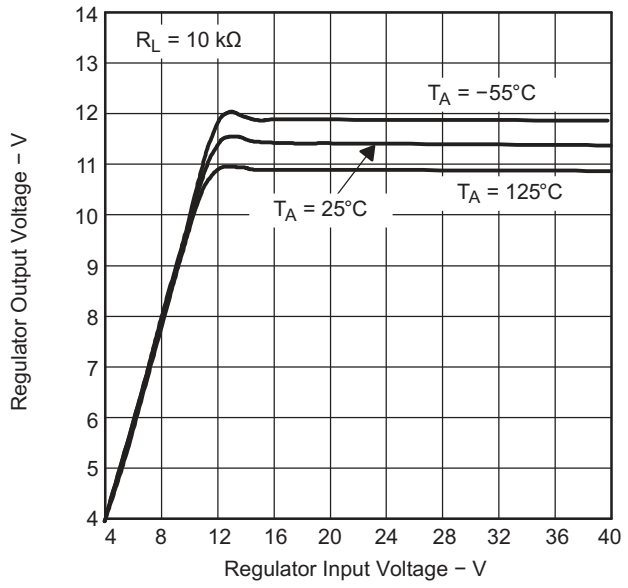


Figure 12.

REGULATOR OUTPUT VOLTAGE
vs
REGULATOR INPUT VOLTAGE

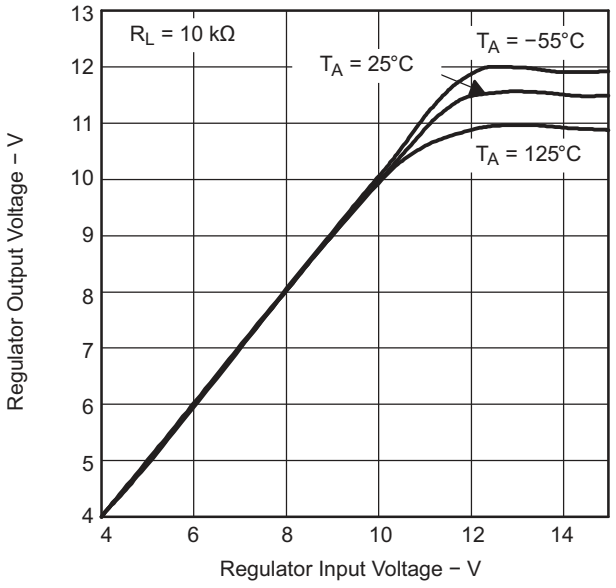


Figure 13.

REGULATOR QUIESCENT CURRENT
vs
REGULATOR INPUT VOLTAGE

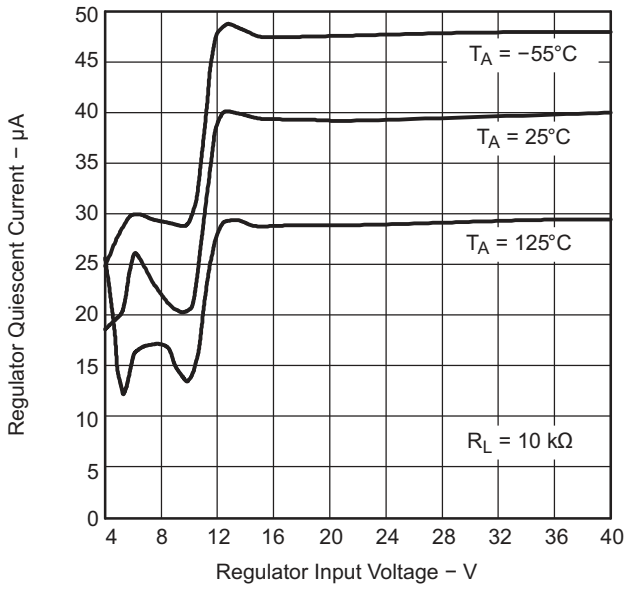


Figure 14.

PEAK SOURCE CURRENT
vs
SUPPLY VOLTAGE

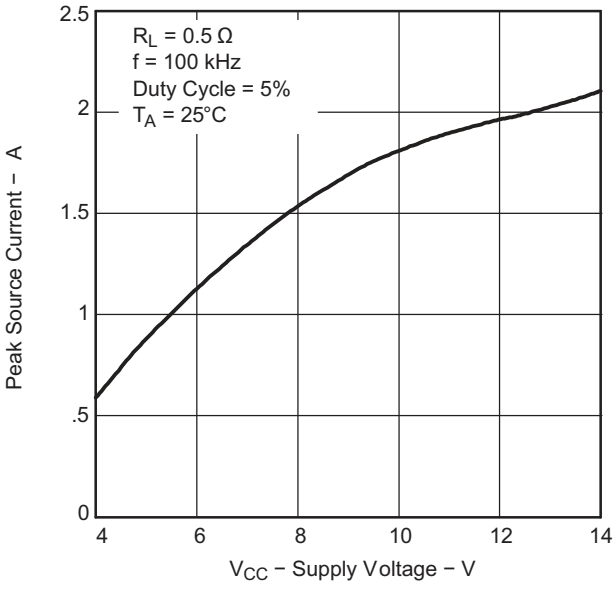


Figure 15.

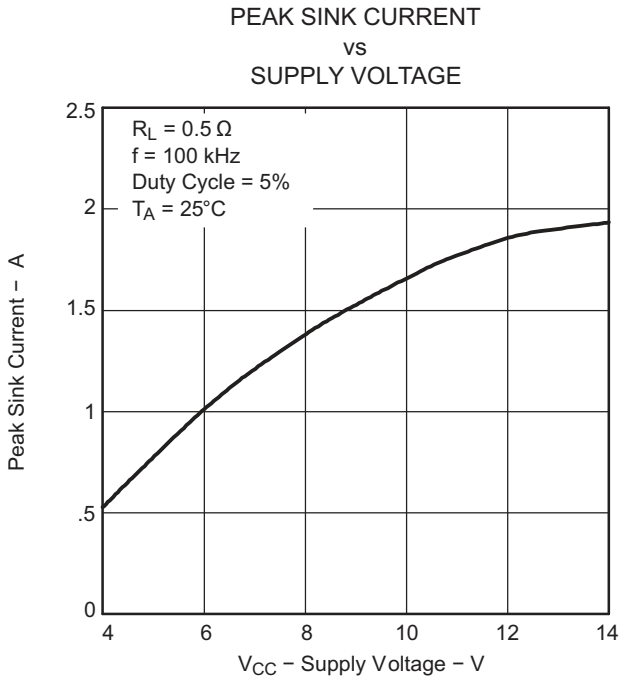


Figure 16.

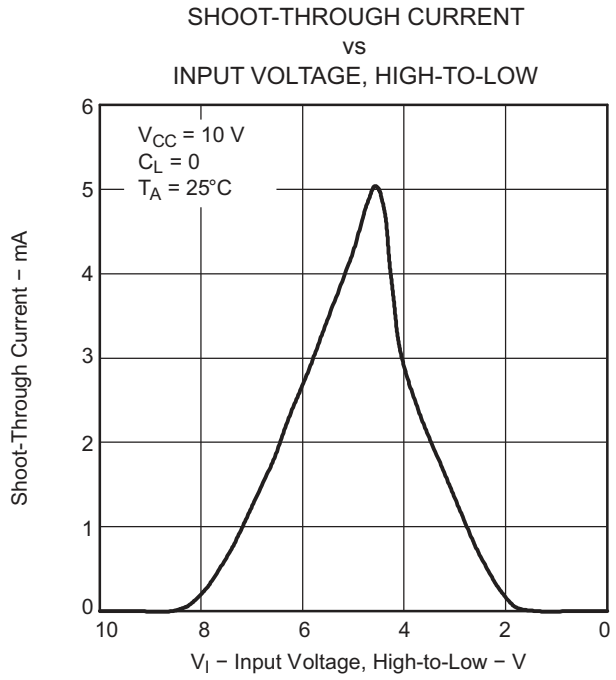


Figure 17.

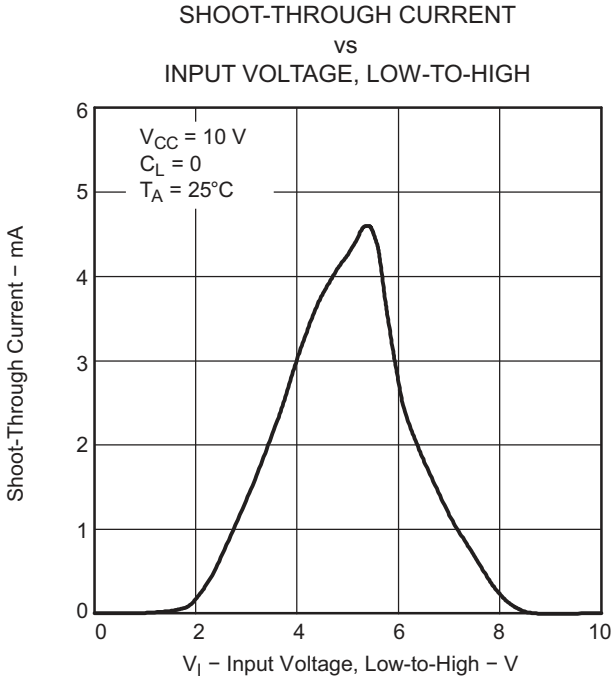


Figure 18.

APPLICATION INFORMATION

The TPS2811 circuits each contain one regulator and two MOSFET drivers. The regulator can be used to limit V_{CC} to between 10 V and 13 V for a range of input voltages from 14 V to 40 V, while providing up to 20 mA of dc drive. The TPS2811 has inverting drivers. These MOSFET drivers are capable of supplying up to 2.1 A or sinking up to 1.9 A (see Figures 15 and 16) of instantaneous current to n-channel or p-channel MOSFETs. The TPS2811 MOSFET drivers have very fast switching times combined with very short propagation delays. These features enhance the operation of today's high-frequency circuits.

The CMOS input circuit has a positive threshold of approximately 2/3 of V_{CC}, with a negative threshold of 1/3 of V_{CC}, and a very high input impedance in the range of 109Ω. Noise immunity is also very high because of the Schmitt-trigger switching. In addition, the design is such that the normal shoot-through current in CMOS (when the input is biased halfway between V_{CC} and ground) is limited to less than 6 mA. The limited shoot-through is evident in the graphs in Figures 17 and 18. The input stage shown in the functional block diagram better illustrates the way the front end works. The circuitry of the device is such that regardless of the rise and/or fall time of the input signal, the output signal will always have a fast transition speed; this basically isolates the waveforms at the input from the output. Therefore, the specified switching times are not affected by the slopes of the input waveforms.

The basic driver portion of the circuits operate over a supply voltage range of 4 V to 14 V with a maximum bias current of 5 µA. Each driver consists of a CMOS input and a buffered output with a 2-A instantaneous drive capability. They have propagation delays of less than 30 ns and rise and fall times of less than 20 ns each. Placing a 0.1-µF ceramic capacitor between V_{CC} and ground is recommended; this will supply the instantaneous current needed by the fast switching and high current surges of the driver when it is driving a MOSFET.

The output circuit is also shown in the functional block diagram. This driver uses a unique combination of a bipolar transistor in parallel with a MOSFET for the ability to swing from VCC to ground while providing 2 A of instantaneous driver current. This unique parallel combination of bipolar and MOSFET output transistors provides the drive required at V_{CC} and ground to guarantee turn-off of even low-threshold MOSFETs. Typical bipolar-only output devices don't easily approach V_{CC} or ground.

The regulator included in the TPS2811 has an input voltage range of 14 V to 40 V. It produces an output voltage of 10 V to 13 V and is capable of supplying from 0 to 20 mA of output current. In grounded source applications, this extends the overall circuit operation to 40 V by clamping the driver supply voltage (V_{CC}) to a safe level for both the driver and the MOSFET gate. The bias current for full operation is a maximum of 150 µA. A 0.1-µF capacitor connected between the regulator output and ground is required to ensure stability. For transient response, an additional 4.7-µF electrolytic capacitor on the output and a 0.1-µF ceramic capacitor on the input will optimize the performance of this circuit. When the regulator is not in use, it can be left open at both the input and the output, or the input can be shorted to the output and tied to either the V_{CC} or the ground pin of the chip.

Matching and Paralleling Connections

Figure 19 and Figure 20 show the delays for the rise and fall time of each channel. As can be seen on a 5-ns scale, there is very little difference between the two channels at no load. Figures 23 and 24 show the difference between the two channels for a 1-nF load on each output. There is a slight delay on the rising edge, but little or no delay on the falling edge. As an example of extreme overload, Figures 25 and 26 show the difference between the two channels, or two drivers in the package, each driving a 10-nF load. As would be expected, the rise and fall times are significantly slowed down. Figures 28 and 29 show the effect of paralleling the two channels and driving a 1-nF load. A noticeable improvement is evident in the rise and fall times of the output waveforms. Finally, Figures 30 and 31 show the two drivers being paralleled to drive the 10-nF load and as could be expected the waveforms are improved. In summary, the paralleling of the two drivers in a package enhances the capability of the drivers to handle a larger load. Because of manufacturing tolerances, it is not recommended to parallel drivers that are not in the same package.

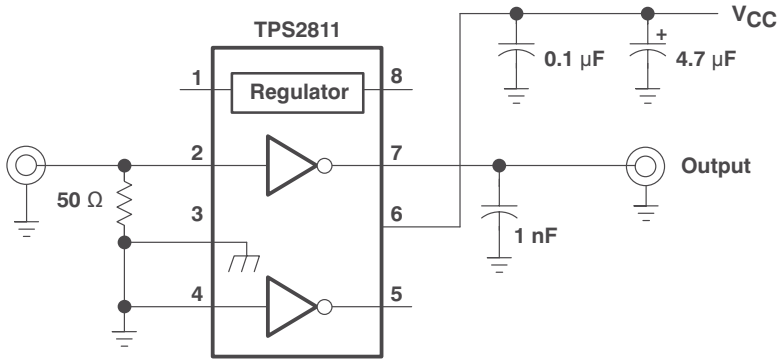
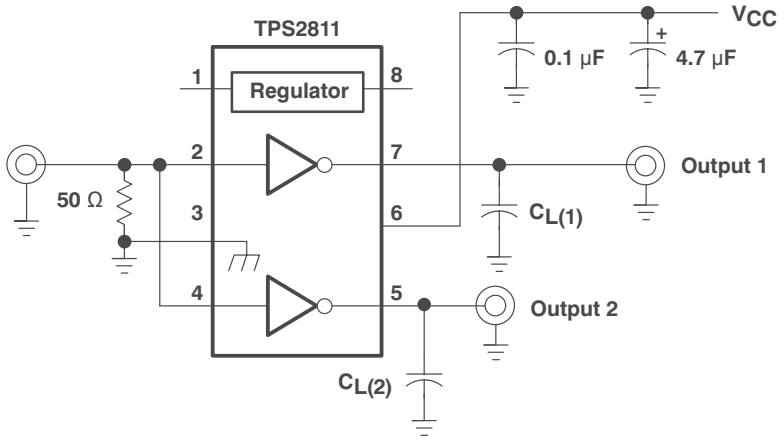


Figure 19. Test Circuit for Measuring Switching Characteristics



A. Input rise and fall times should be ≤10 ns for accurate measurement of ac parameters.

Figure 20. Test Circuit for Measuring Switching Characteristics With the Inputs Connected in Parallel

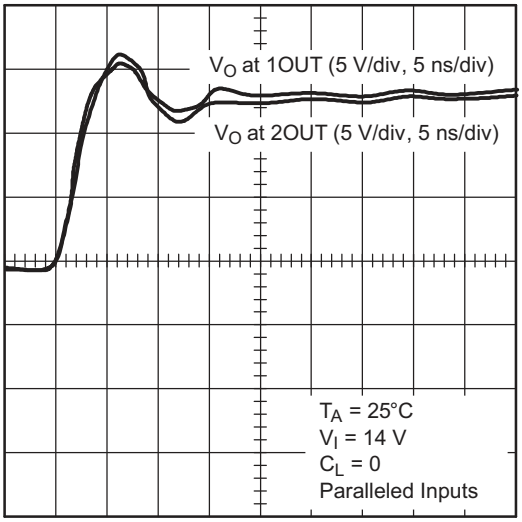


Figure 21. Voltage of 1OUT vs Voltage at 2OUT, Low-to-High Output Delay

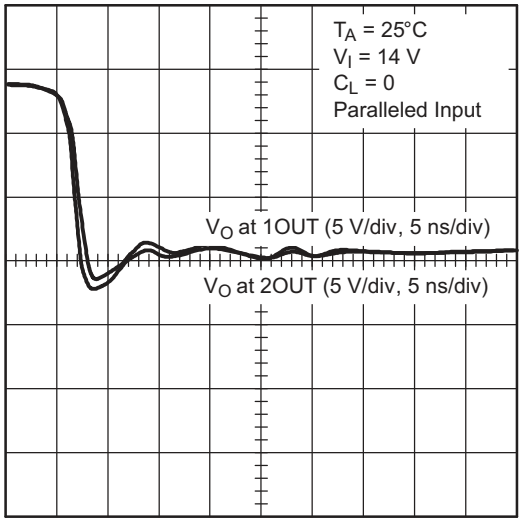


Figure 22. Voltage at 1OUT vs Voltage at 2OUT, High-to-Low Output Delay

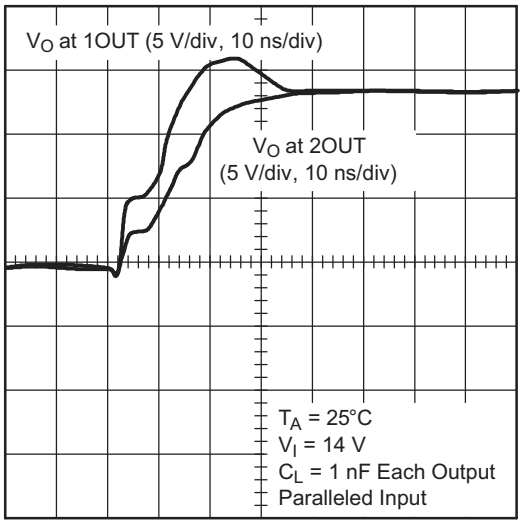


Figure 23. Voltage at 1OUT vs Voltage at 2OUT, Low-to-High Output Delay

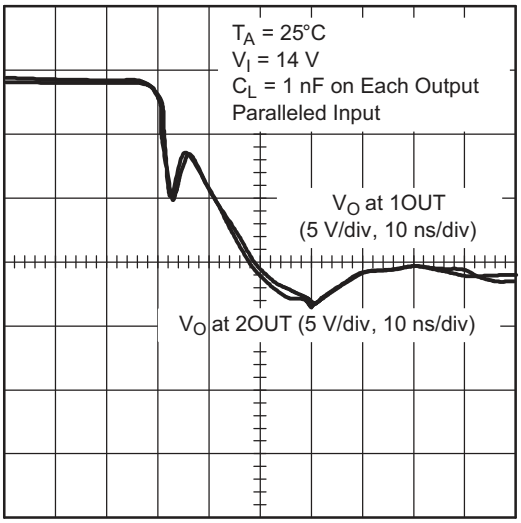


Figure 24. Voltage at 1OUT vs Voltage at 2OUT, High-to-Low Output Delay

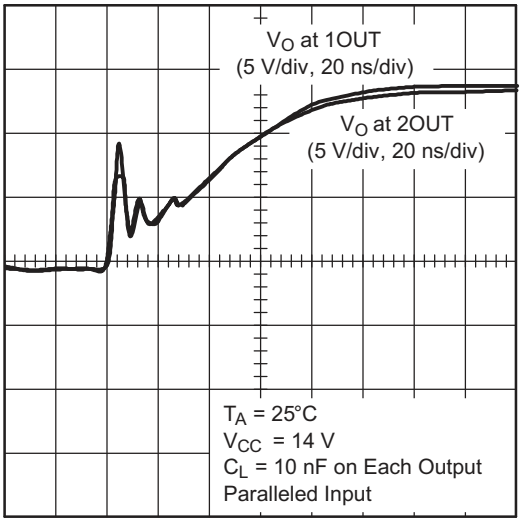


Figure 25. Voltage at 1OUT vs Voltage at 2OUT, Low-to-High Output Delay

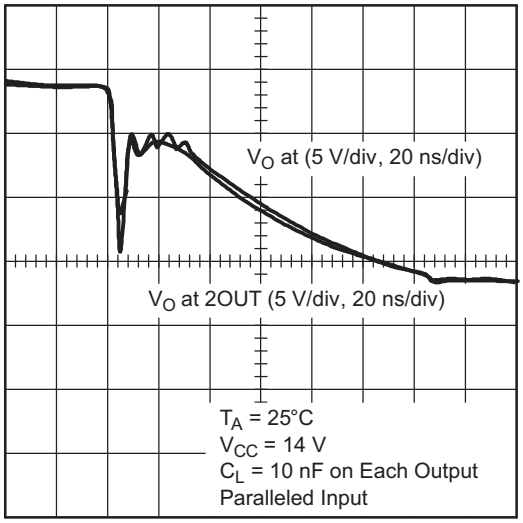


Figure 26. Voltage at 1OUT vs Voltage at 2OUT, High-to-Low Output Delay

A. Input rise and fall times should be ≤10 ns for accurate measurement of ac parameters.

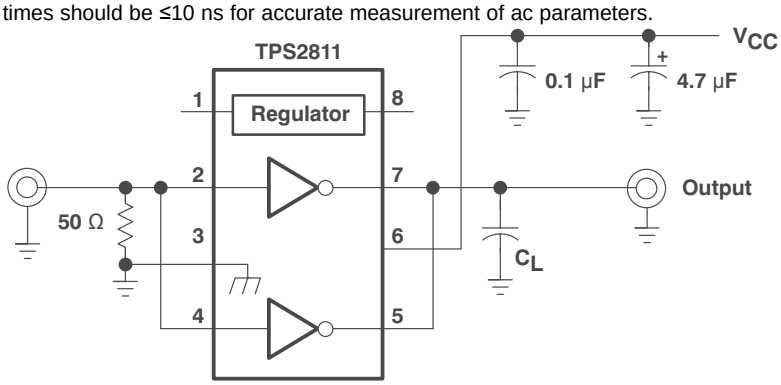


Figure 27. Test Circuit for Measuring Paralleled Switching Characteristics

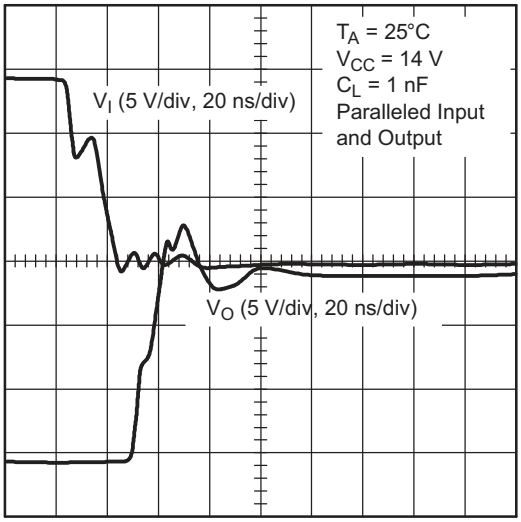


Figure 28. Input Voltage vs Output Voltage, Low-to-High Propagation Delay of Paralleled Drivers

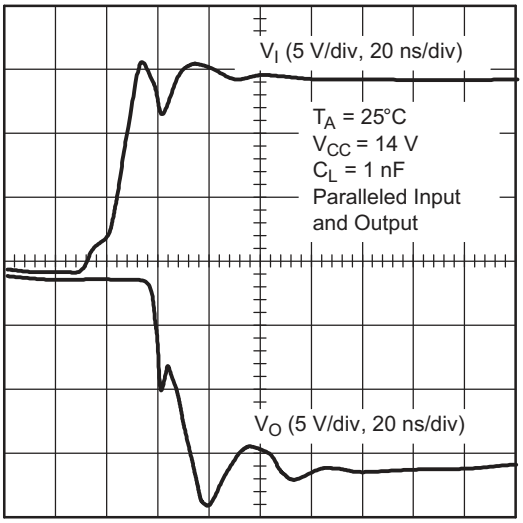


Figure 29. Input Voltage vs Output Voltage, High-to-Low Propagation Delay of Paralleled Drivers

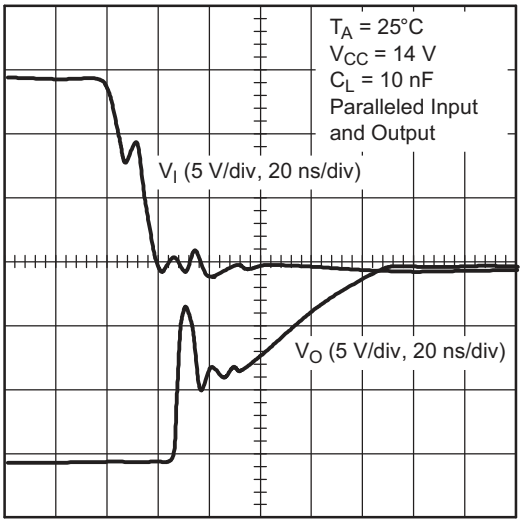


Figure 30. Input Voltage vs Output Voltage, Low-to-High Propagation Delay of Paralleled Drivers

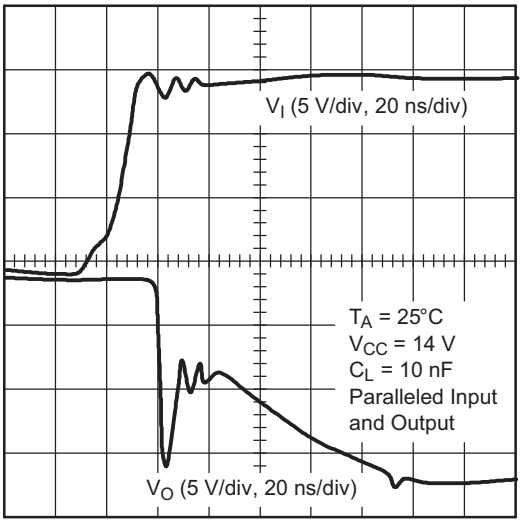


Figure 31. Input Voltage vs Output Voltage, High-to-Low Propagation Delay of Paralleled Drivers

Figures 33 through 47 illustrate the performance of the TPS2811 driving MOSFETs with clamped inductive loads, similar to what is encountered in discontinuous-mode flyback converters. The MOSFETs that were tested range in size from Hex-1 to Hex-4, although the TPS28xx family is only recommended for Hex-3 or below.

The test circuit is shown in Figure 32. The layout rules observed in building the test circuit also apply to real applications. Decoupling capacitor C1 is a 0.1-µF ceramic device, connected between V_{CC} and GND of the TPS2811, with short lead lengths. The connection between the driver output and the MOSFET gate, and between GND and the MOSFET source, are as short as possible to minimize inductance. Ideally, GND of the driver is connected directly to the MOSFET source. The tests were conducted with the pulse generator frequency set very low to eliminate the need for heat sinking, and the duty cycle was set to turn off the MOSFET when the drain current reached 50% of its rated value. The input voltage was adjusted to clamp the drain voltage at 80% of its rating.

As shown, the driver is capable of driving each of the Hex-1 through Hex-3 MOSFETs to switch in 20 ns or less. Even the Hex-4 is turned on in less than 20 ns. Figures 45, 46 and 47 show that paralleling the two drivers in a package enhances the gate waveforms and improves the switching speed of the MOSFET. Generally, one driver is capable of driving up to a Hex-4 size. The TPS2811 family is even capable of driving large MOSFETs that have a low gate charge.

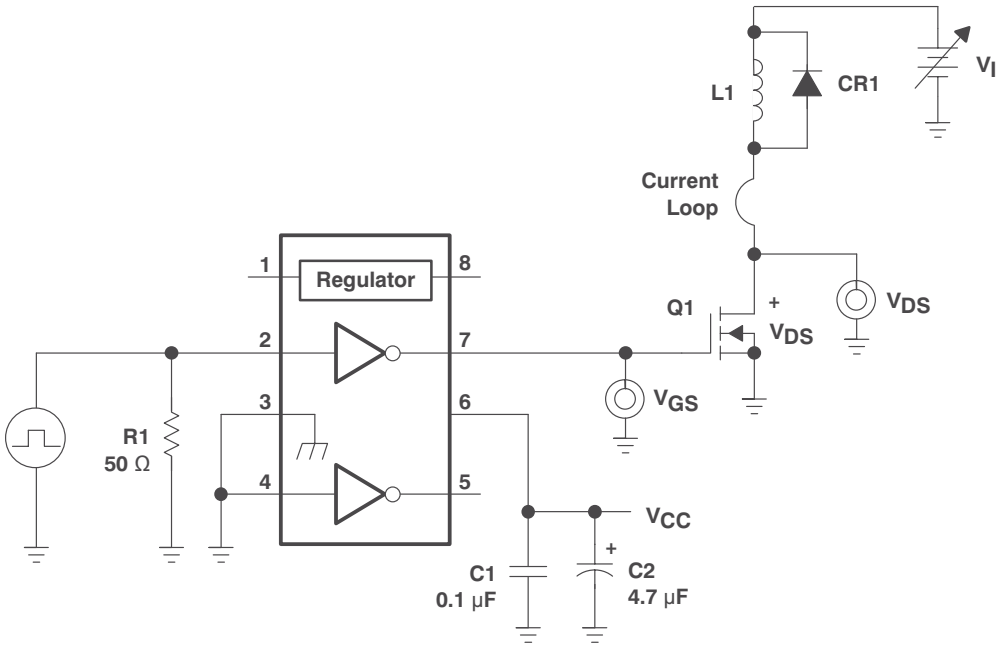


Figure 32. TPS2811 Driving Hex-1 through Hex-4 Devices

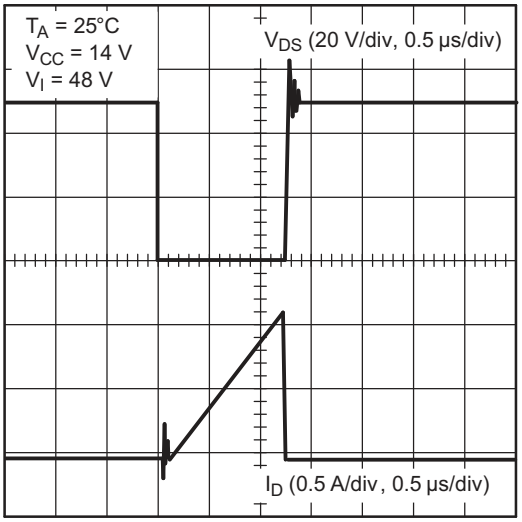


Figure 33. Drain-Source Voltage vs Drain Current, TPS2811 Driving an IRFD014 (Hex-1 Size)

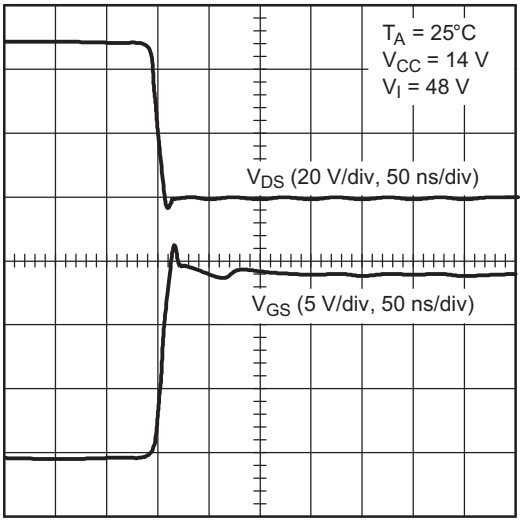


Figure 34. Drain-Source Voltage vs Gate-Source Voltage, at Turn-on, TPS2811 Driving an IRFD014 (Hex-1 Size)

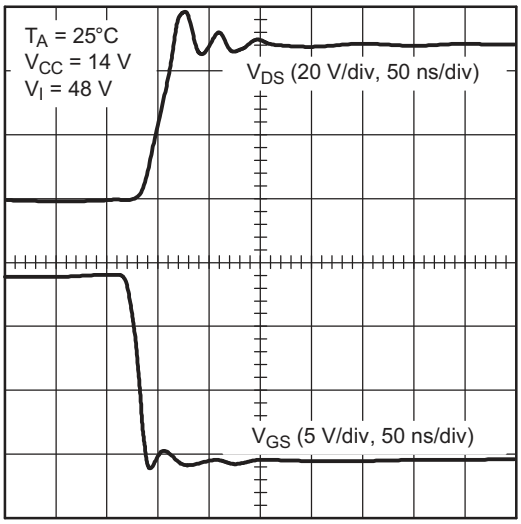


Figure 35. Drain-Source Voltage vs Gate-Source Voltage, at Turn-off, TPS2811 Driving an IRFD014 (Hex-1 Size)

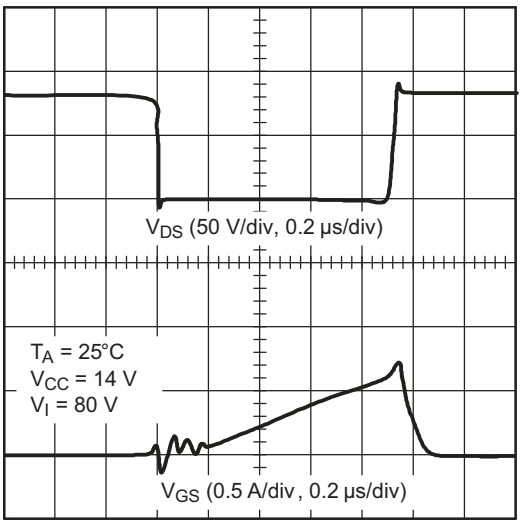


Figure 36. Drain-Source Voltage vs Drain Current, TPS2811 Driving an IRFD120 (Hex-2 Size)

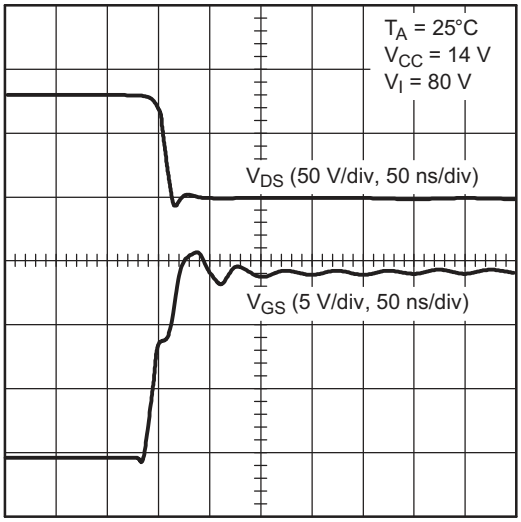


Figure 37. Drain-Source Voltage vs Gate-Source Voltage, at Turn-on, TPS2811 Driving an IRFD120 (Hex-2 Size)

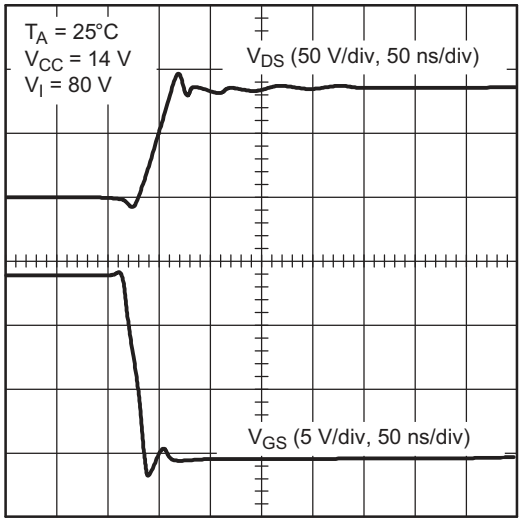


Figure 38. Drain-Source Voltage vs Gate-Source Voltage, at Turn-off, TPS2811 Driving an IRFD120 (Hex-2 Size)

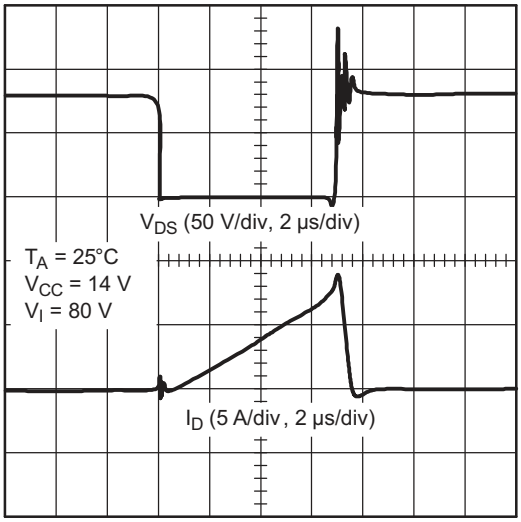


Figure 39. Drain-Source Voltage vs Drain Current, TPS2811 Driving an IRF530 (Hex-3 Size)

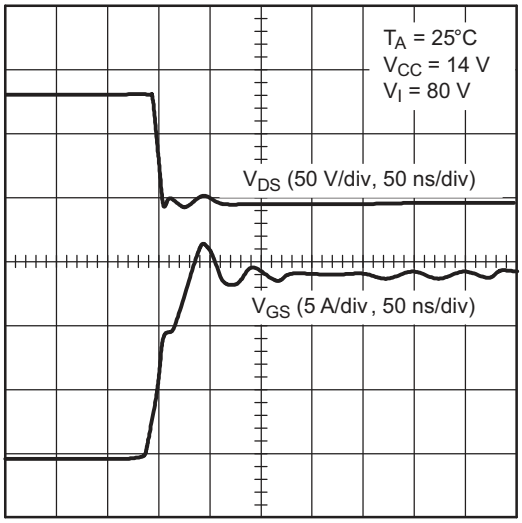


Figure 40. Drain-Source Voltage vs Gate-Source Voltage, at Turn-on, TPS2811 Driving an IRF530 (Hex-3 Size)

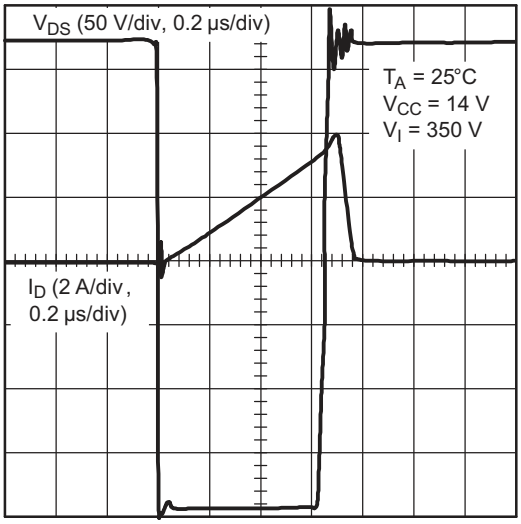


Figure 41. Drain-Source Voltage vs Drain Current, One Driver, TPS2811 Driving an IRF840 (Hex-4 Size)

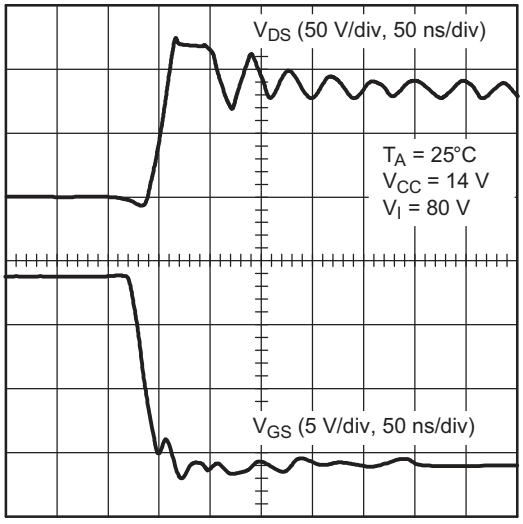


Figure 42. Drain-Source Voltage vs Gate-Source Voltage, at Turn-off, TPS2811 Driving an IRF530 (Hex-3 Size)

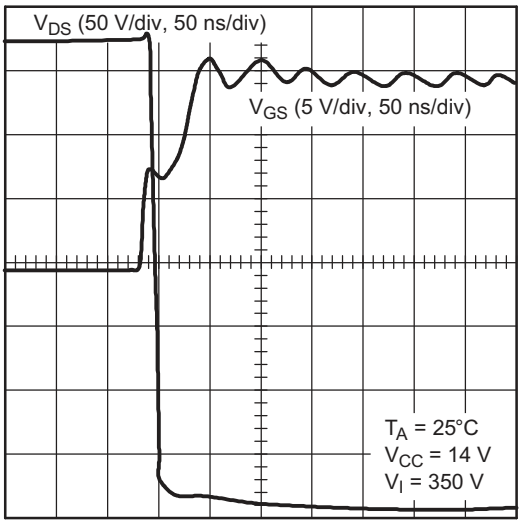


Figure 43. Drain-Source Voltage vs Gate-Source Voltage, at Turn-on, One Driver, TPS2811 Driving an IRF840 (Hex-4 Size)

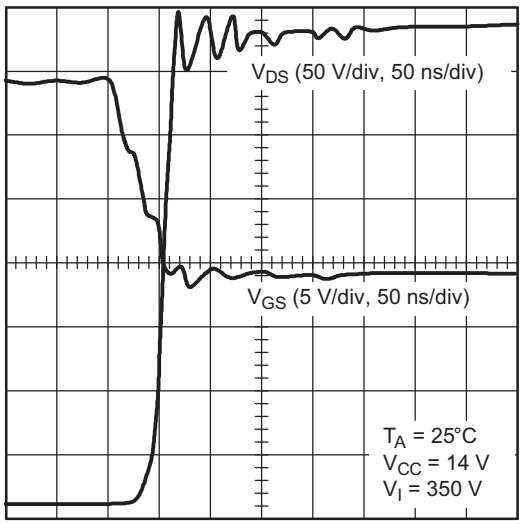


Figure 44. Drain-Source Voltage vs Gate-Source Voltage, at Turn-off, One Driver, TPS2811 Driving an IRF840 (Hex-4 Size)

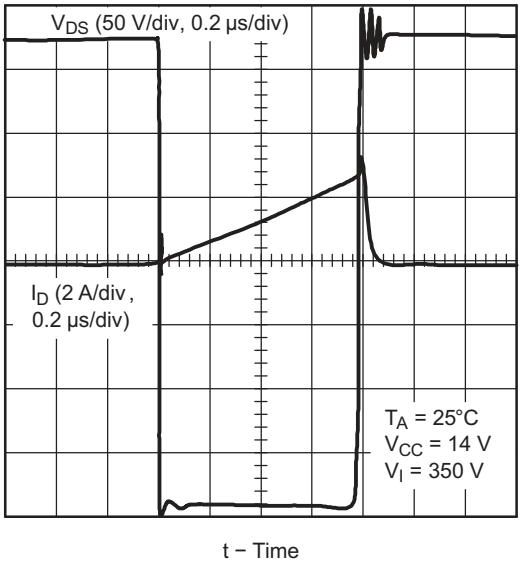


Figure 45. Drain-Source Voltage vs Drain Current, Parallel Drivers, TPS2811 Driving an IRF840 (Hex-4 Size)

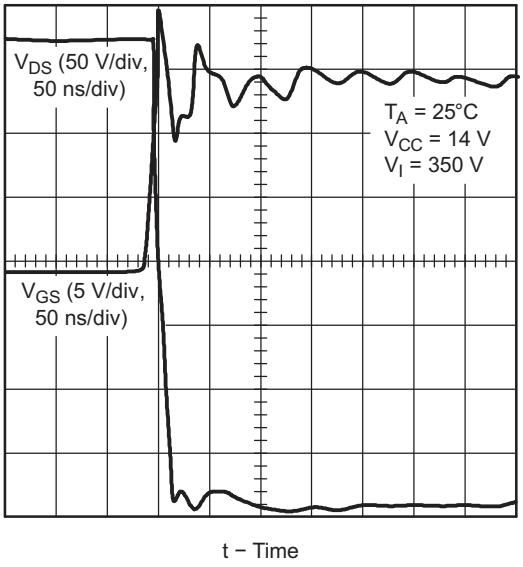


Figure 46. Drain-Source Voltage vs Gate-Source Voltage, at Turn-on, Parallel Drivers, TPS2811 Driving an IRF840 (Hex-4 Size)

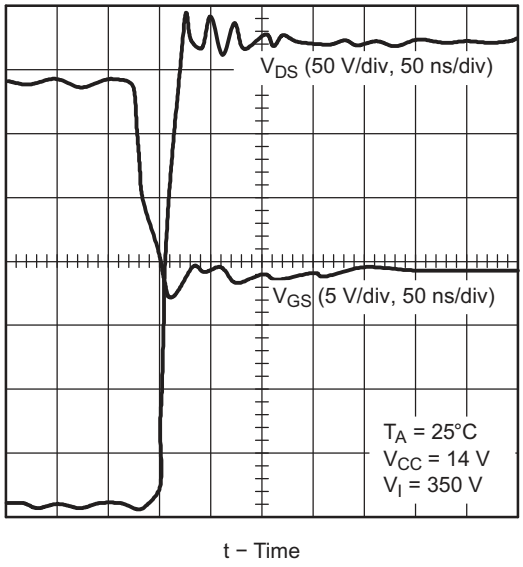
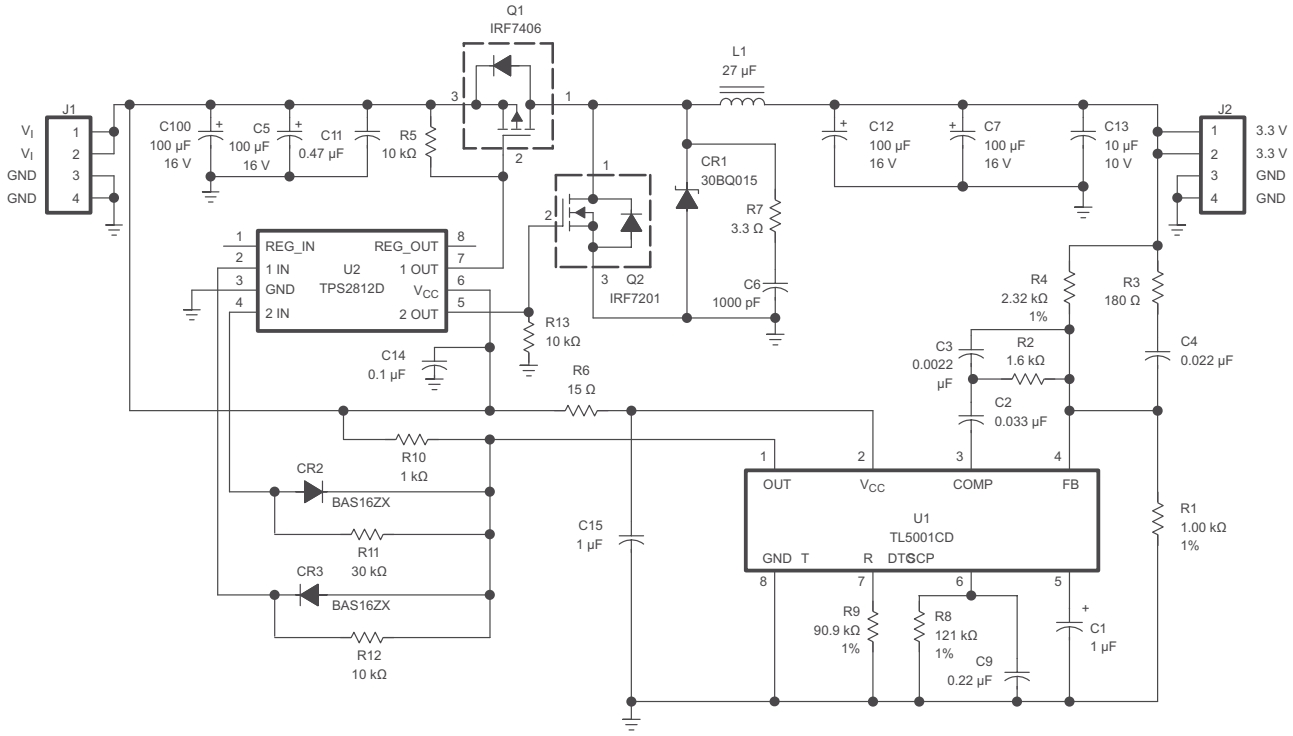


Figure 47. Drain-Source Voltage vs Gate-Source Voltage, at Turn-off, Parallel Drivers, TPS2811 Driving an IRF840 (Hex-4 Size)

Synchronous Buck Regulator

Figure 48 is the schematic for a 100-kHz synchronous-rectified buck converter implemented with a TL5001 pulse-width-modulation (PWM) controller and a TPS2812 driver. The bill of materials is provided in Table 1. The converter operates over an input range from 5.5 V to 12 V and has a 3.3-V output capable of supplying 3 A continuously and 5 A during load surges. The converter achieves an efficiency of 90.6% at 3 A and 87.6% at 5 A. Figures 49 and 50 show the power switch switching performance. The output ripple voltage waveforms are documented in Figures 54 and 55.

The TPS2812 drives both the power switch, Q2, and the synchronous rectifier, Q1. Large shoot-through currents, caused by power switch and synchronous rectifier remaining on simultaneously during the transitions, are prevented by small delays built into the drive signals, using CR2, CR3, R11, R12, and the input capacitance of the TPS2812. These delays allow the power switch to turn off before the synchronous rectifier turns on and vice versa. Figure 51 shows the delay between the drain of Q2 and the gate of Q1; expanded views are provided in Figures 52 and 53.



NOTE: If the parasitics of the external circuit cause the voltage to violate the Absolute Maximum Rating for the Output pins, Schottky diodes should be added from ground to output and from output to V_{CC}.

Figure 48. 3.3-V 3-A Synchronous-Rectified Buck Regulator Circuit

Table 2. Bill of Materials, 3.3-V, 3-A Synchronous-Rectified Buck Converter(1)

REFERENCE	DESCRIPTION	VENDOR	
U1	TL5001CD, PWM	Texas Instruments	972-644-5580
U2	TPS2812D, N.I. MOSFET Driver	Texas Instruments	972-644-5580
CR1	3 A, 15 V, Schottky, 30BQ015	International Rectifier	310-322-3331
CR2,CR3	Signal Diode, BAS16ZX	Zetex	516-543-7100
C1	1 µF, 16 V, Tantalum		
C2	0.033 µF, 50 V		
C3	0.0022 µF, 50 V		
C4	0.022 µF, 50 V		
C5,C7,C10,C12	100 µF, 16 V, Tantalum, TPSE107M016R0100	AVX	800-448-9411
C6	1000 pF, 50 V		
C9	0.22 µF, 50 V		
C11	0.47 µF, 50 V, Z5U		
C13	10 µF, 10 V, Ceramic, CC1210CY5V106Z	TDK	708-803-6100
C14	0.1 µF, 50 V		
C15	1.0 µF, 50 V		
J1,J2	4-Pin Header	Nova Magnetics, Inc.	972-272-8287
L1	27 µH, 3 A/5 A, SML5040	International Rectifier	310-322-3331
Q1	IRF7406, P-FET	International Rectifier	310-322-3331
Q2	IRF7201, N-FET		
R1	1.00 kΩ, 1%		
R2	1.6 kΩ		
R3	180 Ω		
R4	2.32 kΩ, 1 %		
R5,R12,R13	10 kΩ		
R6	15 Ω		
R7	3.3 Ω		
R8	121 kΩ, 1%		
R9	90.9 kΩ, 1%		
R10	1 kΩ		
R11	30 kΩ		

(1) Unless otherwise specified, capacitors are X7R ceramics, and resistors are 5%, 1/10 W.

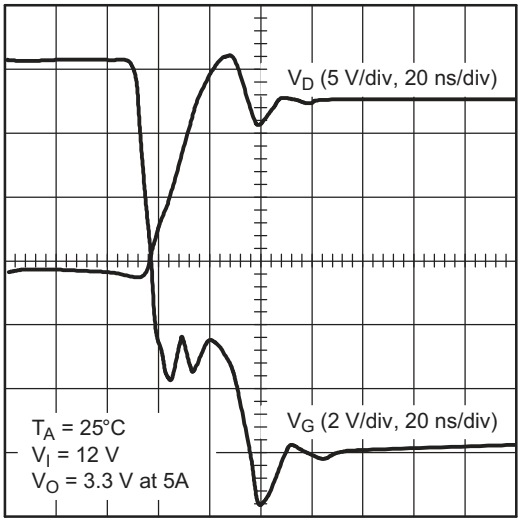


Figure 49. Q1 Drain Voltage vs Gate Voltage, at Switch Turn-on

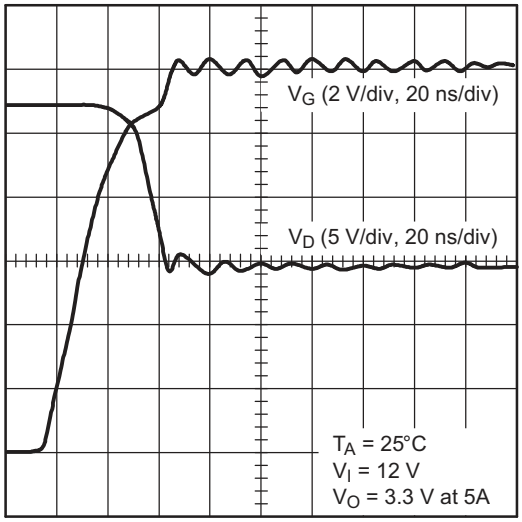


Figure 50. Q1 Drain Voltage vs Gate Voltage, at Switch Turn-off

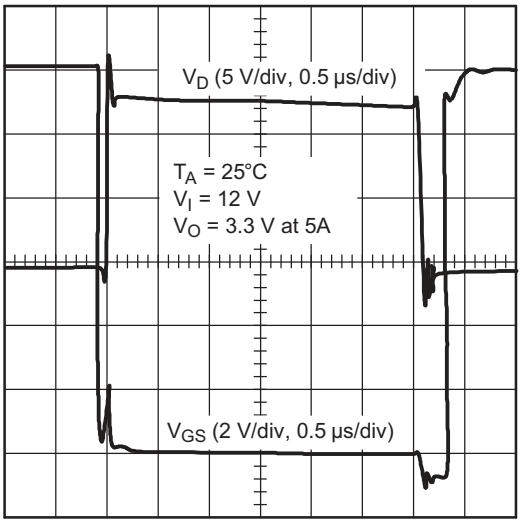


Figure 51. Q1 Drain Voltage vs Q2 Gate-Source Voltage

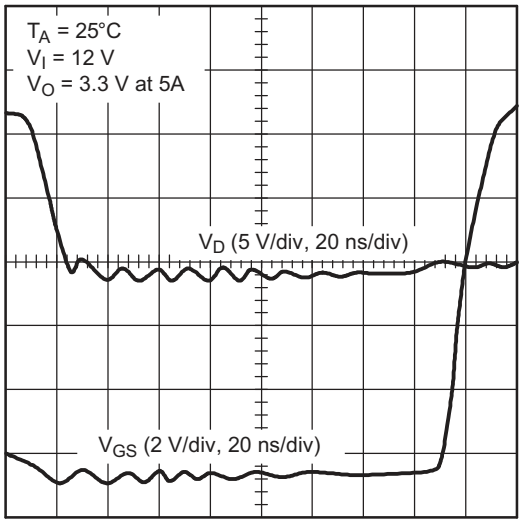


Figure 52. Q1 Drain Voltage vs Q2 Gate-Source Voltage

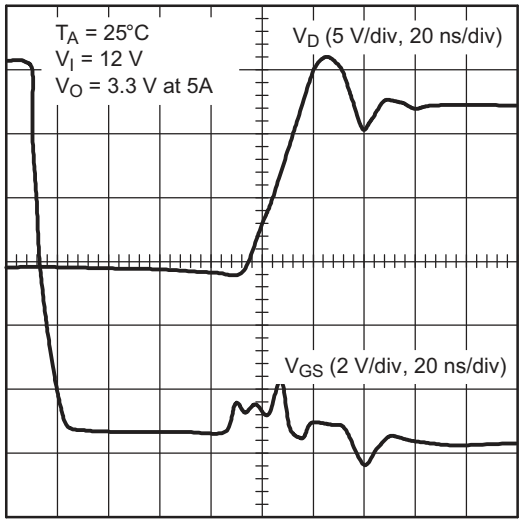


Figure 53. Q1 Drain Voltage vs Q2 Gate-Source Voltage

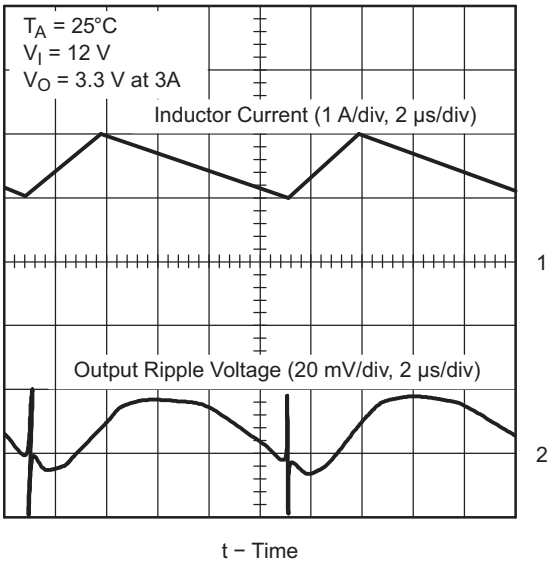


Figure 54. Output Ripple Voltage vs Inductor Current, at 3 A

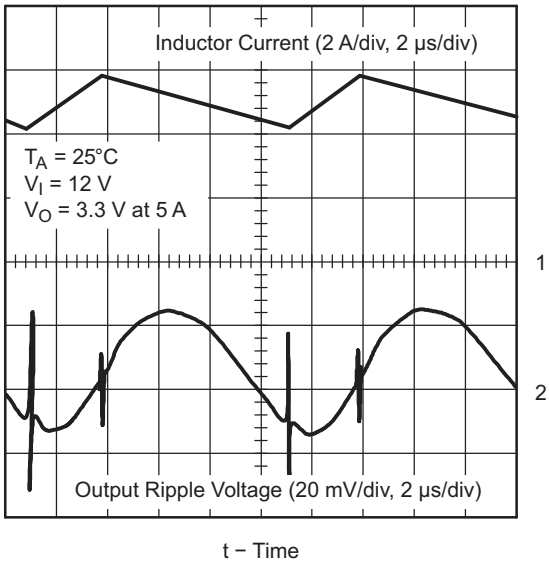


Figure 55. Output Ripple Voltage vs Inductor Current, at 5 A

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2811QPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	2811Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS2811-Q1 :

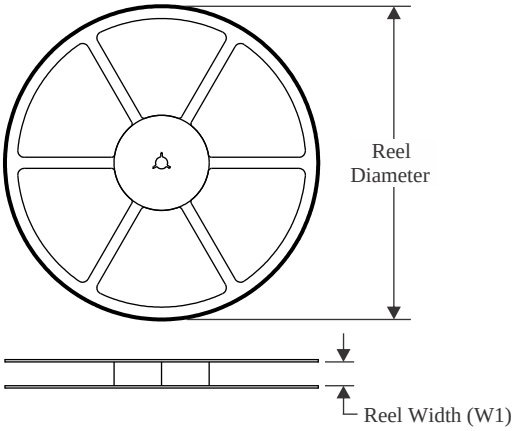
- Catalog: TPS2811

NOTE: Qualified Version Definitions:

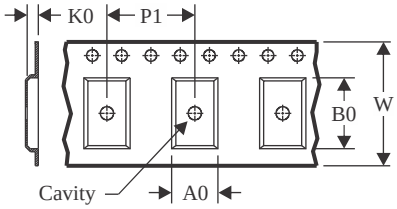
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

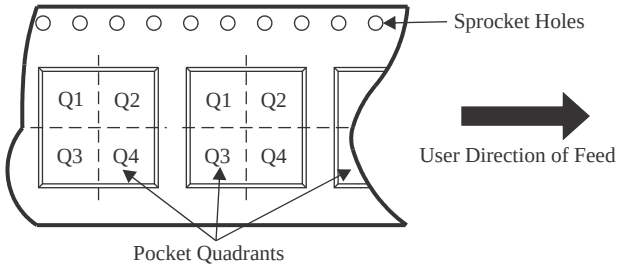


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

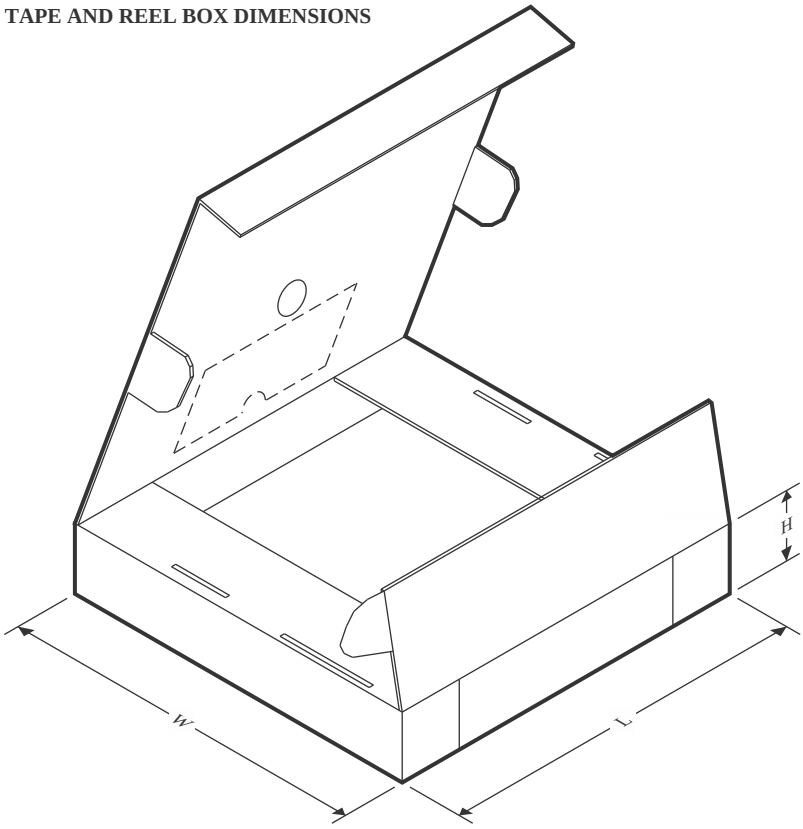
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2811QPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

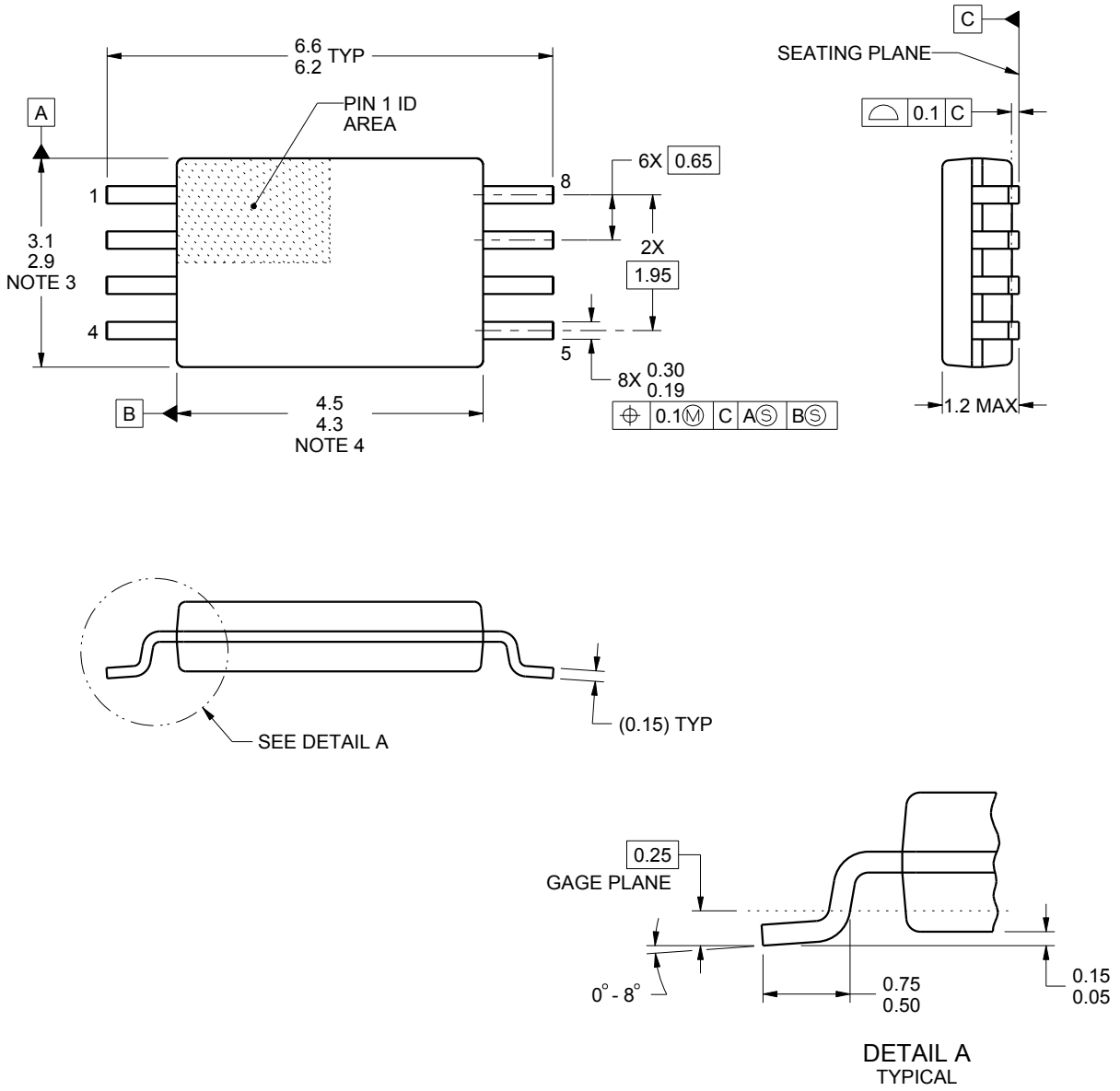
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2811QPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0008A

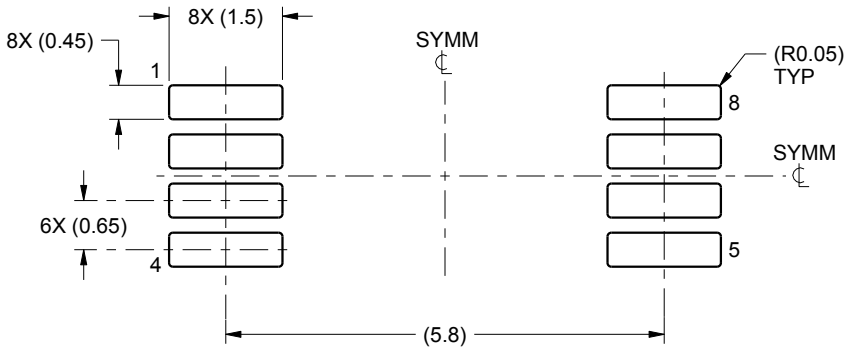
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

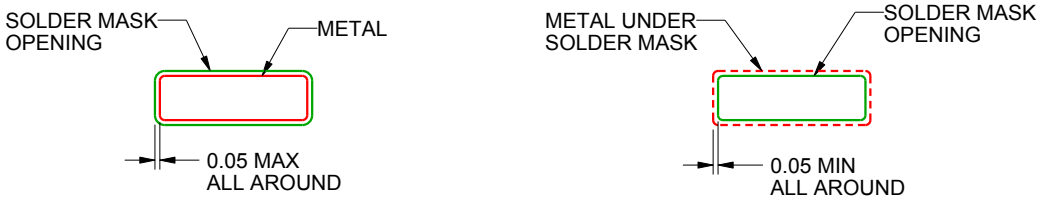


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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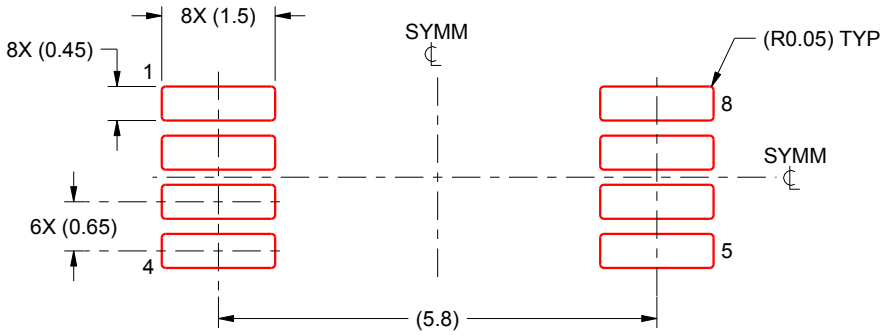
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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