April 2005

FAN8741/FAN8742
Spindle Motor and 6-CH Driver
[Spindle(PWM), Sled 2-CH(PWM) 4-CH(Linear)]

Features

Common

- Built-in thermal shutdown circuit (TSD)
- 8 Independent voltage sources
- Corresponds to 3.3V or 5V DSP
- 4 selectable mute inputs

Spindle

- Output PWM mode control
- FG output: open collector type
- Selectable brake(short & reverse brake)
- Built-in hall bias
- 180^{o} commutation(compatible with conventional BLDC spindle motor)
- Built in short-through protection function

BTL(Sled 2-channels)

- Output PWM mode control
- Built in short-through protection function

BTL(Other 4-channels)

- Output linear mode control

Typical Applications

- CD-ROM
- CD-RW
- DVD-ROM
- DVD-RAM
- DVD Player (DVDP)
- Other compact disk media
- Game consoles

Description

Suitable for a 3-phase BLDC (Brush-Less Direct Current) spindle motor driver with PWM, the monolithic FAN8741/FAN8742 IC also includes 2-ch motor drivers with PWM for sled motors and 4-ch linear drivers which drive the focus actuator, tracking actuator, tilt actuator, and loading motor in optical media applications. Designed specifically for high-speed/high-density optical media applications, the FAN8741/FAN8742's power stage is created by D-MOS transistors which have extremely low RDS_{ON}. This enables less heat generation and guarantees improved reliability.

The FAN8741G/FAN8742G is available in a 56-SSOP-HS package, which has high-power dissipation and the leadframe is exposed to the top side.

The FAN8741MTF/FAN8742MTF is available in a 56-TSSOP-EP package, which is very thin and the leadframe is exposed to the bottom side.

Ordering Information

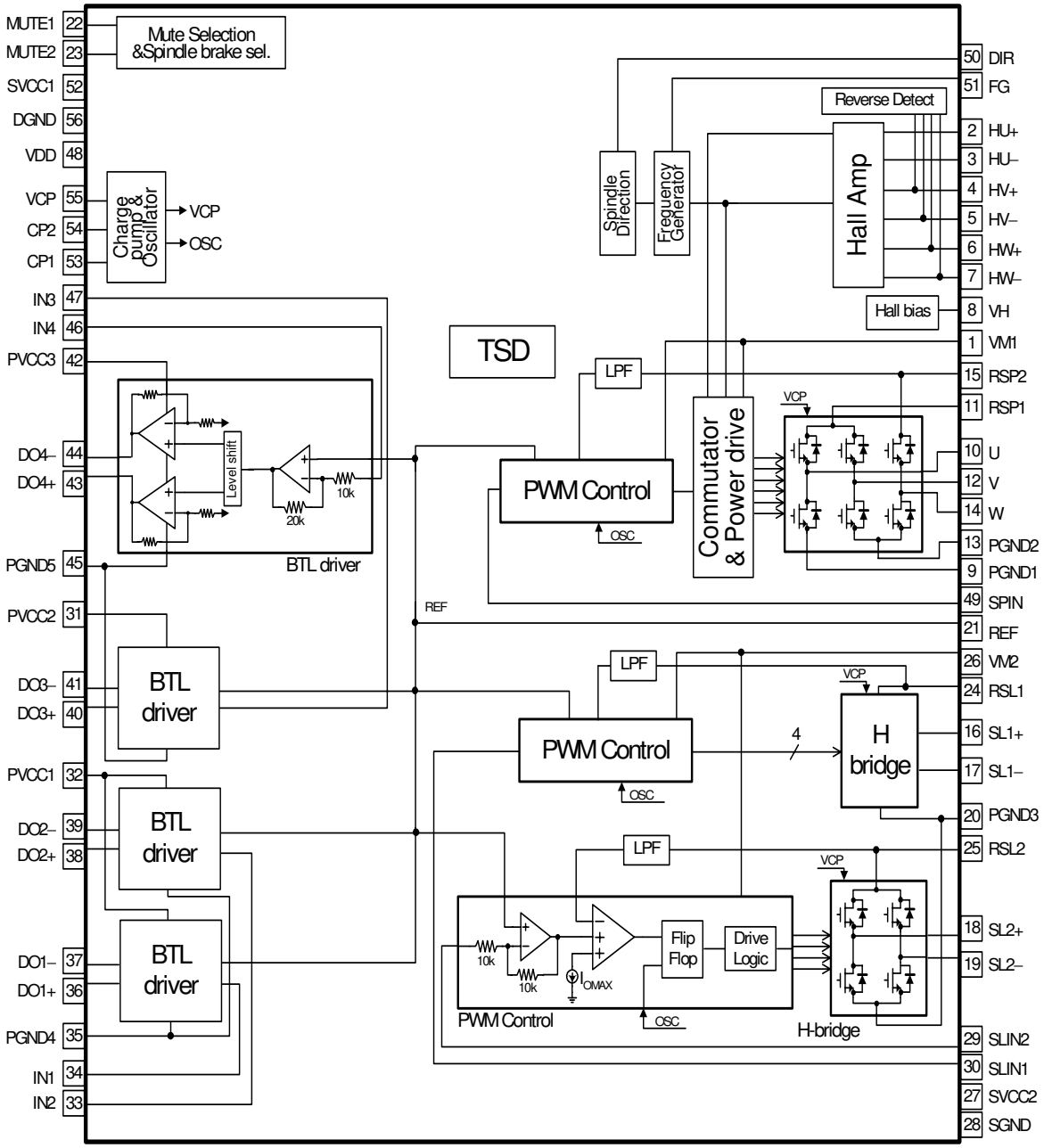
Device	Package	Operating Temp.
FAN8741G	56-SSOP-HS	–25°C to +75°C
FAN8741GX	56-SSOP-HS	–25°C to +75°C
FAN8742G	56-SSOP-HS	–25°C to +75°C
FAN8742GX	56-SSOP-HS	–25°C to +75°C
FAN8741MTF	56-TSSOP-EP	–25°C to +75°C
FAN8741MTFX	56-TSSOP-EP	–25°C to +75°C
FAN8742MTF	56-TSSOP-EP	–25°C to +75°C
FAN8742MTFX	56-TSSOP-EP	–25°C to +75°C

HS=HeatSlug, EP=ExposedPad

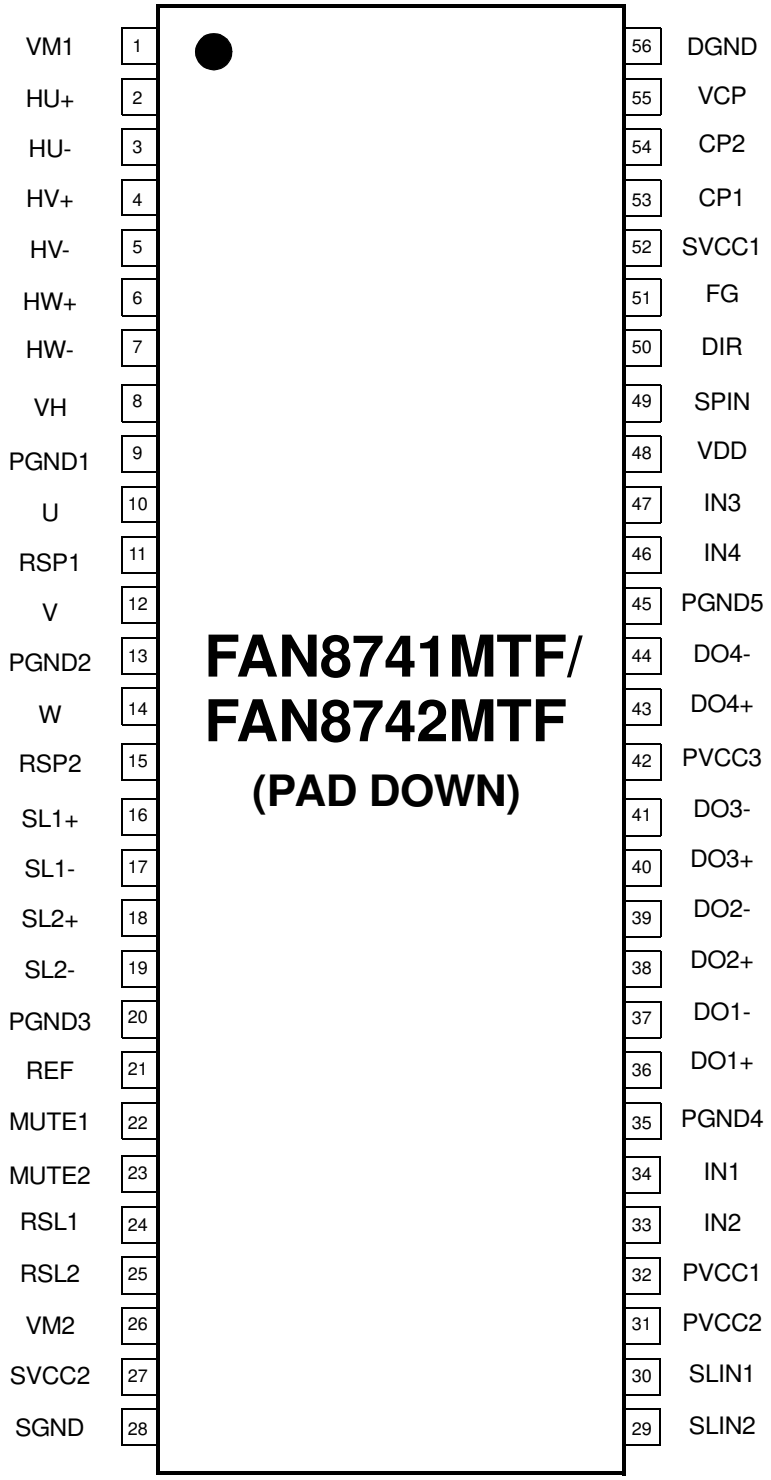
X:Tape & Reel type

FAN8741:FG3X
FAN8742:FG1X

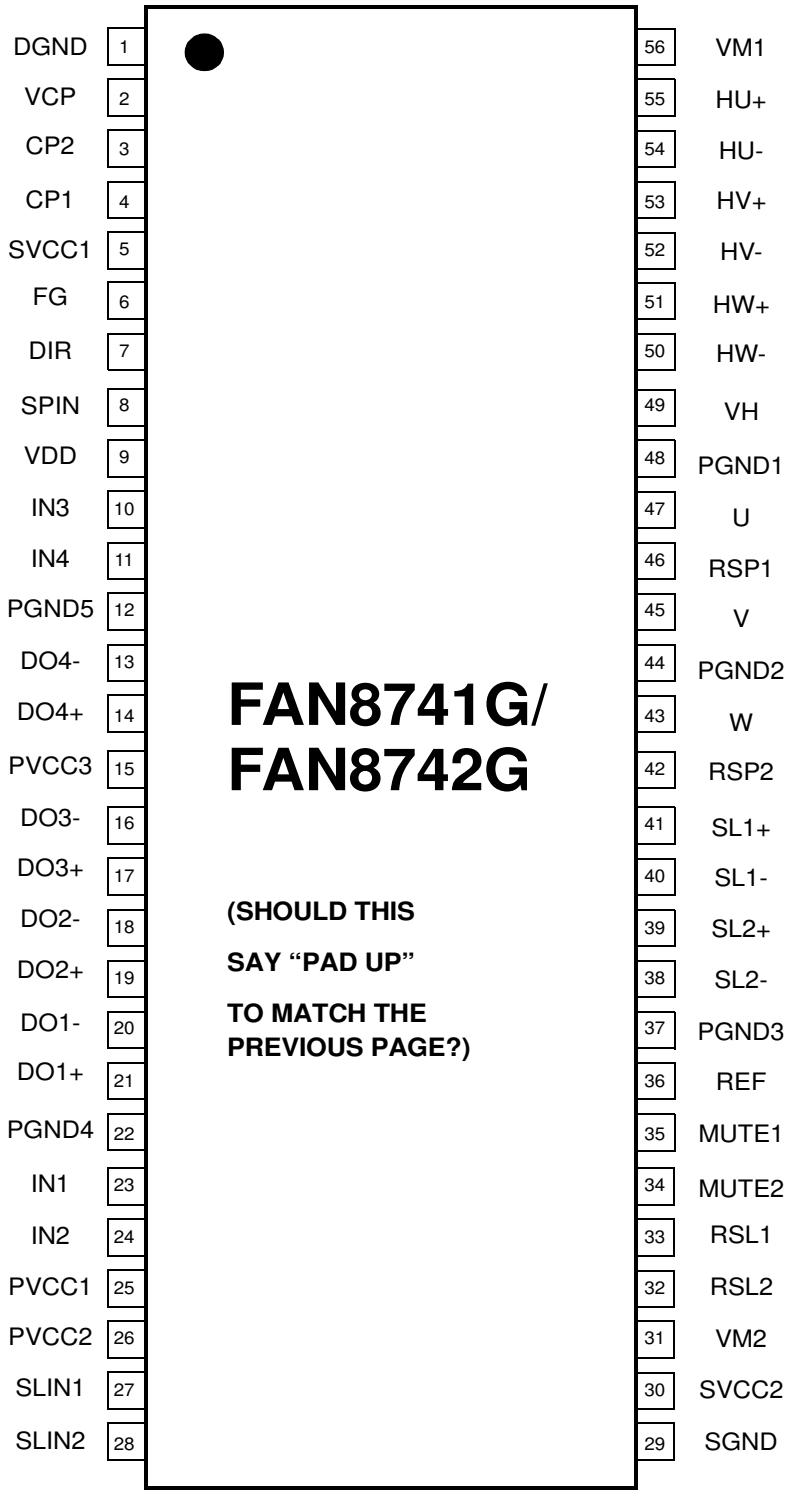
Internal Block Diagram (Pins numbered according to the FAN8741MTF--Leadframe exposed to the bottom)



Pin Assignments(Leadframe exposed to the bottom side)



Pin Assignments (Leadframe exposed to the top side)



Pin Definitions

Pin Number (exposed to bottom)	Pin Number (exposed to top)	Pin Name	I/O	Pin Function Description
1	56	VM1	P	Power supply for spindle
2	55	HU+	A	Hall signal input(Hu+)
3	54	HU-	A	Hall signal input(Hu-)
4	53	HV+	A	Hall signal input(Hv+)
5	52	HV-	A	Hall signal input(Hv-)
6	51	HW+	A	Hall signal input(Hw+)
7	50	HW-	A	Hall signal input(Hw-)
8	49	VH	A	Hall bias
9	48	PGND1	P	Power ground 1 for spindle channel
10	47	U	A	3-phase output U for spindle
11	46	RSP1	A	Spindle current sensing 1
12	45	V	A	3-phase output V for spindle
13	44	PGND2	P	Power ground 2 for spindle channel
14	43	W	A	3-phase output W for spindle
15	42	RSP2	A	Spindle current sensing 2
16	41	SL1+	A	Sled channel 1 drive output +
17	40	SL1-	A	Sled channel 1 drive output -
18	39	SL2+	A	Sled channel 2 drive output +
19	38	SL2-	A	Sled channel 2 drive output -
20	37	PGND3	P	Power ground for sled channels
21	36	REF	A	Reference voltage input
22	35	MUTE1	A	Mute input 1
23	34	MUTE2	A	Mute input 2
24	33	RSL1	A	Sled current sensing 1
25	32	RSL2	A	Sled current sensing 2
26	31	VM2	P	Power supply for sled
27	30	SVCC2	P	Power supply for BTL Pre driver
28	29	SGND	P	Signal ground for BTL signal block
29	28	SLIN2	A	Sled channel 2 input
30	27	SLIN1	A	Sled channel 1 input
31	26	PVCC2	P	Power supply for BTL CH3
32	25	PVCC1	P	Power supply for BTL CH1/2
33	24	IN2	A	Channel 2 input
34	23	IN1	A	Channel 1 input
35	22	PGND4	P	Power ground for BTL CH1/2
36	21	DO1 +	A	Channel 1 drive output +
37	20	DO1 -	A	Channel 1 drive output -
38	19	DO2 +	A	Channel 2 drive output +
39	18	DO2 -	A	Channel 2 drive output -
40	17	DO3 +	A	Channel 3 drive output +
41	16	DO3 -	A	Channel 3 drive output -
42	15	PVCC3	P	Power supply for BTL CH4

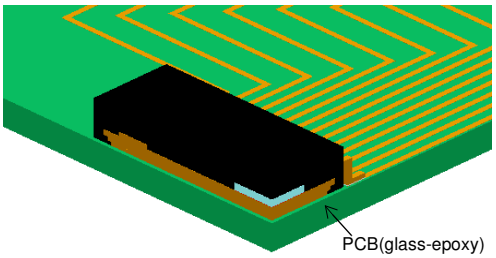
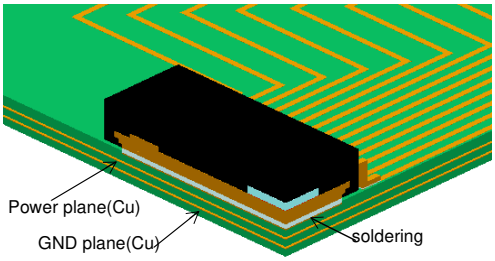
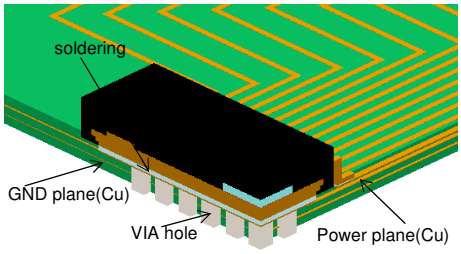
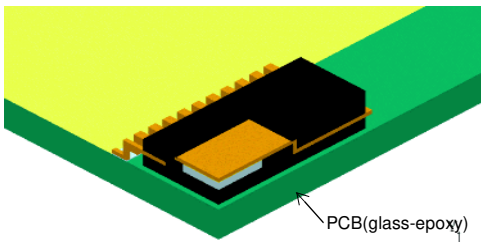
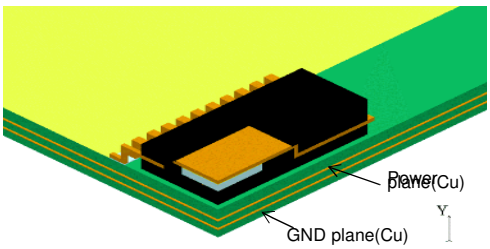
Pin Definitions(continued)

Pin Number (exposed to bottom)	Pin Number (exposed to top)	Pin Name	I/O	Pin Function Description
43	14	DO4 +	A	Channel 4 drive output +
44	13	DO4 -	A	Channel 4 drive output -
45	12	PGND5	P	Power ground for BTL CH3/4
46	11	IN4	A	Channel 4 input
47	10	IN3	A	Channel 3 input
48	9	VDD	P	Power supply for digital block
49	8	SPIN	A	Spindle channel input
50	7	DIR	O	Spindle rotational direction output
51	6	FG	O	Spindle frequency generator FAN8741MTF=3X, FAN8742MTF=1X
52	5	SVCC1	P	Power supply for signal block
53	4	CP1	A	Charge pump capacitor1
54	3	CP2	A	Charge pump capacitor2
55	2	VCP	A	Charge pumped voltage
56	1	DGND	P	Ground for digital block

Absolute Maximum Ratings (Ta = 25°C)

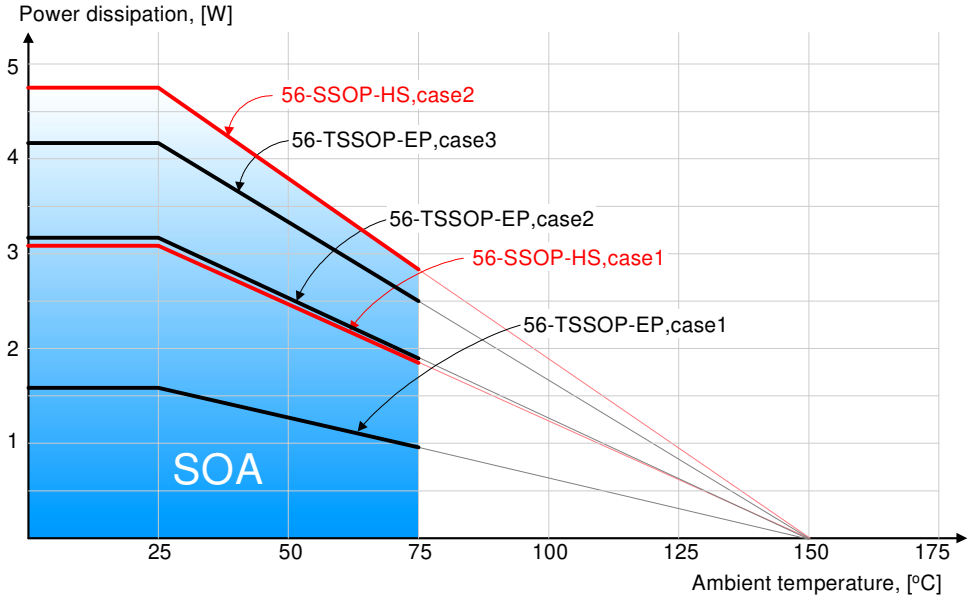
Parameter	Value	Unit
Supply Voltage (Signal block)	7	V
Supply Voltage (Digital block)	7	V
Supply Voltage (Spindle/Sled/BTL/BTL pre driver)	15	V
Power Dissipation (56-TSSOP-EP)	1.6 / 3.2 / 4.1	W
Power Dissipation (56-SSOP-HS)	3.1 / 4.7	W
Operating Temperature Range	-20 to +75	°C
Storage Temperature Range	-40 to +150	°C
Maximum Output Current (Spindle)	2.0	A
Maximum Output Current (CH1/2/3/4, Sled)	1.0	A

NOTE:

56-TSSOP-EP, Case 1	56-TSSOP-EP, Case 2	Remark
		Pd is measured base on the JEDEC/ STD(JESD 51-2)
Pd=1.6 W	Pd=3.2 W	
56-TSSOP-EP, Case 3		
		
Pd=4.1 W		
56-SSOP-HS, Case 1	**56-SSOP-HS, Case 2**	
		
Pd=3.1W	Pd=4.7W	

1. 56-TSSOP-EP, Case 1: Single layer PCB with 1 signal plane only, PCB size is 76mm × 114mm × 1.6mm.
2. 56-TSSOP-EP, Case 2: Multi layer PCB with 1 signal, 1 power and 1 ground planes, PCB size is 76mm × 114mm × 1.6mm, Cu plane sizes for power and ground is 74mm × 62mm × 0.035mm. Down pad of IC is soldered on the PCB.
3. 56-TSSOP-EP, Case 3: PCB condition is same to case 2 except via holes, which penetrate PCB all layers. Down pad of IC is soldered on the PCB.
4. 56-SSOP-HS, Case 1: Single layer PCB with 1 signal plane only, PCB size is 76mm × 114mm × 1.6mm.
5. 56-SSOP-HS, Case 2: Multi layer PCB with 1 signal, 1 power and 1 ground planes, PCB size is 76mm × 114mm × 1.6mm, Cu plane sizes for power and ground is 74mm × 62mm × 0.035mm.
6. Power dissipation is reduced by -12.8mW/°C for using above Ta=25°C in 56-TSSOP-EP, case 1.
7. Power dissipation is reduced by -25.6mW/°C for using above Ta=25°C in 56-TSSOP-EP, case 2.
8. Power dissipation is reduced by -32.8mW/°C for using above Ta=25°C in 56-TSSOP-EP, case 3.
9. Power dissipation is reduced by -24.8mW/°C for using above Ta=25°C in 56-SSOP-HS, case 1.
10. Power dissipation is reduced by -37.6mW/°C for using above Ta=25°C in 56-SSOP-HS, case 2.
11. Do not exceed P_D and SOA (Safe Operating Area).

Power Dissipation Curve



Recommended Operating Conditions (Ta = 25°C)

Parameter	Min.	Typ.	Max.	Unit
Supply Voltage (Spindle Signal block)	4.5	5	5.5	V
Supply Voltage (Digital block)	4.5	5	5.5	V
Supply Voltage (Spindle driver)	4.5	12	13.2	V
Supply Voltage (Sled driver)	4.5	12	13.2	V
Supply Voltage (BTL driver)	4.5	12	SV_{CC2}	V
Supply Voltage (BTL signal block)	4.5	12	13.2	V
Output current(Spindle)	-	1.0	1.5	A
Output current(Focus, Tracking, Loading)	-	0.5	0.8	A
Output current(Sled)	-	0.5	0.8	A

ELECTRICAL CHARACTERISTICS (Ta = 25°c)

(Ta=25°C, SVCC1=VDD=PVCC1=VM2=5V,VM1=SVCC2=PVCC2=PVCC3=12V unless otherwise noted)

Parameter	Condition	Min.	Typ.	Max.	Units
COMMON PART					
Quiescent Circuit Current 1	Mute1=L, Mute2=L	-	1	-	mA
		-	1	-	
Quiescent Circuit Current 2	Mute1=L, Mute2=H	-	1.5	-	mA
		-	9.5	-	
Quiescent Circuit Current 3	Mute1=H, Mute2=H	-	4	-	mA
		-	13	-	
Mute Low Voltage	MUTE=variation	-	-	0.8	V
Mute High Voltage	MUTE=variation	3.0	-	-	V
Mute Input Current	MUTE=5V	-	130	-	μA
Charge Pump Voltage 1	I_{PUMP}=0mA	-	19	-	V
Charge Pump Voltage 2	I_{PUMP}=-1mA	-	18	-	V
THERMAL SHUTDOWN					
Operating Temperature*	-	-	150	-	°C
Hysteresis Temperature*	-	-	25	-	°C
SPINDLE DRIVE PART					
Control Input Deadzone11	SPIN>VREF	20	50	100	mV
Control Input Deadzone12	SPIN<VREF	-100	-50	-20	mV
Control Voltage Input Range		0	-	5	V
Output Gain	$G_{MSP}=G_{VO}/RCS_{SP}$, $RCS_{SP}=0.33\Omega$, $G_{VO}=1$[V/V]	2.55	3.0	3.45	A/V
Output On Resistance(upper)	Io=500mA	-	0.4	-	Ω
Output On Resistance(lower)	Io=500mA	-	0.4	-	Ω
Output Limit Current	$RCS_{SP}=0.33\Omega$	-	1.5	-	A
Hall Amp Common Mode Input Range	-	1	-	4	V
Minimum Hall Input Level*	-	50	-	-	mV
Hall Bias Output Voltage	I_{HB}=10mA	0.5	1.0	1.5	V
Hall Bias Input Current		-	1	5	μA
FG Low Voltage	I_{FG}=3mA	-	-	0.5	V
DIR Low Voltage	I_{DIR}=3mA	-	-	0.5	V
SLED DRIVE PART					
Control Input Deadzone21	SLIN1/SLIN2 > VREF	0	15	30	mV
Control Input Deadzone22	SLIN1/SLIN2 < VREF	-30	-15	0	mV
Output Gain	$G_{MSL}=G_{VO}/RCS_{SL}$, $RCS_{SL}=1\Omega$, $G_{VO}=1$[V/V]	0.85	1.0	1.15	A/V
Output On Resistance(upper)	Io=250mA	-	1.0	-	Ω
Output On Resistance(lower)	Io=250mA	-	1.0	-	Ω
Output Limit Current	$RCS_{SL}=1\Omega$	-	0.5	-	A

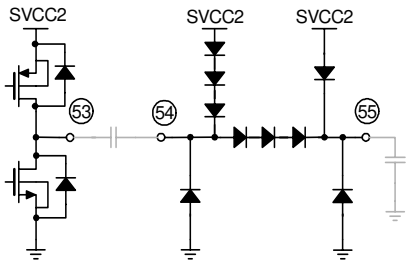
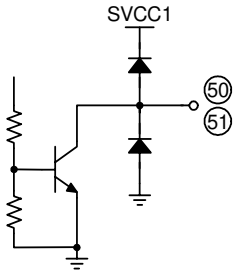
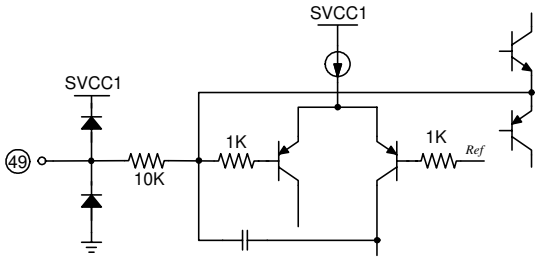
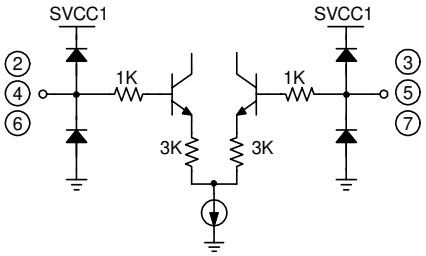
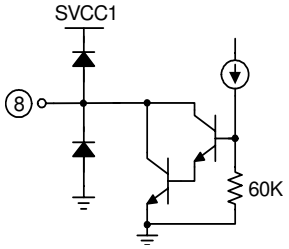
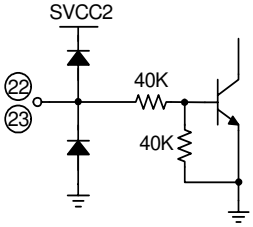
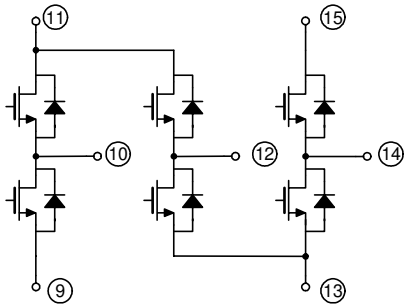
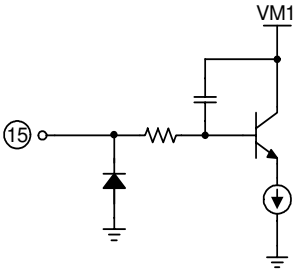
* : Design guarantee specification

ELECTRICAL CHARACTERISTICS (Ta = 25°C, continued)

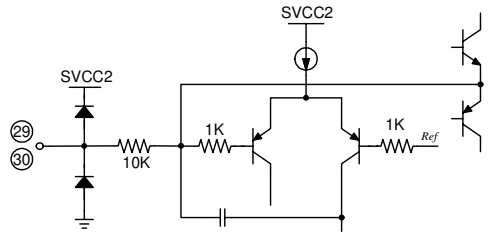
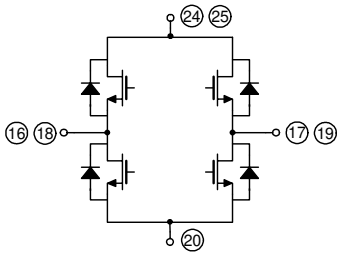
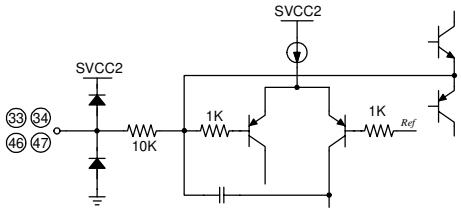
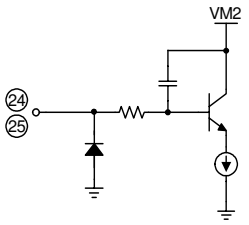
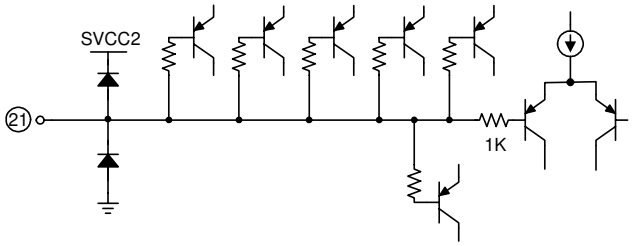
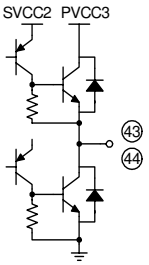
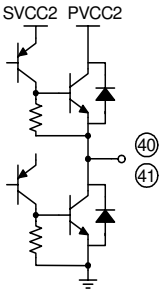
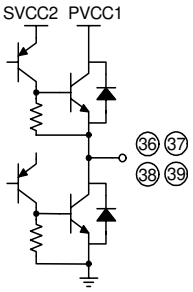
(Ta=25°C, SVCC1=VDD=PVCC1=VM2=5V,VM1=SVCC2=PVCC2=PVCC3=12V unless otherwise noted)

Parameter	Condition	Min.	Typ.	Max.	Units
CH1,CH2 DRIVE PART (TYPICALLY ACTUATOR DRIVER)					
Output Saturation Voltage H	I_O=500mA		0.5		V
Output Saturation Voltage L	I_O=500mA		0.5		V
Closed Loop Voltage Gain	-	16.5	18	19.5	dB
Output Offset Voltage	VREF=IN1=IN2=1.65V	-50	-	50	mV
CH3,CH4 DRIVE PART (TYPICALLY TILT,LOADING DRIVER)					
Output Saturation Voltage H	I_O=500mA		1.0		V
Output Saturation Voltage L	I_O=500mA		0.5		V
Closed Loop Voltage Gain	-	16.5	18	19.5	dB
Output Offset Voltage	VREF=IN3=IN4=1.65V	-50	-	50	mV
CH1,CH3 GAIN DIFFERENCE SPEC (TYPICALLY FOCUS,TILT DRIVER)					
CH1-CH3 Gain Difference	G_{VFT12} - G_{VFT34}	-0.5	0	0.5	dB

Equivalent Circuits(Pins numbered according to FAN8741MTF)

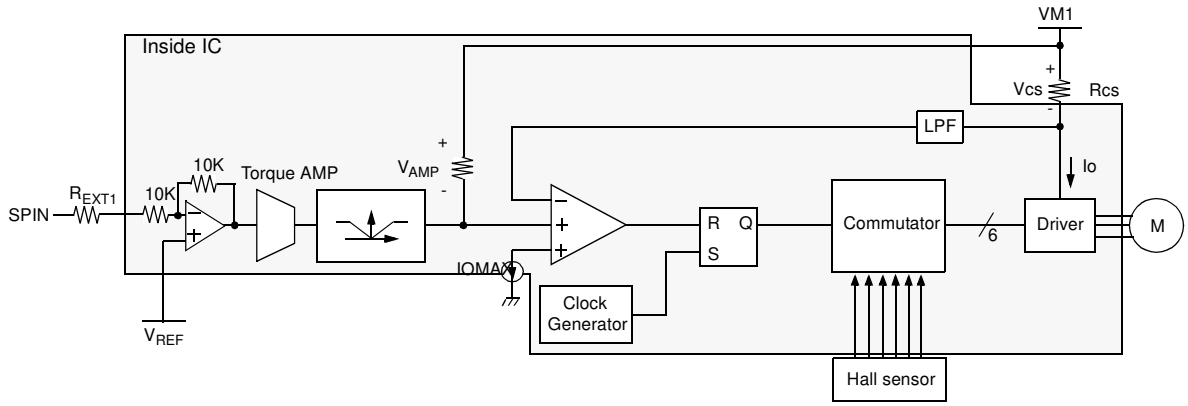
Charge Pump Outputs	FG/DIR Outputs
	
Spin Input	**Hall Inputs**
	
Hall Bias Input	**Mute1 & 2 Inputs**
	
Spindle Drive Outputs	**Spindle Current Sensing Input**
	

Equivalent Circuits(continued)(Pins numbered according to FAN8741MTF)

Sled 1 & 2 Inputs	Sled Drive Outputs
	
CH1/2/3/4 (BTL Channels) Inputs	**Sled 1 & 2 Current Sensing Inputs**
	
Reference Input	**CH4 Outputs**
	
CH3 Outputs	**CH1 & 2 Outputs**
	

Application Information

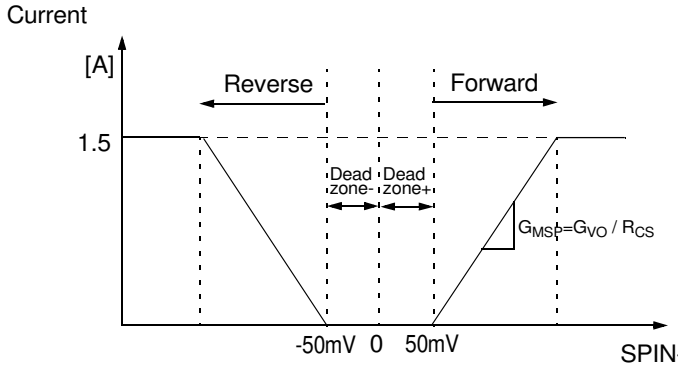
1. Torque Control & Output Current Control of 3-phase Bldc Motor



1) By amplifying the voltage difference between V_{REF} and SPIN from Servo IC(or DSP), the Torque AMP produces the input voltage(V_{AMP}) which means input current command.
2) The output current (I_O) is converted into the voltage (V_{CS}) through the sense resistor (R_{CS}) and compared with the V_{AMP}.
3) The clock generator always make the RS latch become set periodically, this enables the output driver's on state, when the V_{CS} and the V_{AMP} are equal the state becomes off.
4) By the negative feedback loop, the sensed output voltage V_{CS} equals to the V_{AMP}.
5) Commuting sequence is selected by hall sensor input, and the minimum hall input is 50mV.
6) The gain and limit currents are calculated as shown in the table below.($Gvo=V_{AMP}/(SPIN-V_{REF})=1[V/V]$).

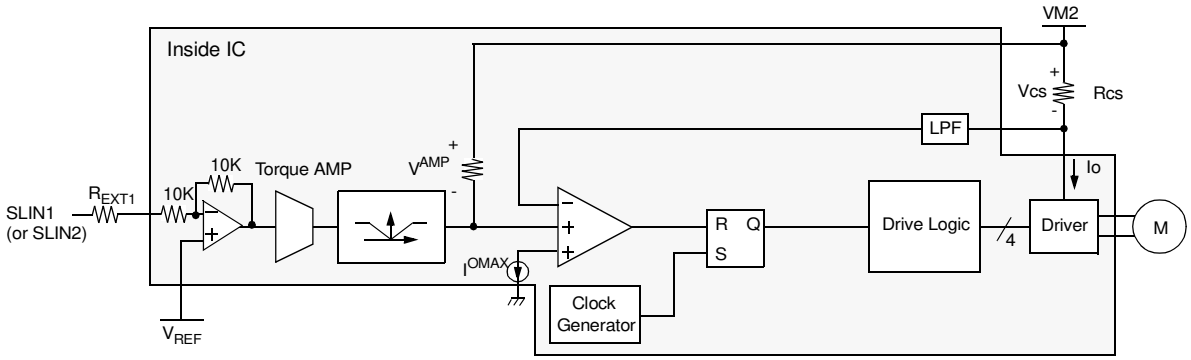
Limit current	Input/Output gain[A/V]	Remark
$\frac{0.5}{Rcs}$	$\frac{10K}{R_{EXT1}+10K} \bullet \frac{G_{VO}}{R_{CS}}$	$\frac{10K}{R_{EXT1}+10K}$ is gain scaler

7) Spindle block adopts 180° commutation methodology which is fully compatible with a conventional BLDC spindle motor. Users don't need to change or modify their spindle motor.
8) The range of the input voltage is as shown below when Rcs=0.33Ω, R_{EXT1}=0.



		Rotation
MUTE2 =H	SPIN > V_{REF}	Forward rotation
	SPIN < V_{REF}	Reverse brake
MUTE2 =L,open	-	Short brake
		Short brake

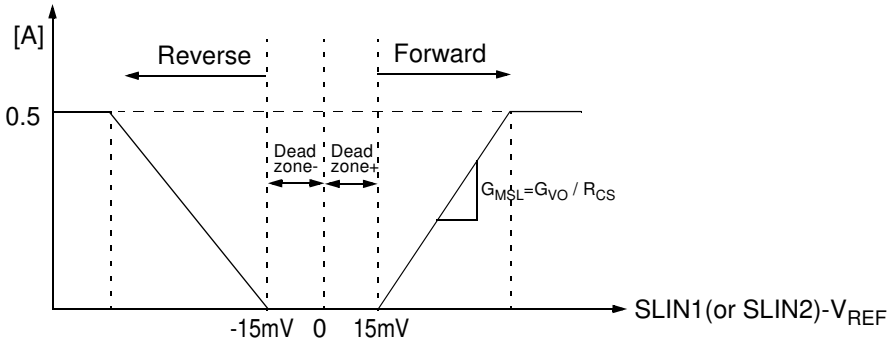
2. Torque Control & Output Current Control Of Sled Motor(2-phase Step Motor)



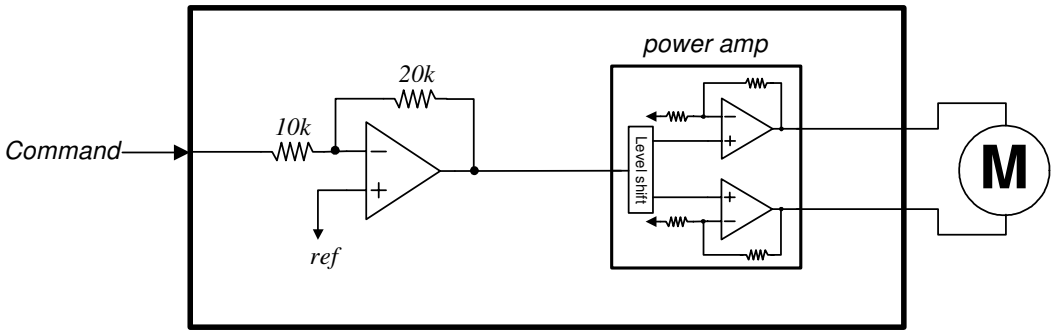
1) By amplifying the voltage difference between V_{REF} and SLIN1(or SLIN2) from Servo IC(or DSP), the Torque AMP produces the input voltage(V_{AMP}) which means input current command.
2) The output current (I_O) is converted into the voltage (V_{CS}) through the sense resistor (R_{CS}) and compared with the V_{AMP}.
3) The clock generator always make the RS latch become set periodically, this enables the output driver's on state, when the V_{CS} and the V_{AMP} are equal the state becomes off.
4) By the negative feedback loop, the sensed output voltage V_{CS} equals to the V_{AMP}.
5) To avoid output upper and lower transistor's short through, a switch trick is needed. Turn on delay time is 1usec, so the phase delay time,when changing the current direction, is 1usec.
6) The gain and limit currents are calculated as shown in the table below.($Gvo=V_{AMP}/[SLIN1(or\ SLIN2)-V_{REF}]=1[V/V]$

Torque limit current	Input/Output gain[A/V]	Remark
$\frac{0.5}{Rcs}$	$\frac{10K}{R_{EXT1}+10K} \bullet \frac{G_{VO}}{R_{CS}}$	$\frac{10K}{R_{EXT1}+10K}$ is gain scaler

7) The range of the torque voltage is as shown below when Rcs=1W, R_{EXT1}=0.



3. Channel 1~4 Schematic



- The reference voltage(ref) is given externally through pin21.
- The input OP-amp output signal is amplified by (20K/10K) times and then fed to the power amplifier. The gain of power amplifier is 4 so the total max gain of channels 1 through 4 is 8.

4. Mute Inputs

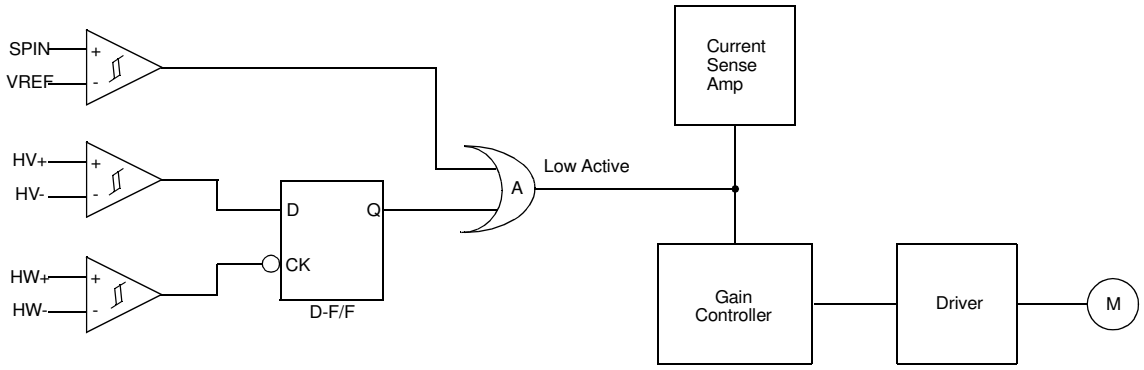
FAN8741 has 2 independent mute pins: Pin #22(MUTE1) and Pin #23(MUTE2). Details are shown below.

MUTE1	MUTE2	SPIN-DLE	SLED	CH1/2/3	CH4(typ. load-ing driver)	SPINDLE brake type
H	H	Enable			Disable	Reverse brake when SPIN<VREF
H	L	Enable			Disable	Short brake SPIN ≠ VREF(note)
L	H	Disable	Enable	Disable	Enable	-
L	L	Disable				-

Note:

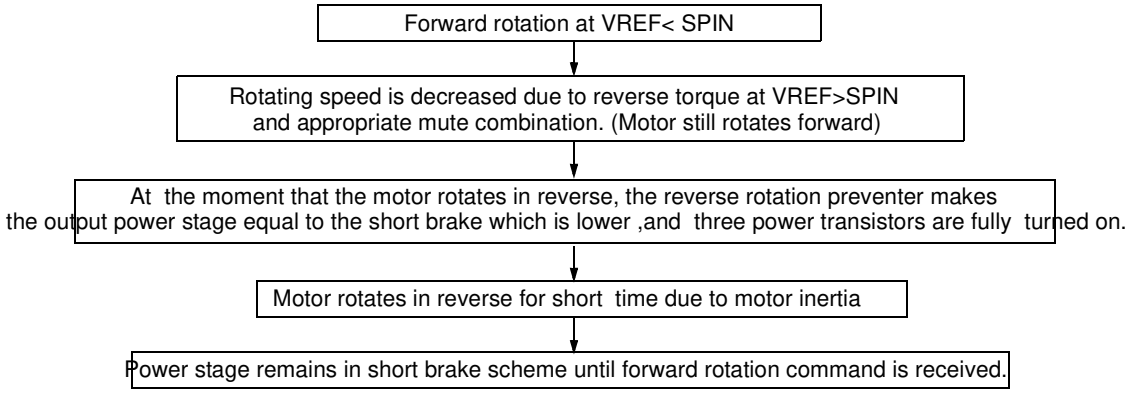
To make the spindle short brake, MUTE2 goes low and the spindle command must not be in deadzone(±50mV). When the spindle command is within the deadzone, the spindle block enters disable mode even though MUTE2 is low.

5. Reverse Rotation Prevention(Spindle)

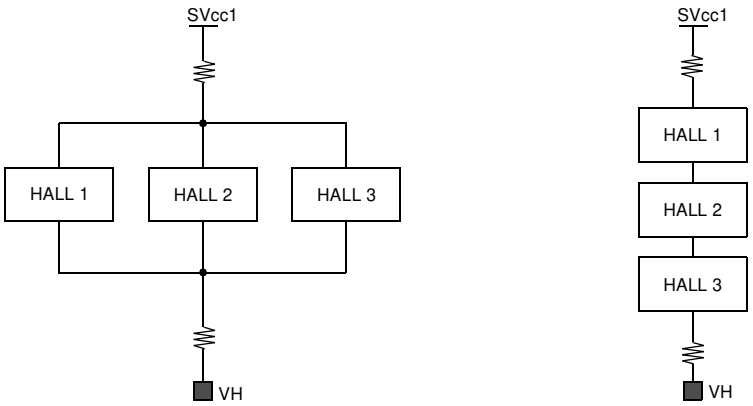


1) As in the state of the forward rotation, the D-F/F output, Q is HIGH and the motor rotates normally. At this state, if the control input is changed such that VREF>SPIN, then the motor rotates slowly by the reverse commutation in the driver. When the motor begins to rotate in the reverse direction, the D-F/F output becomes Low and the OR Gate output becomes Low. This prevents the motor from continuing to rotate in the reverse direction. This operation principle is shown in the following table and flow chart.

Rotation	HV	HW	D-F/F (Q)	Reverse Rotation Preventer	
				V_{REF}<SPIN	V_{REF}>SPIN
Forward	H	H→L	H	Forward	-
Reverse	L	H→L	L	-	Brake and Stop



6. Hall Sensor Connection



7. PWM frequency

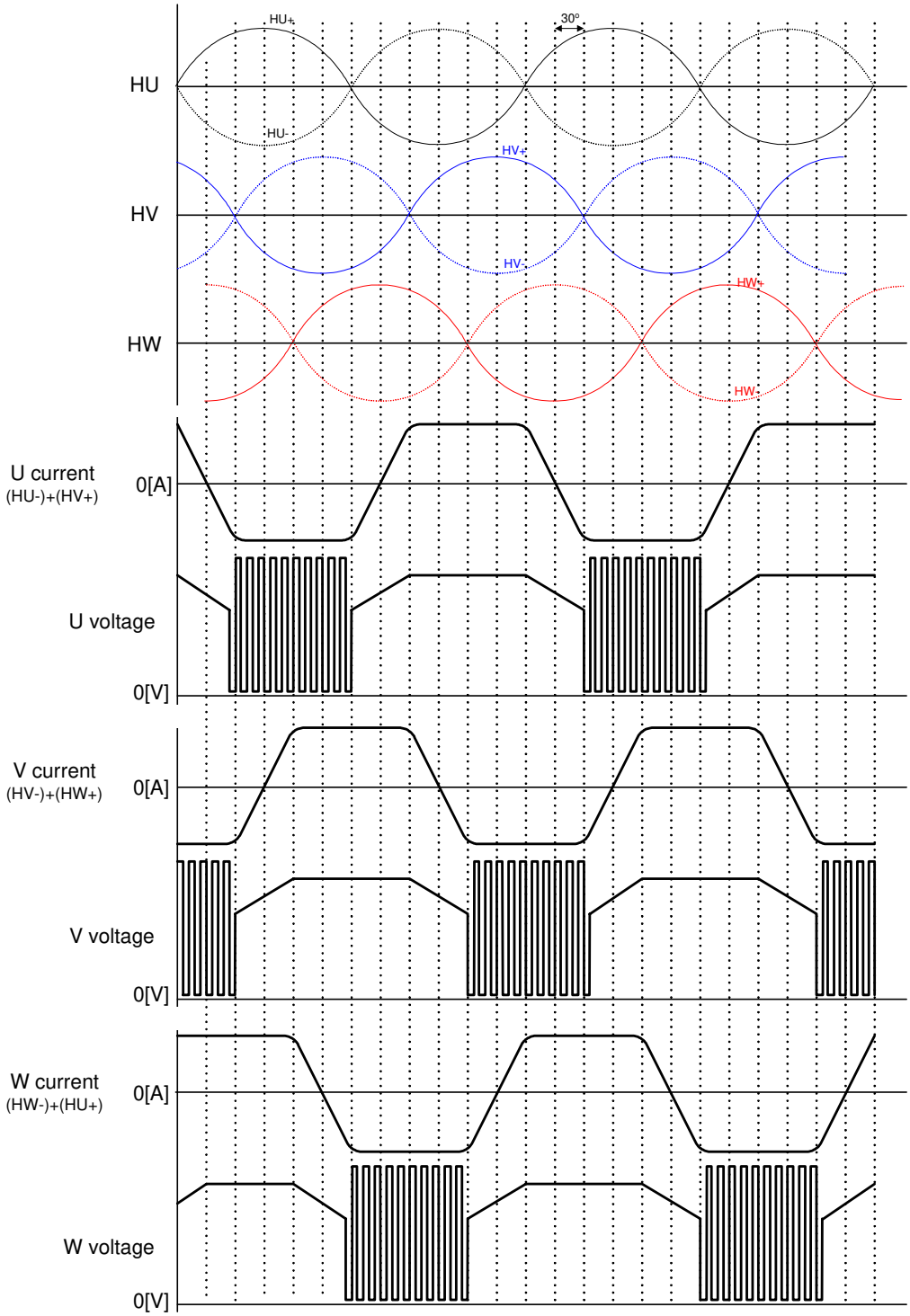
The PWM operation of the spindle and sled channels are controlled by an internal clock generator with a typical frequency of 100KHz.

8. ETC

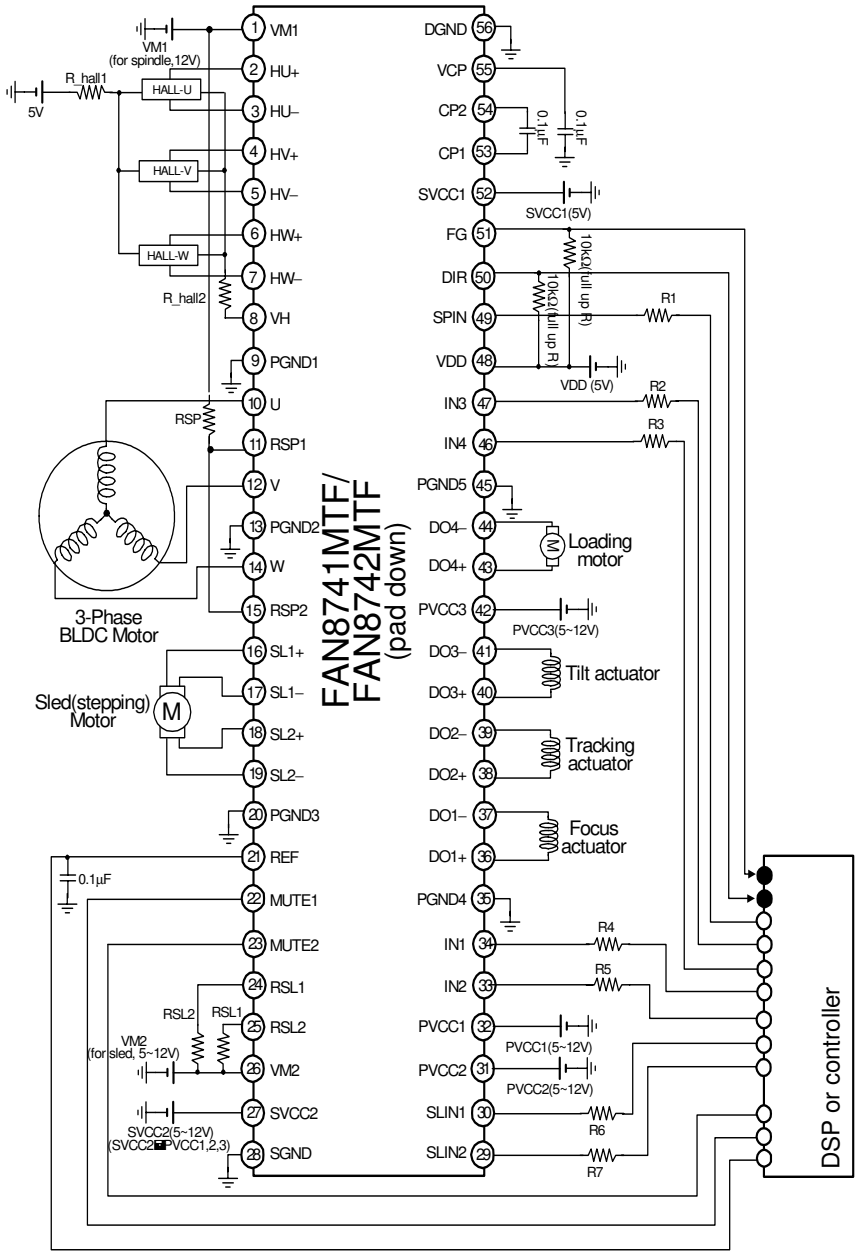
1) FG and DIR output s are open-collector types.

2) By-pass capacitors are recommended at hall sensor and power supply inputs.

9. Spindle Part Input-output Timing Chart

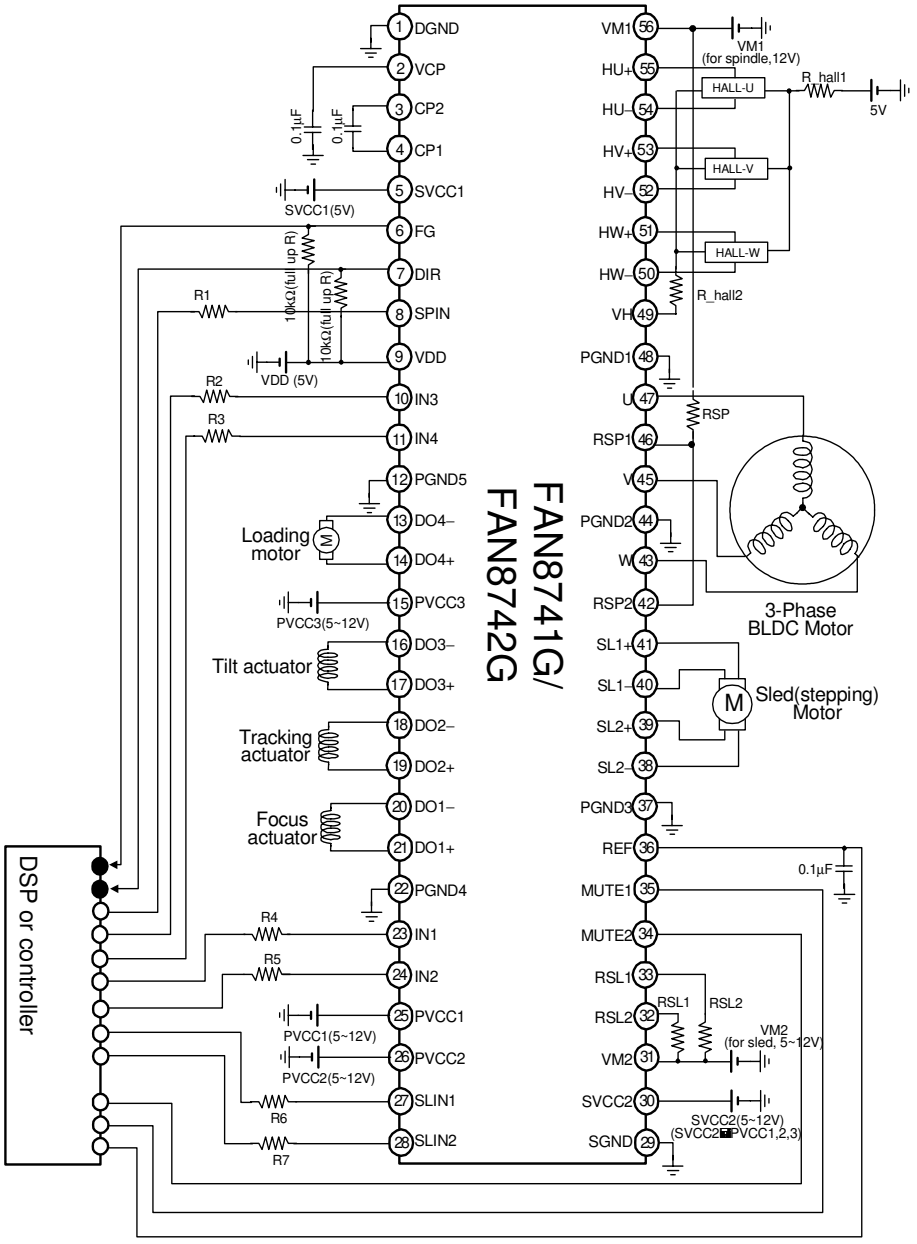


Typical Application Circuits(FAN8741MTF example)



Component	Reference value	Remark
R1~R7	10kΩ	Gain scaling resistors. Please refer to pages 12,13, and 14.
R_hall1,R_hall2	100Ω	Hall bias resistors
RSL1,RSL2	1Ω	Rcs at sled driver. (I_limit=0.5A,Gain=0.5A/V@R6,R7 are 10kΩ)
RSP	0.33Ω	Rcs at spindle driver. (I_limit=1.5A,Gain=1.5A/V@R1 is 10kΩ)
Bypass electrolytic capacitors(47~100μF) are recommended at power supply inputs.		

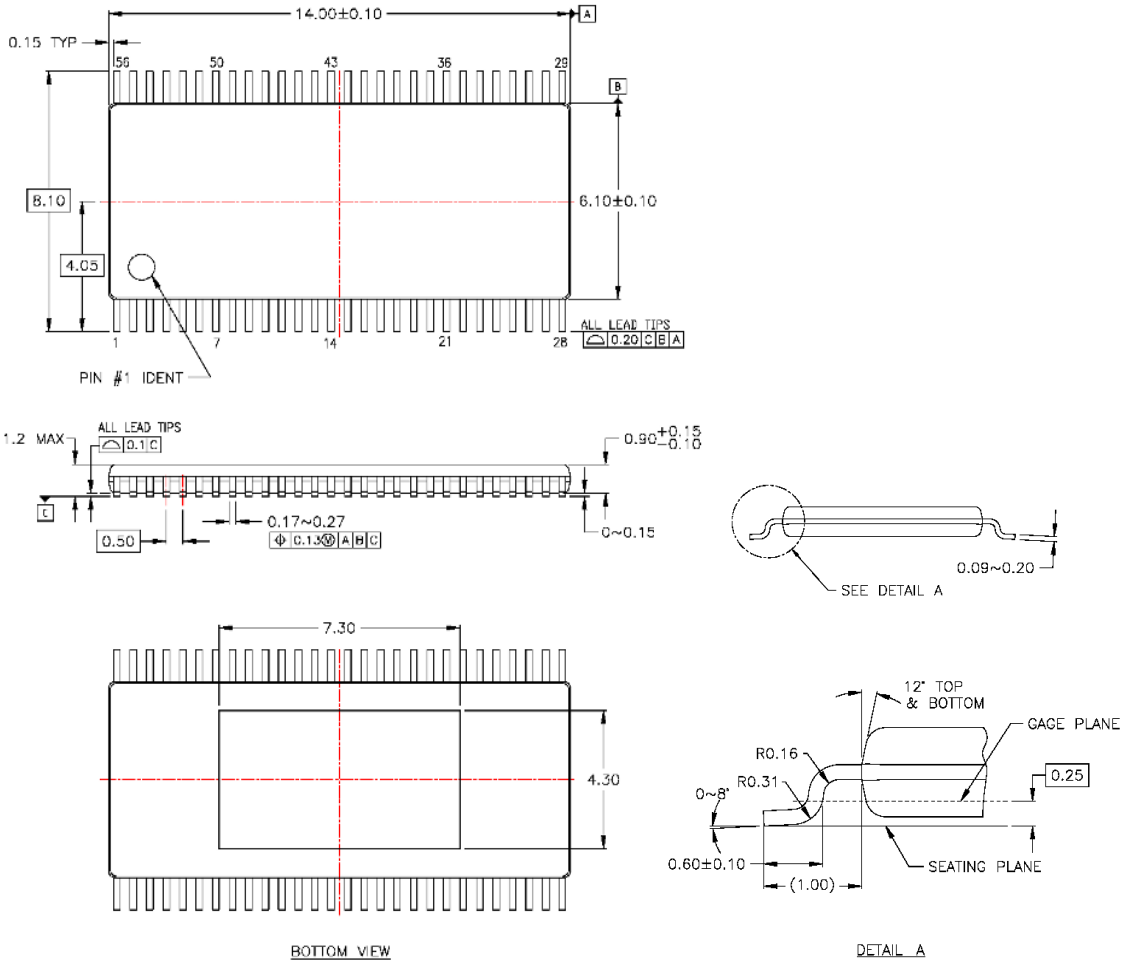
Typical Application Circuits(FAN8741G example)



Component	Reference value	Remark
R1~R7	10kΩ	Gain scaling resistors. Please refer to 12,13,14 pages.
R_hall1,R_hall2	100Ω	Hall bias resistors
RSL1,RSL2	1Ω	Rcs at sled driver. (I_limit=0.5A,Gain=0.5A/V@R6,R7 are 10kΩ)
RSP	0.33Ω	Rcs at spindle driver. (I_limit=1.5A,Gain=1.5A/V@R1 is 10kΩ)
Bypass electrolytic capacitors(47~100µF) are recommended at power supply inputs.		

Package Dimensions of 56-TSSOP-EP(lead frame is exposed to the bottom)

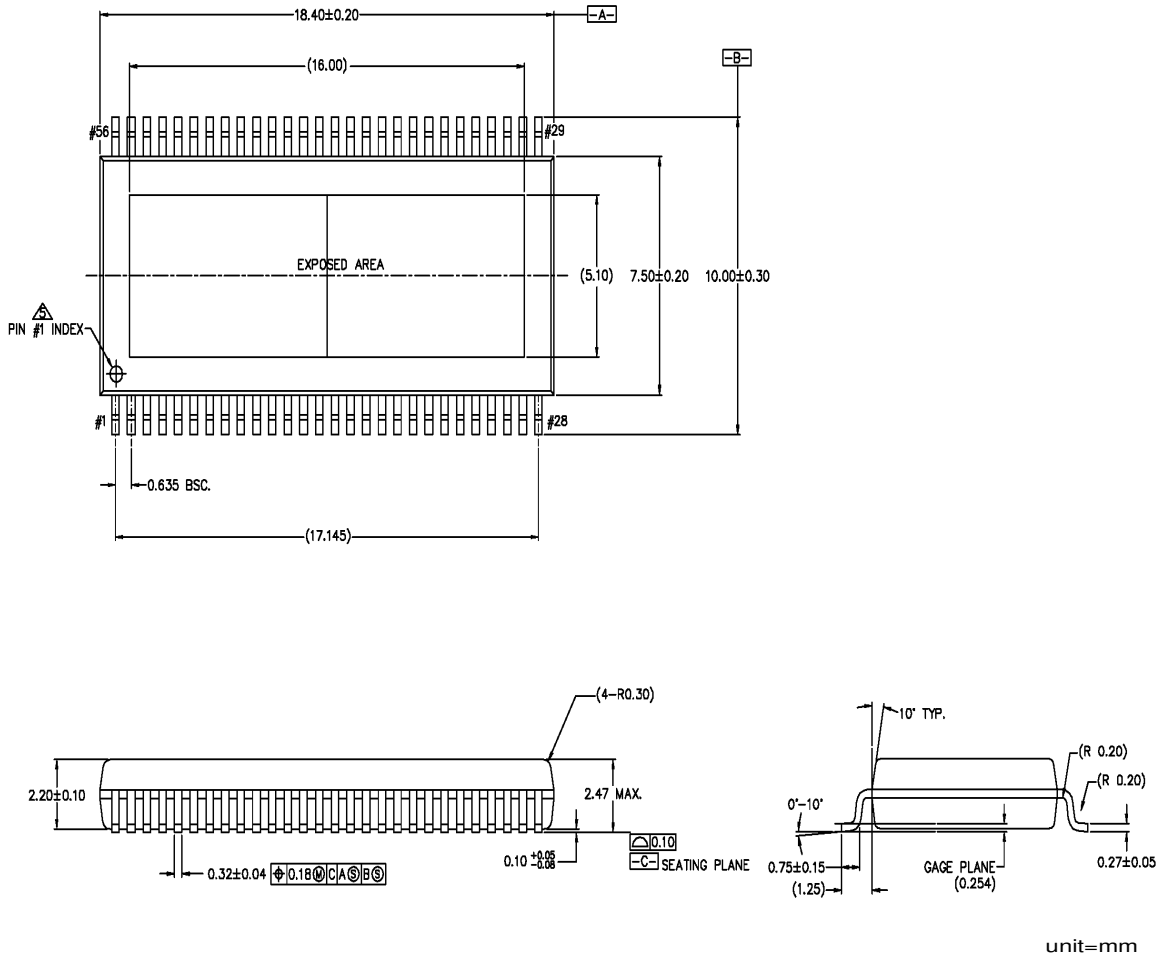
56-TSSOP-EP



unit=mm

Package Dimensions of 56-SSOP-HS(lead frame is exposed to the top)

56-SSOP-HS



unit=mm

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