EVMK2E
Technical Reference Manual
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Keystone 2 EVM Technical Reference Manual

Preface

About this Document

This document is a Technical Reference Manual for the Keystone 2 Evaluation Module (EVMK2E) designed and developed by eInfochips Limited for Texas Instruments, Inc.

Notational Conventions

This document uses the following conventions:

Program listings, program examples, and interactive displays are shown in a mono-spaced font. Examples use **bold** for emphasis, and interactive displays use bold to distinguish commands that you enter from items that the system displays (such as prompts, command output, error messages, etc.).

Square brackets ([and]) identify an optional parameter. If you use an optional parameter, you specify the information within the brackets. Unless the square brackets are in a bold typeface, do not enter the brackets themselves.

Underlined, italicized non-bold text in a command is used to mark place holder text that should be replaced by the appropriate value for the user's configuration.

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Document Revision History

Release	Chapter	Description of Change
1.0	All	Initial Draft
2.0	Table 4-1	Updated Table 4-1(VCC1V8 and VCC0V85V power rating)
2.1	Additional Terms	REACH compliance note added on page 4.

Acronyms

Acronym	Description
AMC or AdvancedMC	Advanced Mezzanine Card
BMC	Board management controller
CCS	Code Composer Studio
DDR3	Double Data Rate 3 Interface
DIP	Dual-In-Line Package
DSP	Digital Signal Processor
DTE	Data Terminal Equipment
EEPROM	Electrically Erasable Programmable Read Only Memory
EMAC	Ethernet Media Access Controller
EMIF	External Memory Interface
EVM	Evaluation Module
I2C	Inter Integrated Circuit
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
JTAG	Joint Test Action Group
LED	Light Emitting Diode
MCH	MicroTCA Carrier Hub
MTCA or MicroTCA	Micro Telecommunication Computing Architecture
MMC	Module Management Controller
PCIe	PCI Express
PICMG®	PCI Industrial Computer Manufacturers Group
RFU	Reserved for Future Use
SATA	Serial Advanced Technology Attachment
SDRAM	Synchronous Dynamic Random Access Memory
SERDES	Serializer-Deserializer
SGMII	Serial Gigabit Media Independent Interface
SODIMM	small outline dual in-line memory module
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
XFI	10 Gigabit Ethernet
XDS200	Texas Instruments' System Trace Emulator

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1. Overview

This chapter provides an overview of the EVMK2E along with the key features and block diagram.

- Key Features
- Functional Overview
- Basic Operation
- Configuration Switch Settings
- Power Supply

1.1 Key Features

The EVMK2E is a high performance, cost-efficient, standalone development platform that enables users to evaluate and develop applications for the Keystone 2 Texas Instruments System-on-Chip (SoC).The EVM's form-factor is equivalent to a double-wide PICMG® AMC.0 R2.0 AdvancedMC module.

EVM comes with an On Board, high speed, system trace capable XDS200 Emulator.

Schematics, code examples and application notes are available, to ease the hardware development process and to reduce the time to market.

The key features of the EVM are:

- Texas Instruments' fixed point DSP – 66AK2E05
- 4096 Mbytes of DDR3-1600 ECC Unbuffred SO-DIMM
- 512 Mbytes of NAND Flash
- 16 Mbytes of NOR Flash
- Eight Gigabit Ethernet ports supporting 10/100/1000 Mbps data-rate – two on AMC connector, two RJ-45 Connector and four ports on uRTM connector (Zone-3)
- 170 pin B+ style AMC Interface containing, PCIe, SATA, Gigabit Ethernet, TSIP
- TWO 160 pin ZD+ style uRTM Interface containing HyperLink, SGMII ,XFI
- 128 Kbytes I2C EEPROM for Boot support from I2C
- 4 User LEDs, 1 Banks of DIP Switches and 3 Software-controlled LEDs
- Two RS232 Serial interface on 4-Pin header or UART over mini-USB connector
- EMIF, Timer, I2C, SPI, UART on 120-pin expansion header
- Two USB3.0 ports, Port-0 supports Host mode and Port-1 supports Host or Device mode (Operating at 5 Gbps data-rate)
- One LCD display for debugging states
- RoHS Compliant Design
- MIPI 60-Pin JTAG header to support all types of external emulator
- On Board XDS200 Emulator
- Board management controller (BMC) for Intelligent Platform Management Interface (IPMI) will available in future revision.
- Powered by DC power-brick adaptor (12V/5A) or AMC Carrier back-plane
- Double wide PICMG ® AdvancedMC (AMC) form factor (7.11" x 5.84")

1.2 Functional Overview

The EVM contains 66AK2Ex platform, based on TI's industry leading KeyStone II architecture, combines up to four ARM® Cortex™-A15 MPCore™ processors with TI's TMS320C66x high performance DSP. The 66AK2Ex platform provides up to 5.6 GHz of ARM and 1.25 GHz of DSP processing coupled with security and packet processing and Ethernet switching, all at lower power than multichip solutions making it optimal for embedded systems. For applications like enterprise video, digital video recording, video analytics, industrial imaging, industrial control and enterprise voice gateways, the 66AK2Ex platform combines ARM's best-in-class single-thread performance for control processing with the compute performance of the C66x DSP. Using TI's heterogeneous programming runtime software and tools, customers can easily develop differentiated products with 66AK2Ex SoCs.
The functional block diagram of EVMK2E is shown in below

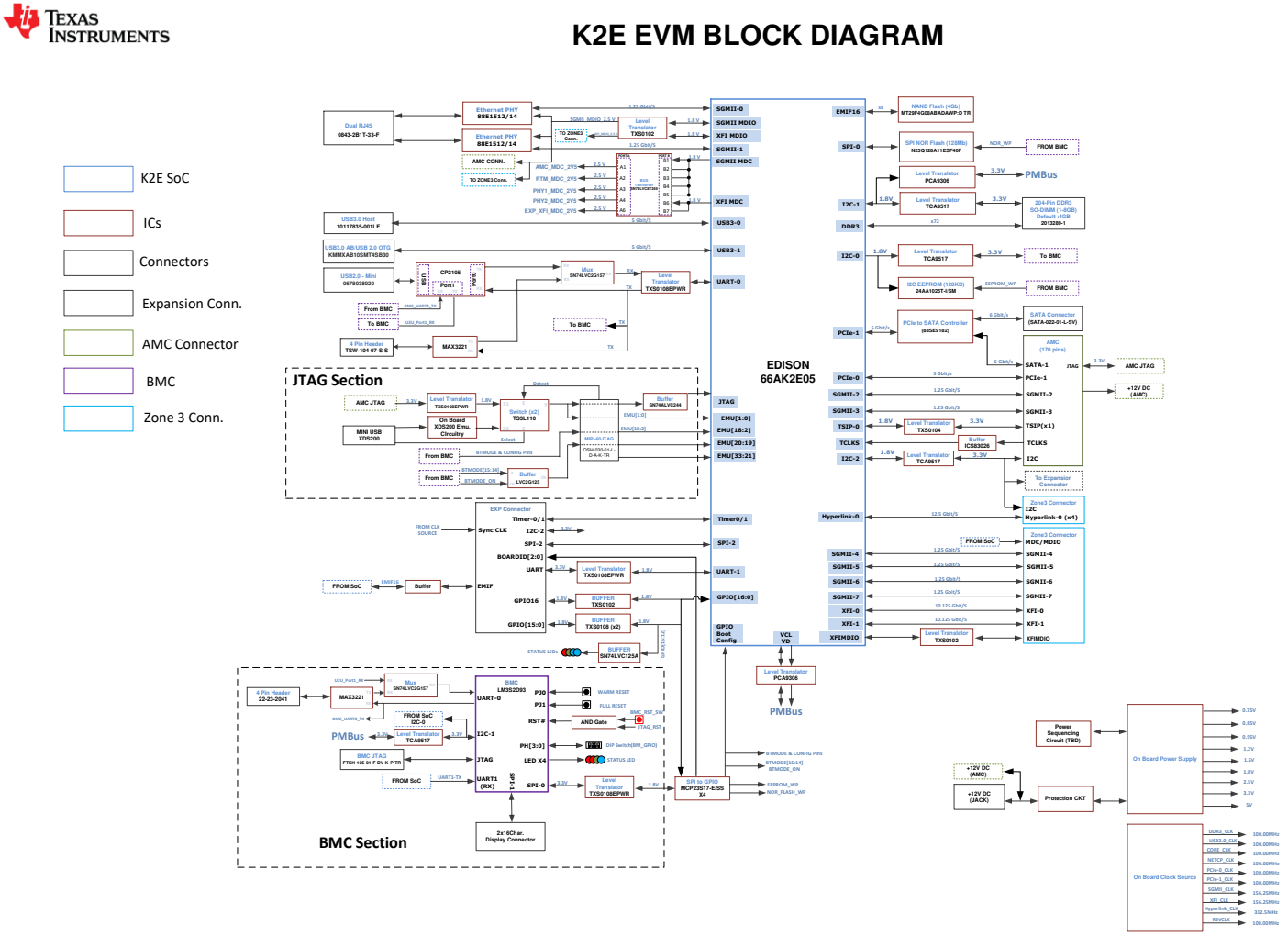

Figure 1.1: Block Diagram of EVMK2E

1.3 Basic Operation

The EVMK2E platform is designed to work with TI's Code Composer Studio (CCS) development environment and ships with a version specifically tailored for this board. CCS can interface with the board via on-board XDS200 emulation circuitry using the USB cable supplied along with this EVM or through an external emulator. We recommend using CCS rev 5.3 later versions.

The EVMK2E comes with the Texas Instruments Multicore Software Development Kit (MCSDK) for SYS/BIOS OS. The BIOS MCSDK provides the core foundational building blocks that facilitate application software development on TI's high performance and multicore DSPs. The MCSDK also includes an out-of-box demonstration; see the "MCSDK Getting Started Guide".

To start operating the board, follow instructions in the Quick Start Guide. This guide provides instruction for proper connections and configuration for running the POST and OOB Demos. After completing the POST and OOB Demos, proceed with installing CCS and the EVM support files by following the instructions on the USB flash drive. This process will install all the necessary development tools, drivers and documentation..

After the installation is completed, follow below steps to run Code Composer Studio.

1. Power ON the board using power brick adaptor (12V/5A) supplied along with this EVM or Insert this EVM board into MicroTCA chassis or AMC carrier back-plane.
2. Connect USB cable from host PC to EVM board.
3. Launch Code Composer Studio from host PC by double clicking on its icon at PC desktop.

Detailed information about the EVM including examples and reference material is available in the USB flash drive available with this EVM kit.

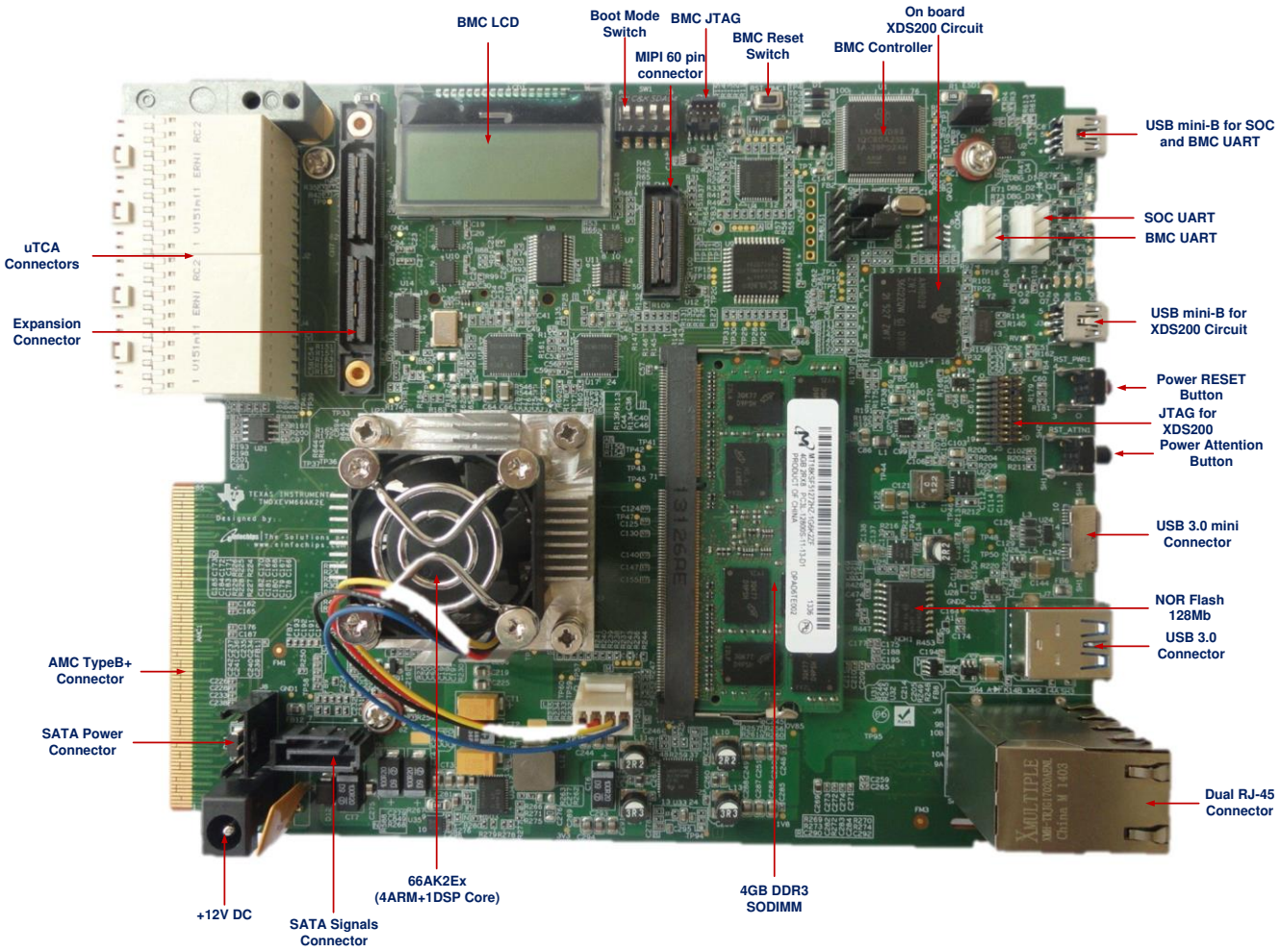

Figure 1.2: EVMK2E top side

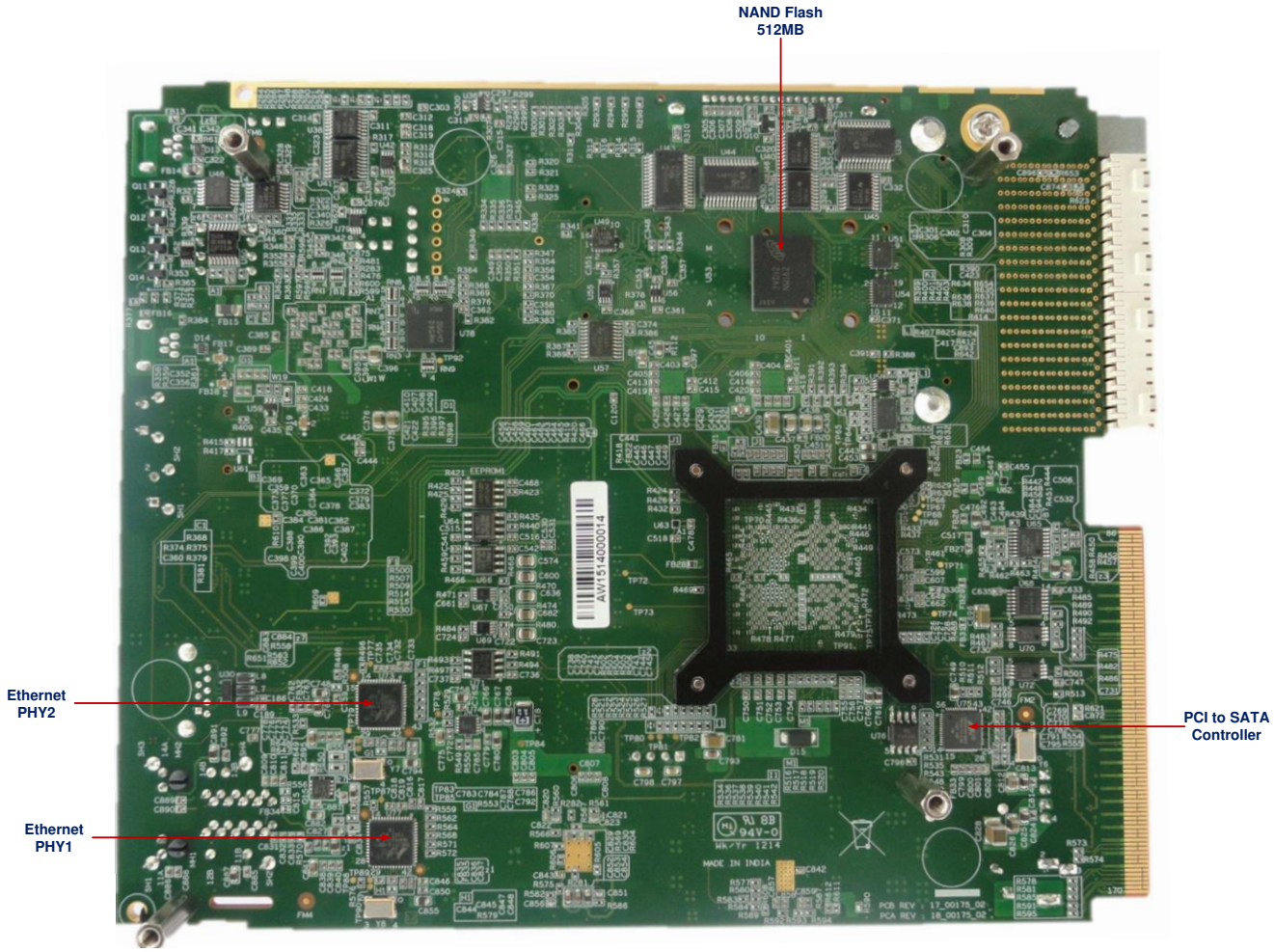

Figure 1.3: EVMK2E bottom side

1.4 Power Supply

The EVMK2E can be powered from a single +12V / 5.0A DC (60W) external power supply connected to the DC power jack (J11). Internally, +12V input is converted into required voltage levels using local DC-DC converters.

- CVDD (+0.75V~+1.00V) used for the Smart-Reflex enabled DSP and ARM Core logic
- CVDD1 (+0.95V) is used for ARM Array SRAM
- +1.5V is used for DDR3 buffers of SoC, and DDR3 SODIMM module
- +0.75V is used for DDR3 SODIMM module termination
- +1.8V is used for SoC peripheral (GPIO, JTAG, TIMER, SPI, TSIP, RESETs, NMI, Smart Reflex, Hyperlink, MDIO, UART) I/O supply and other buffer I/O supply
- +2.5V is used for Gigabit Ethernet PHY(88SE1512/14) core
- +3.3V is used for USB Digital and Analog of SoC
- +0.85V is used for SERDES Low Analog and USB Analog of SoC
- +5V is used for external USB3.0 ports
- The DC power jack connector is a 2.5mm barrel-type plug with center-tip as positive polarity

The EVMK2E can also draw power from the AMC edge connector (AMC1). If the board is inserted into a PICMG® AMC.0 R2.0 compliant system chassis or AMC Carrier backplane, an external +12V supply from DC jack (J11) is not required.

Note:
External Power Supply Requirements:
Nom Voltage: 12 VDC
Max Current: 5000 mA
Efficiency Level V

External Power Supply Regulatory Compliance Certifications: Recommend selection and use of an external a power supply which meets TI's required minimum electrical ratings in addition to complying with applicable regional product regulatory/safety certification requirements such as (by example) UL, CSA, VDE, CCC, PSE, etc.

2. Introduction to the EVMK2E board

This chapter provides an introduction and details of interfaces for the EVMK2E board. It contains:

- Memory Map
- EVM Boot mode and Boot configuration switch settings
- Board Revision ID
- JTAG - Emulation Overview
- Clock Domains
- I2C boot EEPROM / SPI NOR Flash
- BMC (Board management controller)
- Gigabit Ethernet PHY
- DDR3 External Memory Interface (SODIMM Module)
- 16-bit Asynchronous External Memory Interface
- HyperLink Interface
- PCIe Interface
- UART Interface
- XFI (10-GbE)
- Expansion Header
- Universal Serial Bus 2.0/3.0(USB2.0/3.0)
- EVM I2C Routing diagram

2.1 Memory Map

The memory map of the 66AK2E05 device is as shown in Table 2.1.

Table 2.1: 66AK2E05 Memory Map

Physical 40 bit Address					
Start	End	Bytes	ARM View	DSP View	SOC View
00 0000 0000	00 0003 FFFF	256K	ARM ROM	Reserved	ARM ROM
00 0004 0000	00 007F FFFF	8M-256K	Reserved	Reserved	Reserved
00 0080 0000	00 0087 FFFF	512K	Reserved	L2 SRAM	L2 SRAM
00 0088 0000	00 008F FFFF	512K	Reserved	Reserved	Reserved
00 0090 0000	00 00DF FFFF	5M	Reserved	Reserved	Reserved
00 00E0 0000	00 00E0 7FFF	32K	Reserved	L1P SRAM	L1P SRAM
00 00E0 8000	00 00EF FFFF	1M-32K	Reserved	Reserved	Reserved
00 00F0 0000	00 00F0 7FFF	32K	Reserved	L1D SRAM	L1D SRAM
00 00F0 8000	00 00FF FFFF	1M-32K	Reserved	Reserved	Reserved
00 0100 0000	00 0100 FFFF	64K	ARM AXI2VBUSM registers	C66x CorePac registers	C66x CorePac registers
00 0101 0000	00 010F FFFF	1M-64K	Reserved	C66x CorePac registers	C66x CorePac registers
00 0110 0000	00 0110 FFFF	64K	ARM STM Stimulus Ports	C66x CorePac registers	C66x CorePac registers
00 0101 0000	00 01BF FFFF	11M-64K	Reserved	C66x CorePac registers	C66x CorePac registers
00 01C0 0000	00 01CF FFFF	1M	Reserved	Reserved	Reserved
00 01D0 0000	00 01D0 007F	128	Tracer CFG0	Tracer CFG0	Tracer CFG0
00 01D0 0080	00 01D0 7FFF	32K-128	Reserved	Reserved	Reserved
00 01D0 8000	00 01D0 807F	128	Tracer CFG1	Tracer CFG1	Tracer CFG1
00 01D0 8080	00 01D0 FFFF	32K-128	Reserved	Reserved	Reserved
00 01D1 0000	00 01D1 007F	128	Tracer CFG2	Tracer CFG2	Tracer CFG2
00 01D1 0080	00 01D1 7FFF	32K-128	Reserved	Reserved	Reserved
00 01D1 8000	00 01D1 807F	128	Tracer CFG3	Tracer CFG3	Tracer CFG3
00 01D1 8080	00 01D1 FFFF	32K-128	Reserved	Reserved	Reserved
00 01D2 0000	00 01D2 007F	128	Tracer CFG4	Tracer CFG4	Tracer CFG4
00 01D2 0080	00 01D2 7FFF	32K-128	Reserved	Reserved	Reserved
00 01D2 8000	00 01D2 807F	128	Tracer CFG5	Tracer CFG5	Tracer CFG5
00 01D2 8080	00 01D2 FFFF	32K-128	Reserved	Reserved	Reserved
00 01D3 0000	00 01D3 007F	128	Tracer CFG6	Tracer CFG6	Tracer CFG6
00 01D3 0080	00 01D3 7FFF	32K-128	Reserved	Reserved	Reserved
00 01D3 8000	00 01D3 807F	128	Tracer CFG7	Tracer CFG7	Tracer CFG7
00 01D3 8080	00 01D3 FFFF	32K-128	Reserved	Reserved	Reserved
00 01D4 0000	00 01D4 007F	128	Tracer CFG8	Tracer CFG8	Tracer CFG8
00 01D4 0080	00 01D4 7FFF	32K-128	Reserved	Reserved	Reserved
00 01D4 8000	00 01D4 807F	128	Tracer CFG9	Tracer CFG9	Tracer CFG9
00 01D4 8080	00 01D4 FFFF	32K-128	Reserved	Reserved	Reserved
00 01D5 0000	00 01D5 007F	128	Reserved	Reserved	Reserved
00 01D5 0080	00 01D5 7FFF	32K-128	Reserved	Reserved	Reserved
00 01D5 8000	00 01D5 807F	128	Reserved	Reserved	Reserved
00 01D5 8080	00 01D5 FFFF	32K-128	Reserved	Reserved	Reserved

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 01D6 0000	00 01D6 007F	128	Reserved	Reserved	Reserved
00 01D6 0080	00 01D6 7FFF	32K-128	Reserved	Reserved	Reserved
00 01D6 8000	00 01D6 807F	128	Reserved	Reserved	Reserved
00 01D6 8080	00 01D6 FFFF	32K-128	Reserved	Reserved	Reserved
00 01D7 0000	00 01D7 007F	128	Reserved	Reserved	Reserved
00 01D7 0080	00 01D7 7FFF	32K-128	Reserved	Reserved	Reserved
00 01D7 8000	00 01D7 807F	128	Reserved	Reserved	Reserved
00 01D7 8080	00 01D7 FFFF	32K-128	Reserved	Reserved	Reserved
00 01D8 0000	00 01D8 007F	128	Reserved	Reserved	Reserved
00 01D8 0080	00 01D8 7FFF	32K-128	Reserved	Reserved	Reserved
00 01D8 8000	00 01D8 807F	128	Reserved	Reserved	Reserved
00 01D8 8080	00 01D8 8FFF	32K-128	Reserved	Reserved	Reserved
00 01D9 0000	00 01D9 007F	128	Reserved	Reserved	Reserved
00 01D9 0080	00 01D9 7FFF	32K-128	Reserved	Reserved	Reserved
00 01D9 8000	00 01D9 807F	128	Reserved	Reserved	Reserved
00 01D9 8080	00 01D9 FFFF	32K-128	Reserved	Reserved	Reserved
00 01DA 0000	00 01DA 007F	128	Tracer CFG20	Tracer CFG20	Tracer CFG20
00 01DA 0080	00 01DA 7FFF	32K-128	Reserved	Reserved	Reserved
00 01DA 8000	00 01DA 807F	128	Reserved	Reserved	Reserved
00 01DA 8080	00 01DA FFFF	32K-128	Reserved	Reserved	Reserved
00 01DB 0000	00 01DB 007F	128	Tracer CFG22	Tracer CFG22	Tracer CFG22
00 01DB 0080	00 01DB 7FFF	32K-128	Reserved	Reserved	Reserved
00 01DB 8000	00 01DB 807F	128	Reserved	Reserved	Reserved
00 01DB 8080	00 01DB 8FFF	32K-128	Reserved	Reserved	Reserved
00 01DC 0000	00 01DC 007F	128	Tracer CFG24	Tracer CFG24	Tracer CFG24
00 01DC 0080	00 01DC 7FFF	32K-128	Reserved	Reserved	Reserved
00 01DC 8000	00 01DC 807F	128	Tracer CFG25	Tracer CFG25	Tracer CFG25
00 01DC 8080	00 01DC FFFF	32K-128	Reserved	Reserved	Reserved
00 01DD 0000	00 01DD 007F	128	Tracer CFG26	Tracer CFG26	Tracer CFG26
00 01DD 0080	00 01DD 7FFF	32K-128	Reserved	Reserved	Reserved
00 01DD 8000	00 01DD 807F	128	Tracer CFG27	Tracer CFG27	Tracer CFG27
00 01DD 8080	00 01DD FFFF	32K-128	Reserved	Reserved	Reserved
00 01DE 0000	00 01DE 007F	128	Tracer CFG28	Tracer CFG28	Tracer CFG28
00 01DE 0080	00 01DE 03FF	1K-128	Reserved	Reserved	Reserved
00 01DE 0400	00 01DE 047F	128	Tracer CFG29	Tracer CFG29	Tracer CFG29
00 01DD 0480	00 01DD 07FF	1K-128	Reserved	Reserved	Reserved
00 01DE 0800	00 01DE 087F	128	Tracer CFG30	Tracer CFG30	Tracer CFG30
00 01DE 0880	00 01DE 7FFF	30K-128	Reserved	Reserved	Reserved
00 01DE 8000	00 01DE 807F	128	Tracer CFG31	Tracer CFG31	Tracer CFG31
00 01DE 8080	00 01DF FFFF	64K-128	Reserved	Reserved	Reserved
00 01E0 0000	00 01E3 FFFF	256K	Reserved	Reserved	Reserved
00 01E4 0000	00 01E7FFFF	256k	TSIP_CFG	TSIP_CFG	TSIP_CFG
00 01E8 0000	00 01E8 3FFF	16K	ARM CorePac_CFG	ARM CorePac_CFG	ARM CorePac_CFG

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 01E8 4000	00 01EB FFFF	240k	Reserved	Reserved	Reserved
00 01EC 0000	00 01EF FFFF	256K	Reserved	Reserved	Reserved
00 01F0 0000	00 01F7 FFFF	512K	Reserved	Reserved	Reserved
00 01F8 0000	00 01F8 FFFF	64K	Reserved	Reserved	Reserved
00 01F9 0000	00 01F9 FFFF	64K	Reserved	Reserved	Reserved
00 01FA 0000	00 01FB FFFF	128K	Reserved	Reserved	Reserved
00 01FC 0000	00 01FD FFFF	128K	Reserved	Reserved	Reserved
00 01FE 0000	00 01FF FFFF	128K	Reserved	Reserved	Reserved
00 0200 0000	00 020F FFFF	1M	Network Coprocessor 0(Packet Accelerator, 1-gigabit Ethernet switch subsystem and Security Accelerator)	Network Coprocessor 0(Packet Accelerator, 1-gigabit Ethernet switch subsystem and Security Accelerator)	Network Coprocessor 0(Packet Accelerator, 1-gigabit Ethernet switch subsystem and Security Accelerator)
00 0210 0000	00 0210 FFFF	64K	Reserved	Reserved	Reserved
00 0211 0000	00 0211 FFFF	64K	Reserved	Reserved	Reserved
00 0212 0000	00 0213 FFFF	128K	Reserved	Reserved	Reserved
00 0214 0000	00 0215 FFFF	128K	Reserved	Reserved	Reserved
00 0216 0000	00 0217 FFFF	128K	Reserved	Reserved	Reserved
00 0218 0000	00 0218 7FFF	32k	Reserved	Reserved	Reserved
00 0218 8000	00 0218 FFFF	32k	Reserved	Reserved	Reserved
00 0219 0000	00 0219 FFFF	64k	Reserved	Reserved	Reserved
00 021A 0000	00 021A FFFF	64K	Reserved	Reserved	Reserved
00 021B 0000	00 021B FFFF	64K	Reserved	Reserved	Reserved
00 021C 0000	00 021C 03FF	1K	Reserved	Reserved	Reserved
00 021C 0400	00 021C 3FFF	15K	Reserved	Reserved	Reserved
00 021C 4000	00 021C 43FF	1K	Reserved	Reserved	Reserved
00 021C 4400	00 021C 5FFF	7K	Reserved	Reserved	Reserved
00 021C 6000	00 021C 63FF	1K	Reserved	Reserved	Reserved
00 021C 6400	00 021C 7FFF	7K	Reserved	Reserved	Reserved
00 021C 8000	00 021C 83FF	1K	Reserved	Reserved	Reserved
00 021C 8400	00 021C FFFF	31K	Reserved	Reserved	Reserved
00 021D 0000	00 021D 03FF	1K	Memory protection unit (MPU) 15	Memory protection unit (MPU) 15	Memory protection unit (MPU) 15
00 021D 0400	00 021D 047F	128	Tracer CFG32	Tracer CFG32	Tracer CFG32
00 021D 0100	00 021D 3FFF	15K-128	Reserved	Reserved	Reserved
00 021D 4000	00 021D 40FF	256	Reserved	Reserved	Reserved
00 021D 4100	00 021D 7FFF	16K-256	Reserved	Reserved	Reserved
00 021D 8000	00 021D 80FF	256	Reserved	Reserved	Reserved
00 021D 8100	00 021D BFFF	16K-256	Reserved	Reserved	Reserved
00 021D C000	00 021D C0FF	256	Reserved	Reserved	Reserved
00 021D C100	00 021D EFFF	12K-256	Reserved	Reserved	Reserved
00 021D F000	00 021D F07F	128	Reserved	Reserved	Reserved
00 021D F080	00 021D FFFF	4K-128	Reserved	Reserved	Reserved
00 021E 0000	00 021E FFFF	64K	Reserved	Reserved	Reserved
00 021F 0000	00 021F 07FF	2K	Reserved	Reserved	Reserved
00 021F 0800	00 021F 0FFF	2K	Reserved	Reserved	Reserved

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 021F 1000	00 021F 17FF	2K	Reserved	Reserved	Reserved
00 021F 1800	00 021F 3FFF	10K	Reserved	Reserved	Reserved
00 021F 4000	00 021F 47FF	2K	Reserved	Reserved	Reserved
00 021F 4800	00 021F 7FFF	14K	Reserved	Reserved	Reserved
00 021F 8000	00 021F 87FF	2K	Reserved	Reserved	Reserved
00 021F 8800	00 021F BFFF	14K	Reserved	Reserved	Reserved
00 021F C000	00 021F C7FF	2K	Reserved	Reserved	Reserved
00 021F C800	00 021F FFFF	14K	Reserved	Reserved	Reserved
00 0220 0000	00 0220 007F	128	Timer0	Timer0	Timer0
00 0220 0080	00 0220 FFFF	64K-128	Reserved	Reserved	Reserved
00 0221 0000	00 0221 007F	128	Reserved	Reserved	Reserved
00 0221 0080	00 0221 FFFF	64K-128	Reserved	Reserved	Reserved
00 0222 0000	00 0222 007F	128	Reserved	Reserved	Reserved
00 0222 0080	00 0222 FFFF	64K-128	Reserved	Reserved	Reserved
00 0223 0000	00 0223 007F	128	Reserved	Reserved	Reserved
00 0223 0080	00 0223 FFFF	64K-128	Reserved	Reserved	Reserved
00 0224 0000	00 0224 007F	128	Reserved	Reserved	Reserved
00 0224 0080	00 0224 FFFF	64K-128	Reserved	Reserved	Reserved
00 0225 0000	00 0225 007F	128	Reserved	Reserved	Reserved
00 0225 0080	00 0225 FFFF	64K-128	Reserved	Reserved	Reserved
00 0226 0000	00 0226 007F	128	Reserved	Reserved	Reserved
00 0226 0080	00 0226 FFFF	64K-128	Reserved	Reserved	Reserved
00 0227 0000	00 0227 007F	128	Reserved	Reserved	Reserved
00 0227 0080	00 0227 FFFF	64K-128	Reserved	Reserved	Reserved
00 0228 0000	00 0228 007F	128	Timer 8	Timer 8	Timer 8
00 0228 0080	00 0228 FFFF	64K-128	Reserved	Reserved	Reserved
00 0229 0000	00 0229 007F	128	Timer 9	Timer 9	Timer 9
00 0229 0080	00 0229 FFFF	64K-128	Reserved	Reserved	Reserved
00 022A 0000	00 022A 007F	128	Timer 10	Timer 10	Timer 10
00 022A 0080	00 022A FFFF	64K-128	Reserved	Reserved	Reserved
00 022B 0000	00 022B 007F	128	Timer 11	Timer 11	Timer 11
00 022B 0080	00 022B FFFF	64K-128	Reserved	Reserved	Reserved
00 022C 0000	00 022C 007F	128	Timer 12	Timer 12	Timer 12
00 022C 0080	00 022C FFFF	64K-128	Reserved	Reserved	Reserved
00 022D 0000	00 022D 007F	128	Timer 13	Timer 13	Timer 13
00 022D 0080	00 022D FFFF	64K-128	Reserved	Reserved	Reserved
00 022E 0000	00 022E 007F	128	Timer 14	Timer 14	Timer 14
00 022E 0080	00 022E FFFF	64K-128	Reserved	Reserved	Reserved
00 022F 0000	00 022F 007F	128	Timer 15	Timer 15	Timer 15
00 022F 0080	00 022F 00FF	128	Timer 16	Timer 16	Timer 16
00 022F 0100	00 022F 017F	128	Timer 17	Timer 17	Timer 17
00 022F 0180	00 022F 01FF	128	Timer 18	Timer 18	Timer 18
00 022F 0200	00 022F 027F	128	Timer 19	Timer 19	Timer 19

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 0230 0000	00 0230 FFFF	64K	Reserved	Reserved	Reserved
00 0231 0000	00 0231 01FF	512	PLL Controller	PLL Controller	PLL Controller
00 0231 0200	00 0231 9FFF	40K-512	Reserved	Reserved	Reserved
00 0231 A000	00 0231 BFFF	8K	HyperLink0 SerDes Config	HyperLink0 SerDes Config	HyperLink0 SerDes Config
00 0231 C000	00 0231 DFFF	8K	Reserved	Reserved	Reserved
00 0231 E000	00 0231 FFFF	8K	10GbE SerDes Config	10GbE SerDes Config	10GbE SerDes Config
00 0232 0000	00 0232 3FFF	16K	PCIe0 SerDes Config	PCIe0 SerDes Config	PCIe0 SerDes Config
00 0232 4000	00 0232 5FFF	8K	SGMII 1 SerDes Config	SGMII 1 SerDes Config	SGMII 1 SerDes Config
00 0232 5000	00 0232 7FFF	8K	PCIe1SerDes Config	PCIe1SerDes Config	PCIe1SerDes Config
00 0232 8000	00 0232 8FFF	4K	Reserved	Reserved	Reserved
00 0232 9000	00 0232 9FFF	4K	DDRA PHY Config	DDRA PHY Config	DDRA PHY Config
00 0232 A000	00 0232 BFFF	8K	SGMII 0 SerDes Config	SGMII 0 SerDes Config	SGMII 0 SerDes Config
00 0232 C000	00 0232 CFFF	4K	Reserved	Reserved	Reserved
00 0232 D000	00 0232 DFFF	4K	Reserved	Reserved	Reserved
00 0232 E000	00 0232 FFFF	4K	Reserved	Reserved	Reserved
00 0233 0000	00 0233 03FF	1K	SmartReflex0	SmartReflex0	SmartReflex0
00 0233 0400	00 0233 07FF	1K	Reserved	Reserved	Reserved
00 0233 0400	00 0233 FFFF	62K	Reserved	Reserved	Reserved
00 0234 0000	00 0234 00FF	256	Reserved	Reserved	Reserved
00 0234 0100	00 0234 3FFF	16K	Reserved	Reserved	Reserved
00 0234 4000	00 0234 40FF	256	Reserved	Reserved	Reserved
00 0234 4100	00 0234 7FFF	16K	Reserved	Reserved	Reserved
00 0234 8000	00 0234 80FF	256	Reserved	Reserved	Reserved
00 0234 8100	00 0234 BFFF	16K	Reserved	Reserved	Reserved
00 0234 C000	00 0234 C0FF	256	Reserved	Reserved	Reserved
00 0234 C100	00 0234 FFFF	16K	Reserved	Reserved	Reserved
00 0235 0000	00 0235 0FFF	4K	Power sleep controller (PSC)	Power sleep controller (PSC)	Power sleep controller (PSC)
00 0235 1000	00 0235 FFFF	64K-4K	Reserved	Reserved	Reserved
00 0236 0000	00 0236 03FF	1K	Memory protection unit (MPU) 0	Memory protection unit (MPU) 0	Memory protection unit (MPU) 0
00 0236 0400	00 0236 7FFF	31K	Reserved	Reserved	Reserved
00 0236 8000	00 0236 83FF	1K	Memory protection unit (MPU) 1	Memory protection unit (MPU) 1	Memory protection unit (MPU) 1
00 0236 8400	00 0236 FFFF	31K	Reserved	Reserved	Reserved
00 0237 0000	00 0237 03FF	1K	Memory protection unit (MPU) 2	Memory protection unit (MPU) 2	Memory protection unit (MPU) 2
00 0237 0400	00 0237 7FFF	31K	Reserved	Reserved	Reserved
00 0237 8000	00 0237 83FF	1K	Reserved	Reserved	Reserved
00 0237 8400	00 0237 FFFF	31K	Reserved	Reserved	Reserved
00 0238 0000	00 0238 03FF	1K	Reserved	Reserved	Reserved
00 0238 8000	00 0238 83FF	1K	Memory protection unit (MPU) 5	Memory protection unit (MPU) 5	Memory protection unit (MPU) 5
00 0238 8400	00 0238 87FF	1K	Reserved	Reserved	Reserved
00 0238 8800	00 0238 8BFF	1K	Memory protection unit (MPU) 7	Memory protection unit (MPU) 7	Memory protection unit (MPU) 7
00 0238 8C00	00 0238 8FFF	1K	Memory protection unit (MPU) 8	Memory protection unit (MPU) 8	Memory protection unit (MPU) 8
00 0238 9000	00 0238 93FF	1K	Memory protection unit (MPU) 9	Memory protection unit (MPU) 9	Memory protection unit (MPU) 9
00 0238 9400	00 0238 97FF	1K	Memory protection unit (MPU) 10	Memory protection unit (MPU) 10	Memory protection unit (MPU) 10

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 0238 9800	00 0238 9BFF	1K	Memory protection unit (MPU) 11	Memory protection unit (MPU) 11	Memory protection unit (MPU) 11
00 0238 9C00	00 0238 9FFF	1K	Memory protection unit (MPU) 12	Memory protection unit (MPU) 12	Memory protection unit (MPU) 12
00 0238 A000	00 0238 A3FF	1K	Memory protection unit (MPU) 13	Memory protection unit (MPU) 13	Memory protection unit (MPU) 13
00 0238 A400	00 0238 A7FF	1K	Memory protection unit (MPU) 14	Memory protection unit (MPU) 14	Memory protection unit (MPU) 14
00 0238 A800	00 023F FFFF	471K	Reserved	Reserved	Reserved
00 0240 0000	00 0243 FFFF	256K	Reserved	Reserved	Reserved
00 0244 0000	00 0244 3FFF	16K	DSP trace formatter 0	DSP trace formatter 0	DSP trace formatter 0
00 0244 4000	00 0244 FFFF	48K	Reserved	Reserved	Reserved
00 0245 0000	00 0245 3FFF	16K	Reserved	Reserved	Reserved
00 0245 4000	00 0245 FFFF	48K	Reserved	Reserved	Reserved
00 0246 0000	00 0246 3FFF	16K	Reserved	Reserved	Reserved
00 0246 4000	00 0246 FFFF	48K	Reserved	Reserved	Reserved
00 0247 0000	00 0247 3FFF	16K	Reserved	Reserved	Reserved
00 0247 4000	00 0247 FFFF	48K	Reserved	Reserved	Reserved
00 0248 0000	00 0248 3FFF	16K	Reserved	Reserved	Reserved
00 0248 4000	00 0248 FFFF	48K	Reserved	Reserved	Reserved
00 0249 0000	00 0249 3FFF	16K	Reserved	Reserved	Reserved
00 0249 4000	00 0249 FFFF	48K	Reserved	Reserved	Reserved
00 024A 0000	00 024A 3FFF	16K	Reserved	Reserved	Reserved
00 024A 4000	00 024A FFFF	48K	Reserved	Reserved	Reserved
00 024B 0000	00 024B 3FFF	16K	Reserved	Reserved	Reserved
00 024B 4000	00 024B FFFF	48K	Reserved	Reserved	Reserved
00 024C 0000	00 024C 01FF	512	Reserved	Reserved	Reserved
00 024C 0200	00 024C 03FF	1K-512	Reserved	Reserved	Reserved
00 024C 0400	00 024C 07FF	1K	Reserved	Reserved	Reserved
00 024C 0800	00 024C FFFF	62K	Reserved	Reserved	Reserved
00 024D 0000	00 024F FFFF	192K	Reserved	Reserved	Reserved
00 0250 0000	00 0250 007F	128	Reserved	Reserved	Reserved
00 0250 0080	00 0250 7FFF	32K-128	Reserved	Reserved	Reserved
00 0250 8000	00 0250 FFFF	32K	Reserved	Reserved	Reserved
00 0251 0000	00 0251 FFFF	64K	Reserved	Reserved	Reserved
00 0252 0000	00 0252 03FF	1K	Reserved	Reserved	Reserved
00 0252 0400	00 0252 FFFF	64K-1K	Reserved	Reserved	Reserved
00 0253 0000	00 0253 007F	128	I^2C0	I^2C0	I^2C0
00 0253 0080	00 0253 03FF	1K-128	Reserved	Reserved	Reserved
00 0253 0400	00 0253 047F	128	I^2C1	I^2C1	I^2C1
00 0253 0480	00 0253 07FF	1K-128	Reserved	Reserved	Reserved
00 0253 0800	00 0253 087F	128	I^2C2	I^2C2	I^2C2
00 0253 0880	00 0253 0BFF	1K-128	Reserved	Reserved	Reserved
00 0253 0C00	00 0253 0C3F	64	UART0	UART0	UART0
00 0253 0C40	00 0253 FFFF	1K-64	Reserved	Reserved	Reserved
00 0253 1000	00 0253 103F	64	UART1	UART1	UART1
00 0253 1040	00 0253 FFFF	60K-64	Reserved	Reserved	Reserved

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 0254 0000	00 0255 FFFF	128K	Reserved	Reserved	Reserved
00 0256 0080	00 0257 FFFF	128K	ARM CorePac INTC	ARM CorePac INTC	ARM CorePac INTC
00 0258 0000	00 025F FFFF	512K	Reserved	Reserved	Reserved
00 0260 0000	00 0260 1FFF	8K	Secondary interrupt controller (CIC) 0	Secondary interrupt controller (CIC) 0	Secondary interrupt controller (CIC) 0
00 0260 2000	00 0260 3FFF	8K	Reserved	Reserved	Reserved
00 0260 4000	00 0260 5FFF	8K	Reserved	Reserved	Reserved
00 0260 6000	00 0260 7FFF	8K	Reserved	Reserved	Reserved
00 0260 8000	00 0260 9FFF	8K	Secondary interrupt controller (CIC) 2	Secondary interrupt controller (CIC) 2	Secondary interrupt controller (CIC) 2
00 0260 A000	00 0260 BEFF	8K-256	Reserved	Reserved	Reserved
00 0260 BF00	00 0260 BFFF	256	GPIO Config	GPIO Config	GPIO Config
00 0260 C000	00 0261 BFFF	64K	Reserved	Reserved	Reserved
00 0261 C000	00 0261 FFFF	16K	Reserved	Reserved	Reserved
00 0262 0000	00 0262 0FFF	4K	BOOTCFG chip-level registers	BOOTCFG chip-level registers	BOOTCFG chip-level registers
00 0262 1000	00 0262 FFFF	60K	Reserved	Reserved	Reserved
00 0263 0000	00 0263 FFFF	64K	USB 0 PHY CFG	USB 0 PHY CFG	USB 0 PHY CFG
00 0264 0000	00 0264 07FF	2K	Semaphore Config	Semaphore Config	Semaphore Config
00 0264 0800	00 0264 FFFF	62K	Reserved	Reserved	Reserved
00 0265 0000	00 0267 FFFF	192K	Reserved	Reserved	Reserved
00 0268 0000	00 0268 FFFF	512K	USB 0 MMR CFG	USB 0 MMR CFG	USB 0 MMR CFG
00 0270 0000	00 0270 7FFF	32K	EDMA channel controller (TPCC) 0	EDMA channel controller (TPCC) 0	EDMA channel controller (TPCC) 0
00 0270 8000	00 0270 FFFF	32K	EDMA channel controller (TPCC) 4	EDMA channel controller (TPCC) 4	EDMA channel controller (TPCC) 4
00 0271 0000	00 0271 FFFF	64K	Reserved	Reserved	Reserved
00 0272 0000	00 0272 7FFF	32K	EDMA channel controller (TPCC) 1	EDMA channel controller (TPCC) 1	EDMA channel controller (TPCC) 1
00 0272 8000	00 0272 FFFF	32K	EDMA channel controller (TPCC) 3	EDMA channel controller (TPCC) 3	EDMA channel controller (TPCC) 3
00 0273 0000	00 0273 FFFF	64K	Reserved	Reserved	Reserved
00 0274 0000	00 0274 7FFF	32K	EDMA channel controller (TPCC) 2	EDMA channel controller (TPCC) 2	EDMA channel controller (TPCC) 2
00 0274 8000	00 0275 FFFF	96K	Reserved	Reserved	Reserved
00 0276 0000	00 0276 03FF	1K	EDMA TPCC0 transfer controller (TPTC) 0	EDMA TPCC0 transfer controller (TPTC) 0	EDMA TPCC0 transfer controller (TPTC) 0
00 0276 0400	00 0276 7FFF	31K	Reserved	Reserved	Reserved
00 0276 8000	00 0276 83FF	1K	EDMA TPCC0 transfer controller (TPTC) 1	EDMA TPCC0 transfer controller (TPTC) 1	EDMA TPCC0 transfer controller (TPTC) 1
00 0276 8400	00 0276 FFFF	31K	Reserved	Reserved	Reserved
00 0277 0000	00 0277 03FF	1K	EDMA TPCC1 transfer controller (TPTC) 0	EDMA TPCC1 transfer controller (TPTC) 0	EDMA TPCC1 transfer controller (TPTC) 0
00 0277 0400	00 0277 7FFF	31K	Reserved	Reserved	Reserved
00 0277 8000	00 0277 83FF	1K	EDMA TPCC1 transfer controller (TPTC) 1	EDMA TPCC1 transfer controller (TPTC) 1	EDMA TPCC1 transfer controller (TPTC) 1
00 0278 0400	00 0277 FFFF	31K	Reserved	Reserved	Reserved

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 0278 0000	00 0278 03FF	1K	EDMA TPCC1 transfer controller (TPTC) 2	EDMA TPCC1 transfer controller (TPTC) 2	EDMA TPCC1 transfer controller (TPTC) 2
00 0278 0400	00 0278 7FFF	31K	Reserved	Reserved	Reserved
00 0278 8000	00 0278 83FF	1K	EDMA TPCC1 transfer controller (TPTC) 3	EDMA TPCC1 transfer controller (TPTC) 3	EDMA TPCC1 transfer controller (TPTC) 3
00 0278 8400	00 0278 FFFF	31K	Reserved	Reserved	Reserved
00 0279 0000	00 0279 03FF	1K	EDMA TPCC2 transfer controller (TPTC) 0	EDMA TPCC2 transfer controller (TPTC) 0	EDMA TPCC2 transfer controller (TPTC) 0
00 0279 0400	00 0279 7FFF	31K	Reserved	Reserved	Reserved
00 0279 8000	00 0279 83FF	1K	EDMA TPCC2 transfer controller (TPTC) 1	EDMA TPCC2 transfer controller (TPTC) 1	EDMA TPCC2 transfer controller (TPTC) 1
00 0279 8400	00 0279 FFFF	31K	Reserved	Reserved	Reserved
00 027A 0000	00 027A 03FF	1K	EDMA TPCC2 transfer controller (TPTC) 2	EDMA TPCC2 transfer controller (TPTC) 2	EDMA TPCC2 transfer controller (TPTC) 2
00 027A 0400	00 027A 7FFF	31K	Reserved	Reserved	Reserved
00 027A 8000	00 027A 83FF	1K	EDMA TPCC2 transfer controller (TPTC) 3	EDMA TPCC2 transfer controller (TPTC) 3	EDMA TPCC2 transfer controller (TPTC) 3
00 027A 8400	00 027A FFFF	31K	Reserved	Reserved	Reserved
00 027B 0000	00 027B 03FF	1K	EDMA TPCC3 transfer controller (TPTC) 0	EDMA TPCC3 transfer controller (TPTC) 0	EDMA TPCC3 transfer controller (TPTC) 0
00 027B 0400	00 027B 7FFF	31K	Reserved	Reserved	Reserved
00 027B 8000	00 027B 83FF	1K	EDMA TPCC3 transfer controller (TPTC) 1	EDMA TPCC3 transfer controller (TPTC) 1	EDMA TPCC3 transfer controller (TPTC) 1
00 027B 8400	00 027B 87FF	1K	EDMA TPCC4 transfer controller (TPTC) 0	EDMA TPCC4 transfer controller (TPTC) 0	EDMA TPCC4 transfer controller (TPTC) 0
00 027B 8800	00 027B 8BFF	1K	EEDMA TPCC4 transfer controller (TPTC) 1	EEDMA TPCC4 transfer controller (TPTC) 1	EEDMA TPCC4 transfer controller (TPTC) 1
00 027B 8C00	00 027B FFFF	29K	Reserved	Reserved	Reserved
00 027C 0000	00 027C 03FF	1K	Reserved	Reserved	Reserved
00 027C 0400	00 027C FFFF	63K	Reserved	Reserved	Reserved
00 027D 0000	00 027D 3FFF	16K	TI embedded trace buffer (TETB) - CorePac0	TI embedded trace buffer (TETB) - CorePac0	TI embedded trace buffer (TETB) - CorePac0
00 027D 4000	00 027D 7FFF	16K	TBR_ARM CorePac - Trace buffer - ARM CorePac	TBR_ARM CorePac - Trace buffer - ARM CorePac	TBR_ARM CorePac - Trace buffer - ARM CorePac
00 027D 8000	00 027D FFFF	32K	Reserved	Reserved	Reserved
00 027E 0000	00 027E 3FFF	16K	Reserved	Reserved	Reserved
00 027E 4000	00 027E FFFF	48K	Reserved	Reserved	Reserved
00 027F 0000	00 027F 3FFF	16K	Reserved	Reserved	Reserved
00 027F 4000	00 027F FFFF	48K	Reserved	Reserved	Reserved
00 0280 0000	00 0280 3FFF	16K	Reserved	Reserved	Reserved
00 0280 4000	00 0280 FFFF	48K	Reserved	Reserved	Reserved
00 0281 0000	00 0281 3FFF	16K	Reserved	Reserved	Reserved
00 0281 4000	00 0281 FFFF	48K	Reserved	Reserved	Reserved
00 0282 0000	00 0282 3FFF	16K	Reserved	Reserved	Reserved
00 0282 4000	00 0282 FFFF	48K	Reserved	Reserved	Reserved
00 0283 0000	00 0283 3FFF	16K	Reserved	Reserved	Reserved
00 0283 4000	00 0283 FFFF	48K	Reserved	Reserved	Reserved

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 0284 0000	00 0284 3FFF	16K	Reserved	Reserved	Reserved
00 0284 4000	00 0284 FFFF	48K	Reserved	Reserved	Reserved
00 0285 0000	00 0285 7FFF	32K	TBR_SYS- Trace buffer - System	TBR_SYS- Trace buffer - System	TBR_SYS- Trace buffer - System
00 0285 8000	00 0285 FFFF	32K	Reserved	Reserved	Reserved
00 0286 0000	00 028F FFFF	640K	Reserved	Reserved	Reserved
00 0290 0000	00 0293 FFFF	256K	Reserved	Reserved	Reserved
00 0294 0000	00 029F FFFF	768K	Reserved	Reserved	Reserved
00 02A0 0000	00 02AF FFFF	1M	Navigator configuration	Navigator configuration	Navigator configuration
00 02B0 0000	00 02BF FFFF	1M	Navigator linking RAM	Navigator linking RAM	Navigator linking RAM
00 02C0 0000	00 02C0 FFFF	64K	Reserved	Reserved	Reserved
00 02C1 0000	00 02C1 FFFF	64K	Reserved	Reserved	Reserved
00 02C2 0000	00 02C3 FFFF	128K	Reserved	Reserved	Reserved
00 02C4 0000	00 02C5 FFFF	128K	Reserved	Reserved	Reserved
00 02C6 0000	00 02C7 FFFF	128K	Reserved	Reserved	Reserved
00 02C8 0000	00 02C8 FFFF	64K	Reserved	Reserved	Reserved
00 02C9 0000	00 02C9 FFFF	64K	Reserved	Reserved	Reserved
00 02CA 0000	00 02CB FFFF	128K	Reserved	Reserved	Reserved
00 02CC 0000	00 02CD FFFF	128K	Reserved	Reserved	Reserved
00 02CE 0000	00 02EF FFFF	15M-896K	Reserved	Reserved	Reserved
00 02F0 0000	00 02FF FFFF	1M	10GbE Config	10GbE Config	10GbE Config
00 0300 0000	00 030F FFFF	1M	DBG Config	DBG Config	DBG Config
00 0310 0000	00 07FF FFFF	79M	Reserved	Reserved	Reserved
00 0800 0000	00 0801 FFFF	128K	Extended memory controller (XMC) configuration	Extended memory controller (XMC) configuration	Extended memory controller (XMC) configuration
00 0802 0000	00 0BBF FFFF	60M-128K	Reserved	Reserved	Reserved
00 0BC0 0000	00 0BCF FFFF	1M	Multicore shared memory controller (MSMC) config	Multicore shared memory controller (MSMC) config	Multicore shared memory controller (MSMC) config
00 0BD0 0000	00 0BFF FFFF	3M	Reserved	Reserved	Reserved
00 0C00 0000	00 0C1F FFFF	2M	Multicore shared memory (MSM)	Multicore shared memory (MSM)	Multicore shared memory (MSM)
00 0C20 0000	00 0C5F FFFF	4M	Reserved	Reserved	Reserved
00 0C60 0000	00 0FFF FFFF	58M	Reserved	Reserved	Reserved
00 1000 0000	00 107F FFFF	8M	Reserved	Reserved	Reserved
00 1080 0000	00 1087 FFFF	512K	CorePac0 L2 SRAM	CorePac0 L2 SRAM	CorePac0 L2 SRAM
00 1088 0000	00 108F FFFF	512K	Reserved	Reserved	Reserved
00 1090 0000	00 10DF FFFF	5M	Reserved	Reserved	Reserved
00 10E0 0000	00 10E0 7FFF	32K	CorePac0 L1P SRAM	CorePac0 L1P SRAM	CorePac0 L1P SRAM
00 10E0 8000	00 10EF FFFF	1M-32K	Reserved	Reserved	Reserved
00 10F0 0000	00 10F0 7FFF	32K	CorePac0 L1D SRAM	CorePac0 L1D SRAM	CorePac0 L1D SRAM
00 10F0 8000	00 117F FFFF	9M-32K	Reserved	Reserved	Reserved
00 1180 0000	00 118F FFFF	1M	Reserved	Reserved	Reserved
00 1190 0000	00 11DF FFFF	5M	Reserved	Reserved	Reserved
00 11E0 0000	00 11E0 7FFF	32K	Reserved	Reserved	Reserved
00 11E0 8000	00 11EF FFFF	1M-32K	Reserved	Reserved	Reserved

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 11F0 0000	00 11F0 7FFF	32K	Reserved	Reserved	Reserved
00 11F0 8000	00 127F FFFF	9M-32K	Reserved	Reserved	Reserved
00 1280 0000	00 128F FFFF	1M	Reserved	Reserved	Reserved
00 1290 0000	00 12DF FFFF	5M	Reserved	Reserved	Reserved
00 12E0 0000	00 12E0 7FFF	32K	Reserved	Reserved	Reserved
00 12E0 8000	00 12EF FFFF	1M-32K	Reserved	Reserved	Reserved
00 12F0 0000	00 12F0 7FFF	32K	Reserved	Reserved	Reserved
00 12F0 8000	00 137F FFFF	9M-32K	Reserved	Reserved	Reserved
00 1380 0000	00 1388 FFFF	1M	Reserved	Reserved	Reserved
00 1390 0000	00 13DF FFFF	5M	Reserved	Reserved	Reserved
00 13E0 0000	00 13E0 7FFF	32K	Reserved	Reserved	Reserved
00 13E0 8000	00 13EF FFFF	1M-32K	Reserved	Reserved	Reserved
00 13F0 0000	00 13F0 7FFF	32K	Reserved	Reserved	Reserved
00 13F0 8000	00 147F FFFF	9M-32K	Reserved	Reserved	Reserved
00 1480 0000	00 148F FFFF	1M	Reserved	Reserved	Reserved
00 1490 0000	00 14DF FFFF	5M	Reserved	Reserved	Reserved
00 14E0 0000	00 14E0 7FFF	32K	Reserved	Reserved	Reserved
00 14E0 8000	00 14EF FFFF	1M-32K	Reserved	Reserved	Reserved
00 14F0 0000	00 14F0 7FFF	32K	Reserved	Reserved	Reserved
00 14F0 8000	00 157F FFFF	9M-32K	Reserved	Reserved	Reserved
00 1580 0000	00 158F FFFF	1M	Reserved	Reserved	Reserved
00 1590 0000	00 15DF FFFF	5M	Reserved	Reserved	Reserved
00 15E0 0000	00 15E0 7FFF	32K	Reserved	Reserved	Reserved
00 15E0 8000	00 15EF FFFF	1M-32K	Reserved	Reserved	Reserved
00 15F0 0000	00 15F0 7FFF	32K	Reserved	Reserved	Reserved
00 15F0 8000	00 167F FFFF	9M-32K	Reserved	Reserved	Reserved
00 1680 0000	00 168F FFFF	1M	Reserved	Reserved	Reserved
00 1690 0000	00 16DF FFFF	5M	Reserved	Reserved	Reserved
00 16E0 0000	00 16E0 7FFF	32K	Reserved	Reserved	Reserved
00 16E0 8000	00 16EF FFFF	1M-32K	Reserved	Reserved	Reserved
00 16F0 0000	00 16F0 7FFF	32K	Reserved	Reserved	Reserved
00 16F0 8000	00 177F FFFF	9M-32K	Reserved	Reserved	Reserved
00 1780 0000	00 178F FFFF	1M	Reserved	Reserved	Reserved
00 1790 0000	00 17DF FFFF	5M	Reserved	Reserved	Reserved
00 17E0 0000	00 17E0 7FFF	32K	Reserved	Reserved	Reserved
00 17E0 8000	00 17EF FFFF	1M-32K	Reserved	Reserved	Reserved
00 17F0 0000	00 17F0 7FFF	32K	Reserved	Reserved	Reserved
00 17F0 8000	00 1FFF FFFF	129M-32K	Reserved	Reserved	Reserved
00 2000 0000	00 200F FFFF	1M	System trace manager (STM) configuration	System trace manager (STM) configuration	System trace manager (STM) configuration
00 2010 0000	00 201F FFFF	1M	Reserved	Reserved	Reserved
00 2020 0000	00 205F FFFF	4M	Reserved	Reserved	Reserved

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 2060 0000	00 206F FFFF	1M	Network Coprocessor 1(Packet Accelerator, 1-gigabit Ethernet switch subsystem and Security Accelerator)	Network Coprocessor 1(Packet Accelerator, 1-gigabit Ethernet switch subsystem and Security Accelerator)	Network Coprocessor 1(Packet Accelerator, 1-gigabit Ethernet switch subsystem and Security Accelerator)
00 2070 0000	00 2077 FFFF	512K	USB 1 MMR CFG	USB 1 MMR CFG	USB 1 MMR CFG
00 2078 0000	00 2078 FFFF	64K	USB 1 PHY CFG	USB 1 PHY CFG	USB 1 PHY CFG
00 2079 0000	00 207F FFFF	448K	Reserved	Reserved	Reserved
00 2080 0000	00 208F FFFF	1M	Reserved	Reserved	Reserved
00 2090 0000	00 209F FFFF	1M	Reserved	Reserved	Reserved
00 20A0 0000	00 20A3 FFFF	256K	Reserved	Reserved	Reserved
00 20A4 0000	00 20A4 FFFF	64K	Reserved	Reserved	Reserved
00 20A5 0000	00 20AF FFFF	704K	Reserved	Reserved	Reserved
00 20B0 0000	00 20B3 FFFF	256K	Boot ROM	Boot ROM	Boot ROM
00 20B4 0000	00 20BE FFFF	704K	Reserved	Reserved	Reserved
00 20BF 0000	00 20BF 01FF	64K	Reserved	Reserved	Reserved
00 20C0 0000	00 20FF FFFF	4M	Reserved	Reserved	Reserved
00 2100 0000	00 2100 03FF	1K	Reserved	Reserved	Reserved
00 2100 0400	00 2100 05FF	512	SPI0	SPI0	SPI0
00 2100 0600	00 2100 07FF	512	SPI1	SPI1	SPI1
00 2100 0800	00 2100 09FF	512	SPI2	SPI2	SPI2
00 2100 0A00	00 2100 0AFF	256	EMIF Config	EMIF Config	EMIF Config
00 2100 0B00	00 2100 FFFF	62K-768	Reserved	Reserved	Reserved
00 2101 0000	00 2101 01FF	512	DDR3A EMIF Config	DDR3A EMIF Config	DDR3A EMIF Config
00 2101 0200	00 2101 07FF	2K-512	Reserved	Reserved	Reserved
00 2101 0800	00 2101 09FF	512	Reserved	Reserved	Reserved
00 2101 0A00	00 2101 0FFF	2K-512	Reserved	Reserved	Reserved
00 2101 1000	00 2101 FFFF	60K	Reserved	Reserved	Reserved
00 2102 0000	00 2102 7FFF	32K	PCIe 1config	PCIe 1config	PCIe 1config
00 2102 8000	00 2103 FFFF	96K	Reserved	Reserved	Reserved
00 2104 0000	00 217F FFFF	4M-256K	Reserved	Reserved	Reserved
00 2140 0000	00 2140 00FF	256	HyperLink0 config	HyperLink0 config	HyperLink0 config
00 2140 0100	00 2140 01FF	256	Reserved	Reserved	Reserved
00 2140 0400	00 217F FFFF	4M-512	Reserved	Reserved	Reserved
00 2180 0000	00 2180 7FFF	32K	PCIe 0 config	PCIe 0 config	PCIe 0 config
00 2180 8000	00 21BF FFFF	4M-32K	Reserved	Reserved	Reserved
00 21C0 0000	00 21FF FFFF	4M	Reserved	Reserved	Reserved
00 2200 0000	00 229F FFFF	10M	Reserved	Reserved	Reserved
00 22A0 0000	00 22A0 FFFF	64K	Reserved	Reserved	Reserved
00 22A1 0000	00 22AF FFFF	1M-64K	Reserved	Reserved	Reserved
00 22B0 0000	00 22B0 FFFF	64K	Reserved	Reserved	Reserved
00 22B1 0000	00 22BF FFFF	1M-64K	Reserved	Reserved	Reserved
00 22C0 0000	00 22C0 FFFF	64K	Reserved	Reserved	Reserved
00 22C1 0000	00 22CF FFFF	1M-64K	Reserved	Reserved	Reserved
00 22D0 0000	00 22D0 FFFF	64K	Reserved	Reserved	Reserved

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 22D1 0000	00 22DF FFFF	1M-64K	Reserved	Reserved	Reserved
00 22E0 0000	00 22E0 FFFF	64K	Reserved	Reserved	Reserved
00 22E1 0000	00 22EF FFFF	1M-64K	Reserved	Reserved	Reserved
00 22F0 0000	00 22F0 FFFF	64K	Reserved	Reserved	Reserved
00 22F1 0000	00 22FF FFFF	1M-64K	Reserved	Reserved	Reserved
00 2300 0000	00 2300 FFFF	64K	Reserved	Reserved	Reserved
00 2301 0000	00 230F FFFF	1M-64K	Reserved	Reserved	Reserved
00 2310 0000	00 2310 FFFF	64K	Reserved	Reserved	Reserved
00 2311 0000	00 231F FFFF	1M-64K	Reserved	Reserved	Reserved
00 2320 0000	00 2324 FFFF	384K	Reserved	Reserved	Reserved
00 2325 0000	00 239F FFFF	8M-384K	Reserved	Reserved	Reserved
00 23A0 0000	00 23BF FFFF	2M	Navigator	Navigator	Navigator
00 23C0 0000	00 23FF FFFF	4M	Reserved	Reserved	Reserved
00 2400 0000	00 24FF FFFF	16M	NETCP15 config	NETCP15 config	NETCP15 config
00 2500 0000	00 2507 FFFF	512K	USB1 MMR config	USB1 MMR config	USB1 MMR config
00 2508 0000	00 2508 FFFF	64K	USB1 PHY config	USB1 PHY config	USB1 PHY config
00 2500 0000	00 27FF FFFF	48M-576K	Reserved	Reserved	Reserved
00 2800 0000	00 2FFF FFFF	128M	Reserved	Reserved	Reserved
00 3000 0000	00 33FF FFFF	64M	EMIF16 CS2	EMIF16 CS2	EMIF16 CS2
00 3400 0000	00 37FF FFFF	64M	EMIF16 CS3	EMIF16 CS3	EMIF16 CS3
00 3800 0000	00 3BFF FFFF	64M	EMIF16 CS4	EMIF16 CS4	EMIF16 CS4
00 3C00 0000	00 3FFF FFFF	64M	EMIF16 CS5	EMIF16 CS5	EMIF16 CS5
00 4000 0000	00 4FFF FFFF	256M	HyperLink0 data	HyperLink0 data	HyperLink0 data
00 5000 0000	00 5FFF FFFF	256M	PCIe 0 data	PCIe 0 data	PCIe 0 data
00 6000 0000	00 6FFF FFFF	256M	PCIe 1data	PCIe 1data	PCIe 1data
00 7000 0000	00 FFFF FFFF	2304M	Reserved	Reserved	Reserved
01 0000 0000	01 20FF FFFF	528M	Reserved	Reserved	Reserved
01 2100 0000	01 2100 01FF	512	Reserved	DDR3A EMIF configuration (1)	DDR3A EMIF configuration (1)
01 2100 0200	07 FFFF FFFF	32G-512	Reserved	Reserved	Reserved
08 0000 0000	09 FFFF FFFF	8G	DDR3A data	DDR3A data (1)	DDR3A data (1)
0A 0000 0000	FF FFFF FFFF	984G	Reserved	Reserved	Reserved
End of Table 6-1					

2.2 EVM Boot Mode

The EVMK2E has 4 sliding DIP switches (Board Ref. SW1) to determine boot mode and boot configuration. EVM Boot mode and Boot Configuration Switch Settings given in Table 3.22. DIP switch: (SW1) that can set up to 16 different pre-defined configurations to the BMC. Each DIP configuration to latch in and set up the different boot mode when the SoC RESETFULL reset signal is de-asserted. This occurs when power is applied the board, after the user presses the MCU_RESET push button or after a POR reset is requested from the MMC.SW1 determines general DSP configuration, little or Big Endian mode as well as boot mode selection.

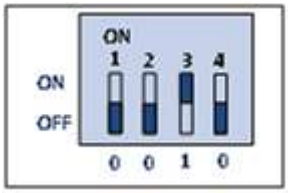

Figure 2.1: EVM DIP Switch settings for ARM SPI boot

More information about using these DIP switches is contained in section 3.3 of this document. For more information on DSP supported Boot Modes. Please refer SoC Data Manual and C66x Boot Loader User Guide.

2.3 Board Revision ID

Board PCB (Printed Circuit Board) and PCA (Printed Circuit Assembly) revision are located in bottom silk, as shown in Figure 2.2. Table 2.2 describes the PCA/PCB revisions.

Figure 2.2: EVM Board Revision

Table 2.2: PCA/PCB revision description

Kit Revision	PCA Rev	PCB Rev	Description
1.0.1.1	18-00175-01	17-00175-01	Proto (Initial engineering samples)
1.0.2.0	18-00175-02	17-00175-02	Alpha + Beta Build

Note: Last two digits represent major PCB / PCA revision number.

2.4 JTAG - Emulation Overview

EVMK2E has on-board XDS200 embedded JTAG emulation circuitry; hence user does not require any external emulator to connect EVM with Code Composer Studio. User can connect CCS with target DSP in EVM through USB cable supplied along with this board. The EVM supports two different types of DSP Emulation - “USB mini-B” and “60-pin MIPI JTAG-DSP”. USB emulation is supported through an on-board, optimized XDS200-class embedded emulation circuit.

In case user wishes to connect external emulator to EVM, the MIPI 60-pin JTAG header (EMU1) is provided on-board for high speed real-time emulation. The MIPI 60-pin JTAG supports all standard (XDS510 or XDS560) TI DSP emulators. Please refer to the documentation supplied with your emulator for connection assistance.

On-board XDS200 embedded JTAG emulator is the default connection to DSP, however when external emulator is connected to EVM, board circuitry switches automatically to give DSP’s emulation access to external emulator. When on-board emulator and external emulator both are connected at the same time, external emulator has priority and on-board emulator is disconnected from DSP.

DSP can also be accessed through the JTAG port on the AMC edge connector. When both the emulators (i.e. on board XDS200 and external emulator) are not present then AMC backplane JTAG takes priority and hence SoC can be accessed through it. The JTAG interface among the DSP, on-board emulator, external emulator and the AMC edge connector is shown in the below Figure 2.3.

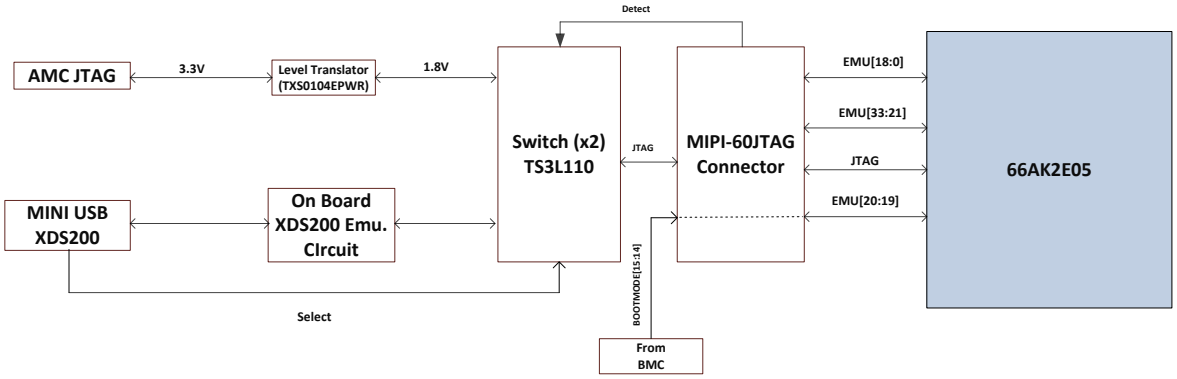

Figure 2.3: EVMK2E JTAG emulation

2.5 Clock Domains

The EVM incorporates a variety of clocks to the SoC as well as other devices which are configured automatically during the power up configuration sequence by BMC. The
Figure **2.4** below illustrates clocking for the system in the EVM module.

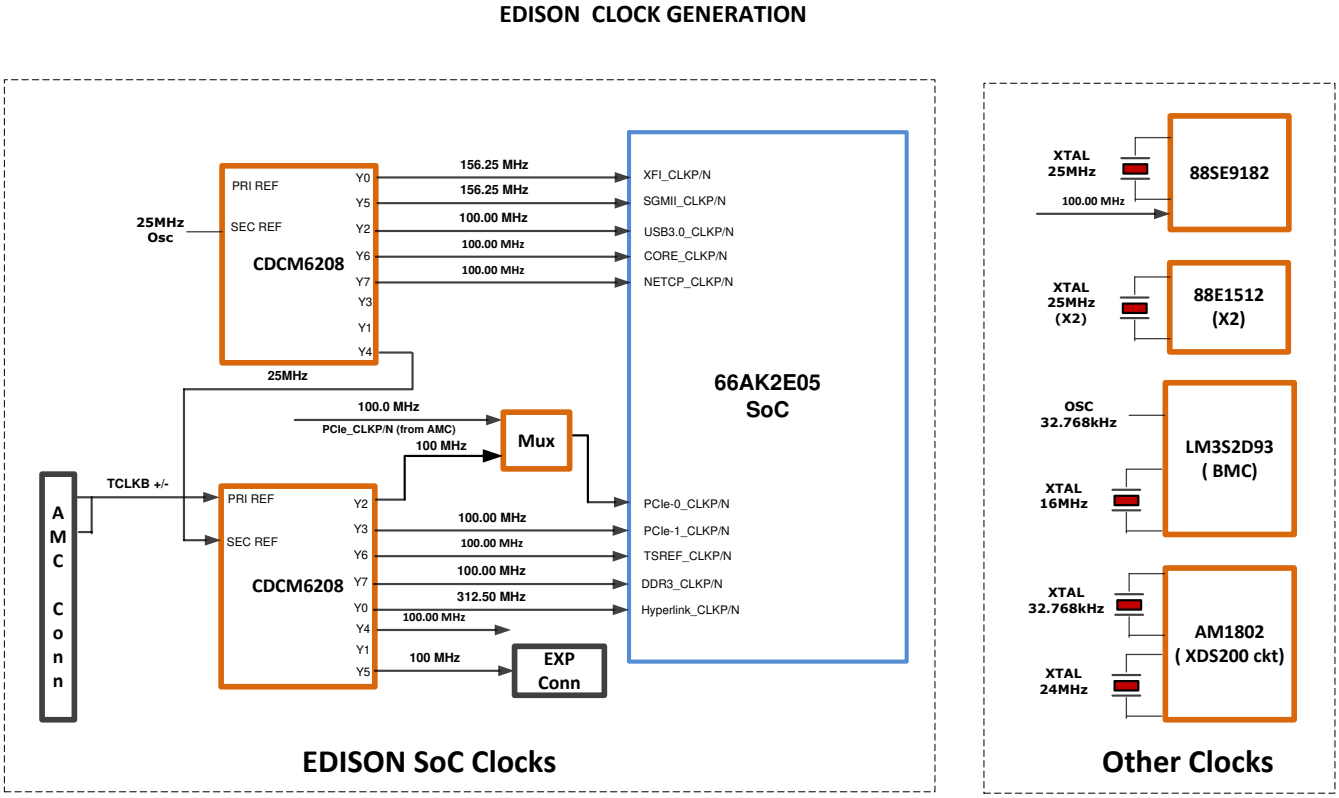

Figure 2.4: EVMK2E Clock Domains

Table 2.3: EVMK2E Clock Configuration

Clock	Frequency	Description
CORECLK(P/N)	100MHz	SoC core clock
DDRCLK(P|N)	100MHz	SoC DDR3 clock
XFICLK(P/N)	156.25MHz	SoC XFI clock
SGMIICLK(P/N)	156.25MHz	SoC SGMII clock
USB3.0CLK(P/N)	100MHz	SoC USB3.0 clock
NETCPCLK(P/N)	100MHz	SoC NETCP clock
HyperLinkCLK(P|N)	312.50MHz	SoC HyperLink clock
PCIE0CLK(P|N)	100MHz	SoC PCIe-0 clock
PCIE1CLK(P|N)	100MHz	SoC PCIe-1 clock
SATACLK(P/N)	100MHz	PCIe to SATA controller clock
TSIPCLK	16.38MHz	SoC TSIP Clock

2.6 I2C Boot EEPROM / SPI NOR Flash

The I2C modules on the 66AK2EX will be used by the DSP to control local peripheral ICs (DACs, ADCs, etc.) or may be used to communicate with other controllers in a system or to implement a user interface.

The I2C bus is connected to one EEPROM and to the 120-pin expansion header (CN7). There are two banks in the I2C EEPROM which respond separately at addresses 0x50 and 0x51. These banks can be loaded with demonstration programs. Currently, the bank at 0x50 contains the I2C boot code and PLL initialization procedure and the bank at 0x51 contains the second level boot-loader program. The second level boot-loader can be used to either run the POST program or launch the OOB demonstration from NOR flash memory.

The serial peripherals interconnect (SPI) module provides an interface between the SoC and other SPI-compliant devices. The primary intent of this interface is to allow for connection to a SPI ROM for boot. The SPI module on SoC is supported only in Master mode.

16MB NOR FLASH (part number N25Q032A11 from NUMONYX) is attached to CS0z on SoC. It contains demonstration programs such as POST or OOB demo. The CS1z of SPI is used by the DSP to access registers within BMC.

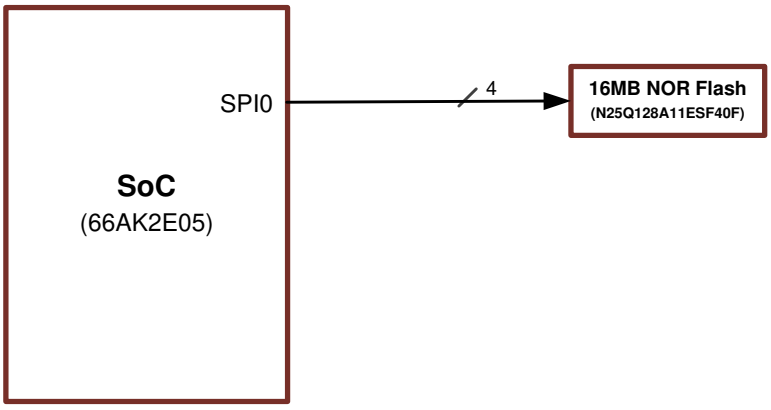

Figure 2.5: EVMK2E SPI NOR Flash Connection

2.7 BMC and MMC

The BMC (TI LMS2D93) controls the reset mechanism of the SoC and provides boot mode and boot Configuration data to SoC through SW1. BMC also provides the transformation of TDM Frame Sync and Clock between AMC connector and SoC. The BMC also supports 3 user LEDs and 1 user Switch through control registers. All BMC registers are accessible over the SPI interface.

The EVM also supports a limited set of Intelligent Platform Management Interface (IPMI) commands using Microcontroller based on Texas Instruments LMS2D93.

The BMC will communicate with MicroTCA Carrier Hub (MCH) over IPMB (Intelligent Platform Management Bus) when inserted into an AMC slot of a PICMG® MTCA.0 R2.0 compliant chassis. The primary purpose of the BMC is to provide necessary information to MCH, to enable the payload power to EVM when it is inserted into the MicroTCA chassis.

The EVM also supports a Blue LED (D5) and Red LED (D3) on the front panel as specified in PICMG® AMC.0 R2.0 AdvancedMC base specification. Both of these LEDs will blink as part of initialization process when the BMC will receive management power.

Blue LED (D4):

Blue LED will turn ON when MicroTCA chassis is powered ON and an EVM is inserted into it. The blue LED will turn OFF when payload power is enabled to the EVM by the MCH.

Red LED (D3):

Red colored D3 will normally be OFF. It will turn ON to provide basic feedback about failures and out of service. The Figure 2.6 below shows the interface between SoC and BMC.

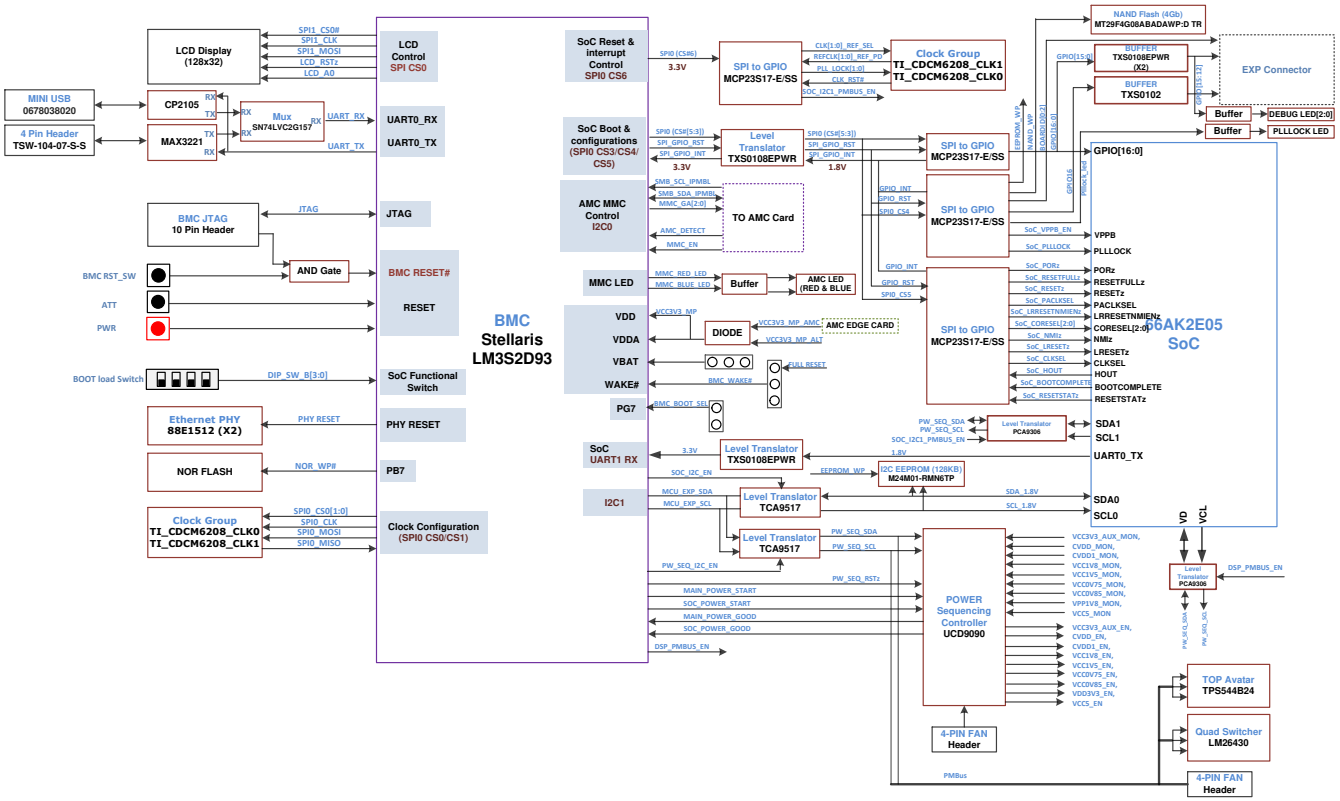

Figure 2.6: EVMK2E BMC Connections

2.8 Gigabit Ethernet connection (8 Port SGMII)

The EVM provides connectivity for both SGMII Gigabit Ethernet ports on the EVM. These are shown in Figure 2.7 below:

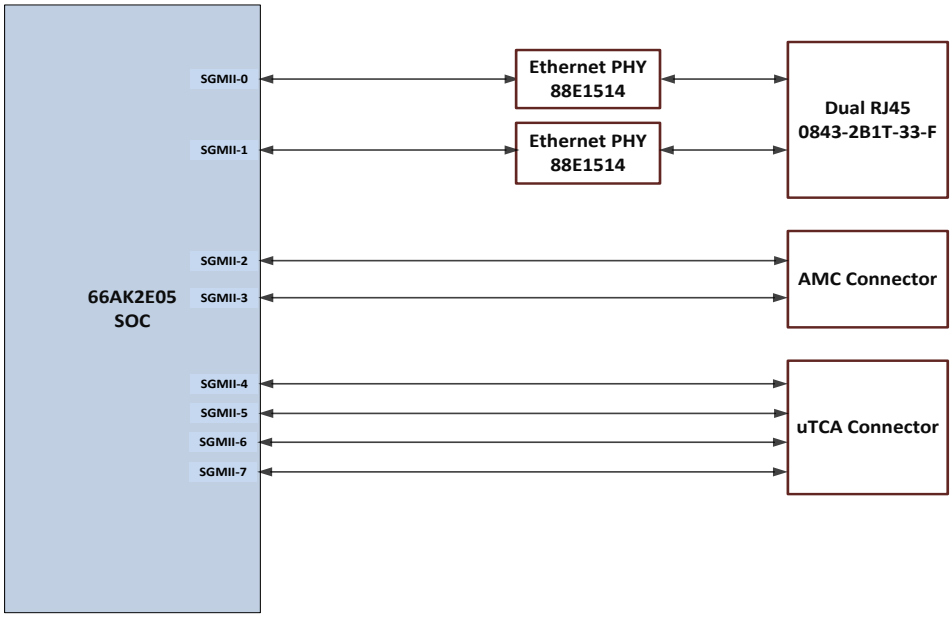

Figure 2.7: EVM Ethernet Routing

The Ethernet PHY (PHY1 and PHY2) is connected to SoC SGMII 0 and 1 to provide a copper interface and routed to a Gigabit RJ-45 connector. The SGMII 2 & 3 of SoC is routed to Port 0 and 1 of the AMC edge connector backplane interface. The SGMII 4 to 7 is routed to uRTM connector.

Please refer below block diagram for the XFI and SGMII MDIO interface implementation on EVMK2E.

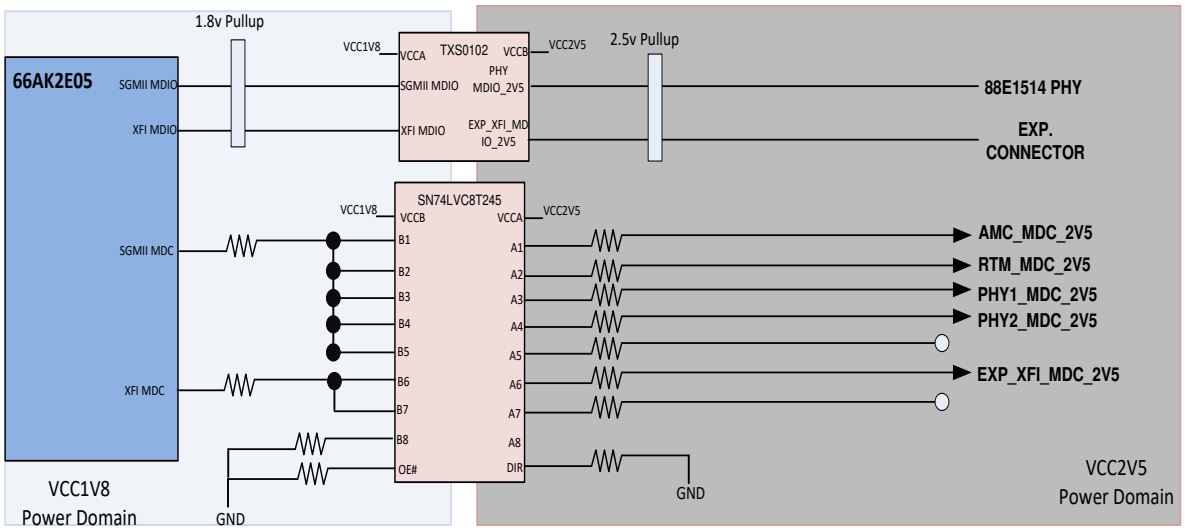

Figure 2.8: EVMK2E XFI and SGMII MDIO Routing

2.9 DDR3 SO-DIMM Memory Module Interface

The EVMK2E has a DDR3 interface connects to one expansion SO-DIMM Socket on EVM. This configuration allow user to use wide (64-bit) modes of the DDR3 EMIF. EVMK2E have default 4GB DDR3 SODIMM module and it will support 1GB to 8GB DDR3 memory. Please refer below Figure 2.9 for DDR3 SO-DIMM interface.

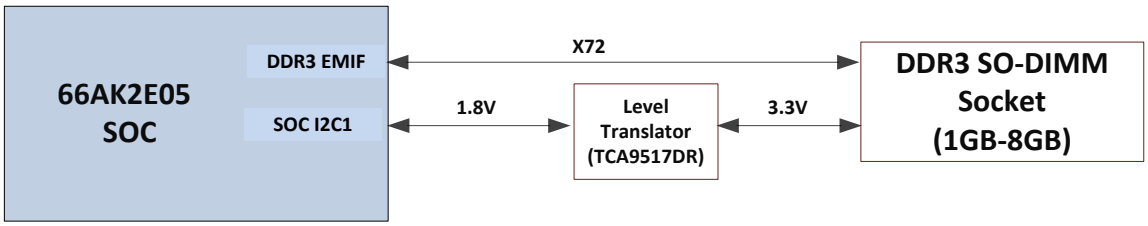

Figure 2.9: EVMK2E DDR3 SO-DIMM Interface

2.10 16-bit Asynchronous External Memory Interface (EMIF-16)

The SoC EMIF-16 interface connects to one 4Gbit (512MB) NAND flash device and 120-pin expansion header (CN7) on the EVM. The EMIF16 module provides an interface between SoC and asynchronous external memories such as NAND,NOR flash and ASRAM memory. For more information see the External Memory Interface (EMIF16) for KeyStone Devices User Guide. Micron NAND flash (512MB) is used in EMIF Interface. The Figure 2.10 shows the EMIF-16 connections.

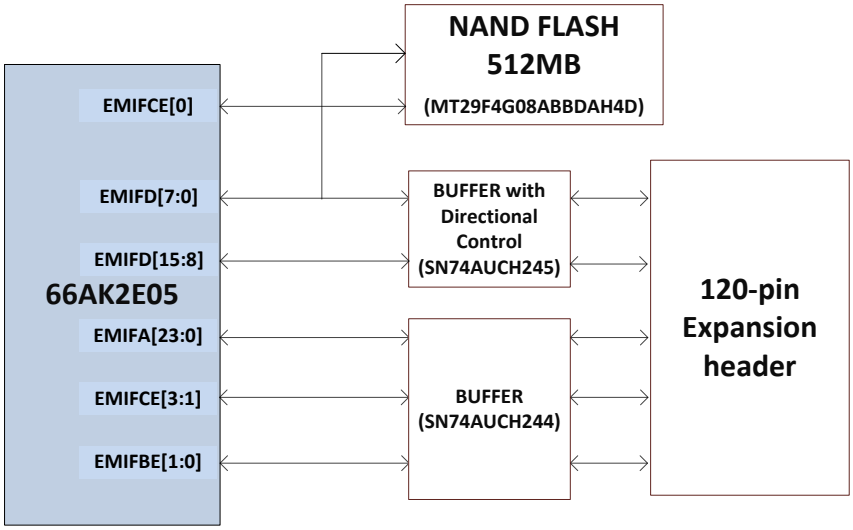

Figure 2.10: EVMK2E EMIF16 Interface

2.11 HyperLink Interface

The SoC provides the one HyperLink bus for companion chip/die interfaces. This group has a four-lane SerDes interface designed to operate at 12.5 Gbps per lane from pin-to-pin. The interface is used to connect with external accelerators.

The interface includes the Serial Station Management Interfaces used to send power management and flow messages between devices. This consists of four LVCMOS inputs and four LVCMOS outputs configured as two 2-wire output buses and two 2-wire input buses. Each 2-wire bus includes a data signal and a clock signal. The
Figure **2.11** illustrates the Hyperlink bus connections on the EVM.

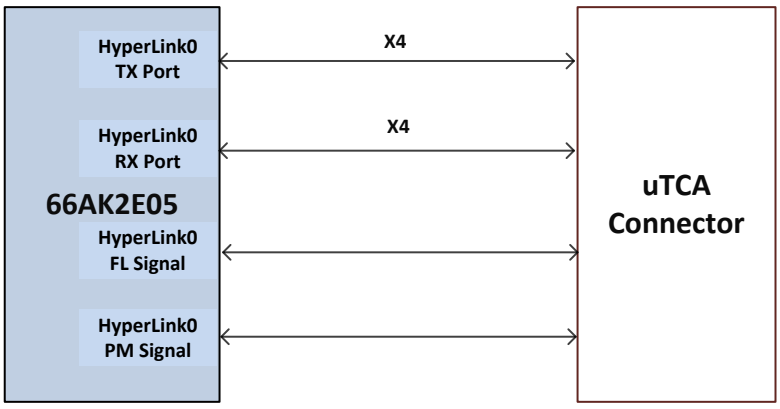

Figure 2.11: EVMK2E HyperLink Interface

2.12 PCIe and SATA Interface

The EVM has 2 ports of PCIe. Each port has 2 lanes. Port-0 on EVM provides a connection between the DSP and AMC edge connector and Port-1 provides a connection between DSP and PCIe to SATA3.0 controllers.

Port-1 of SATA controller Provides connection between SATA controller and AMC edge connector and Port-2 provides connections between SATA controllers to SATA HDD 7 pin Data connector.

The PCI Express interface provides low pin count, high reliability, and high-speed data transfer at rates of 5.0 Gbps per lane on the serial links. For more information, see the Peripheral Component Interconnect Express (PCIe) for KeyStone Devices User Guide.

The Figure 2.12 below shows the PCIe and SATA connectivity to AMC backplane on EVM.

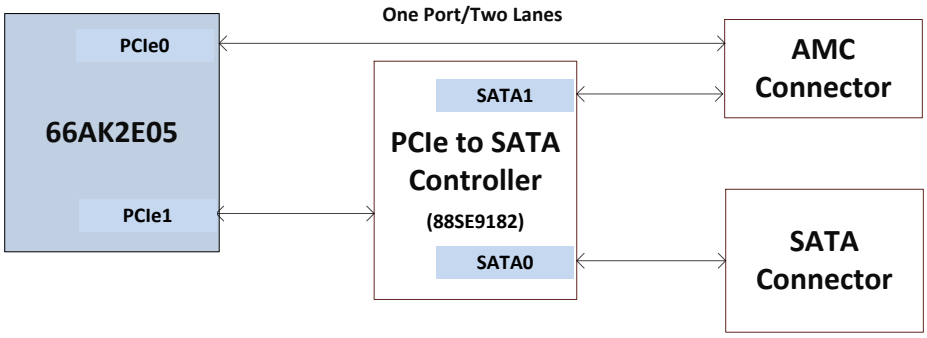

Figure 2.12: EVMK2E PCIe Interface

2.13 UART Interface

A serial port is provided for UART communication by SoC. This serial port can be accessed either through USB connector (J1) or through 4-pin (Tx, Rx, detect and Gnd) serial port header (SOC & BMC). The selection can be made through UART Cable detect signal to Selector. The Figure 2.13 illustrates the UART connections on the EVM.

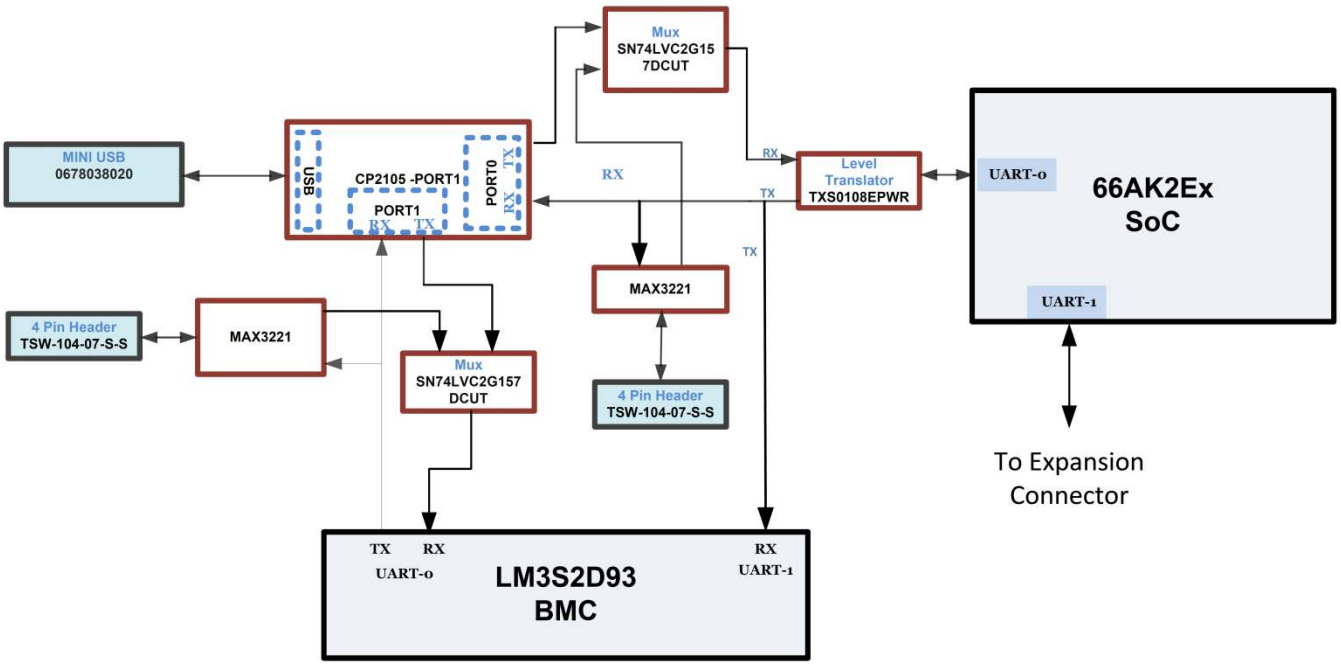

Figure 2.13: EVMK2E UART Connections

2.14 XFI Interface

The EVM provides connectivity for both XFI 10-Gigabit Ethernet ports on the EVM. For more information, see the Gigabit Ethernet (GbE) Switch Subsystem (10 GB) for Keystone II Devices User Guide (literature number SPRUHJ5) .These is shown in Figure 2.14 below

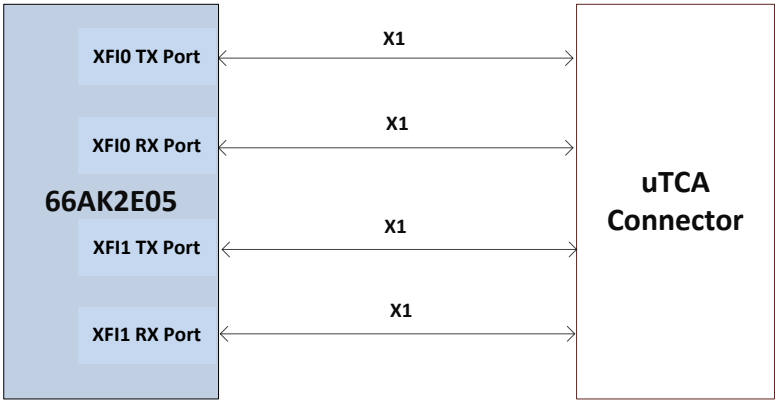

Figure 2.14: EVMK2E XFI Interface

2.15 Expansion Header

The EVM contains a 120-pin header (CN7) which has EMIF, I2C, TIMI [1:0], TIMO [0:1], SPI, GPIO [16:0] and UART signal connections. It should be noted that EMIF, I2C, TIMI [1:0], TIMO [0:1], and SPI, GPIO [16:0] connections to this header (CN3) are of 1.8V level whereas UART signals are of 3.3V level.

2.16 Universal Serial Bus 2.0/3.0(USB2.0/3.0)

The EVM supports new peripherals that have been added include the USB2.0/3.0 controller. There are total two USB ports (Port-0 and Port-1) available on SoC. Port-0 Supports USB2.0/3.0 Host mode and Port-1 supports USB2.0/3.0 Host mode or Device mode. Port-0 is routed on USB3.0 Type A connector and Port-1 is routed on USB3.0 micro AB connector. Both USB ports support data transfer at rates of 5.0 Gbps on the serial links. For more information, see the Universal Serial Bus 3 (USB3) for KeyStone II Devices User Guide (literature number SPRUHJ7).Below
Figure **2.15** shows USB connections between the SoC and USB3.0 connector.

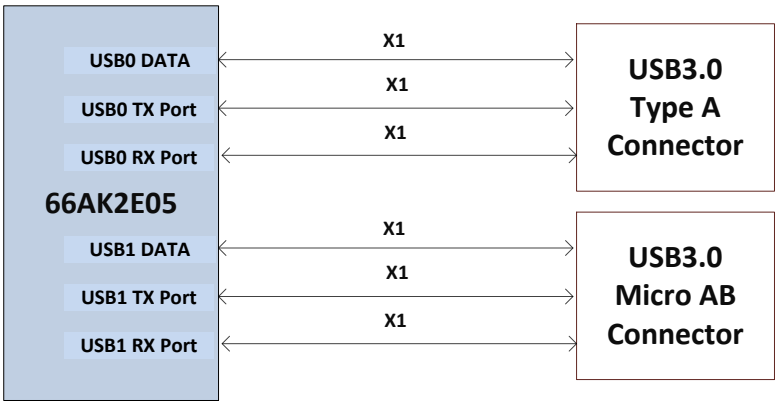

Figure 2.15: EVMK2E USB Interface

2.17 EVMK2E I2C implementation

Please refer below block diagram for the I2C implementation on EVMK2E.

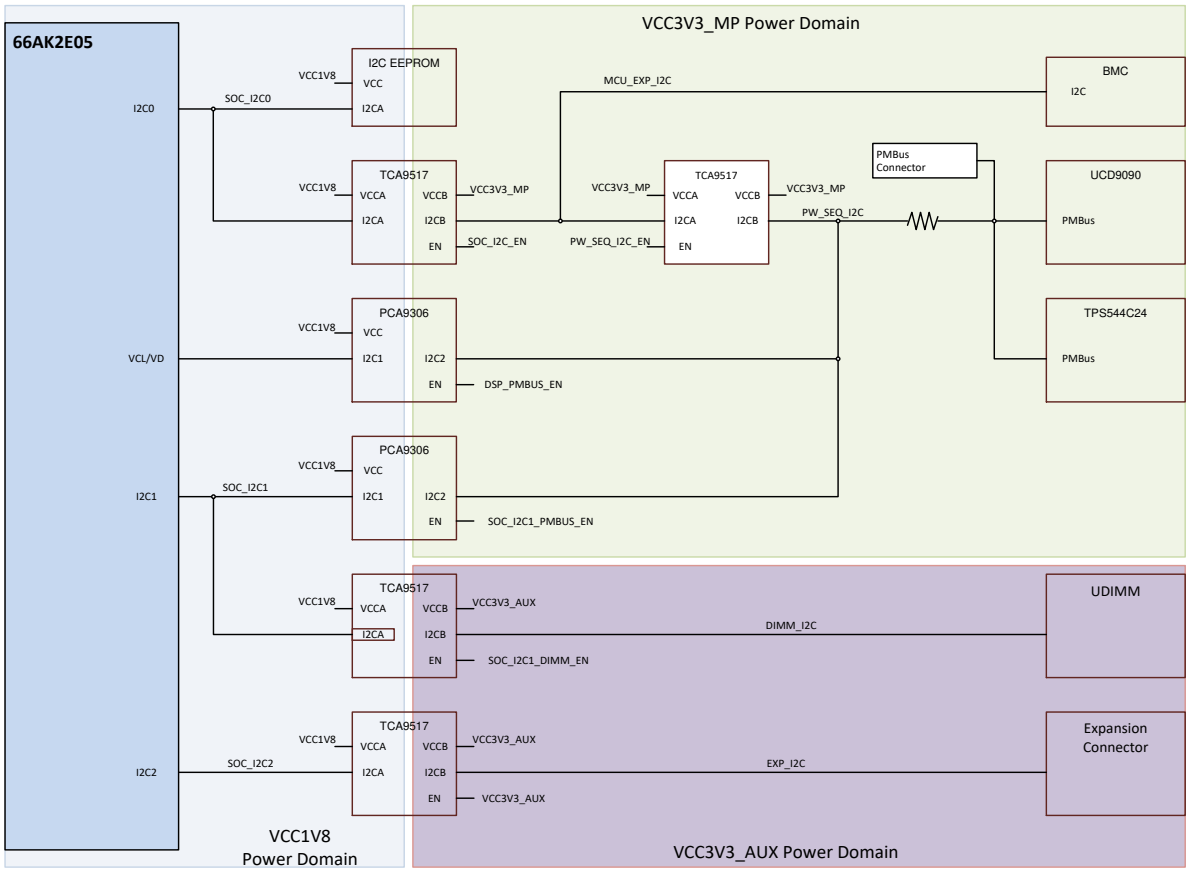

Figure 2.16: EVMK2E I2C interface

3. EVM Board Physical Specifications

This chapter describes the physical layout of the EVMK2E board and its connectors, switches and test points. It contains:

- Board Layout
- Connector Index
- Switches
- Test Points
- System LEDs
-

3.1 Board Layout

The EVM board dimension is 7.11” x 5.84” (180.6mm x 148.5mm). It is a 12-layer board and powered through connector J11.
Figure **3.1** and Figure 3.2 shows assembly layout of the EVM Board.

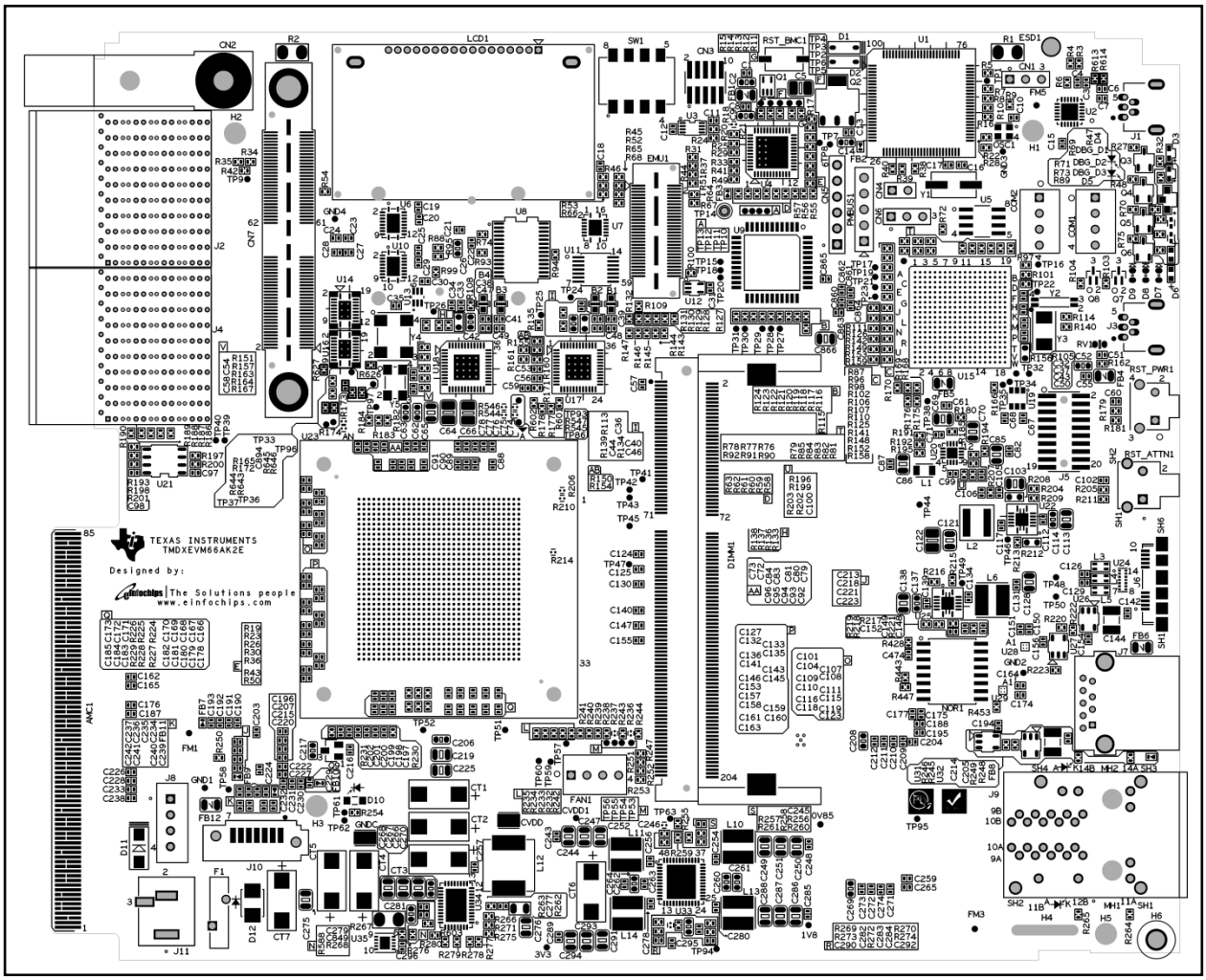

Figure 3.1: EVMK2E Board Assembly Layout – TOP view

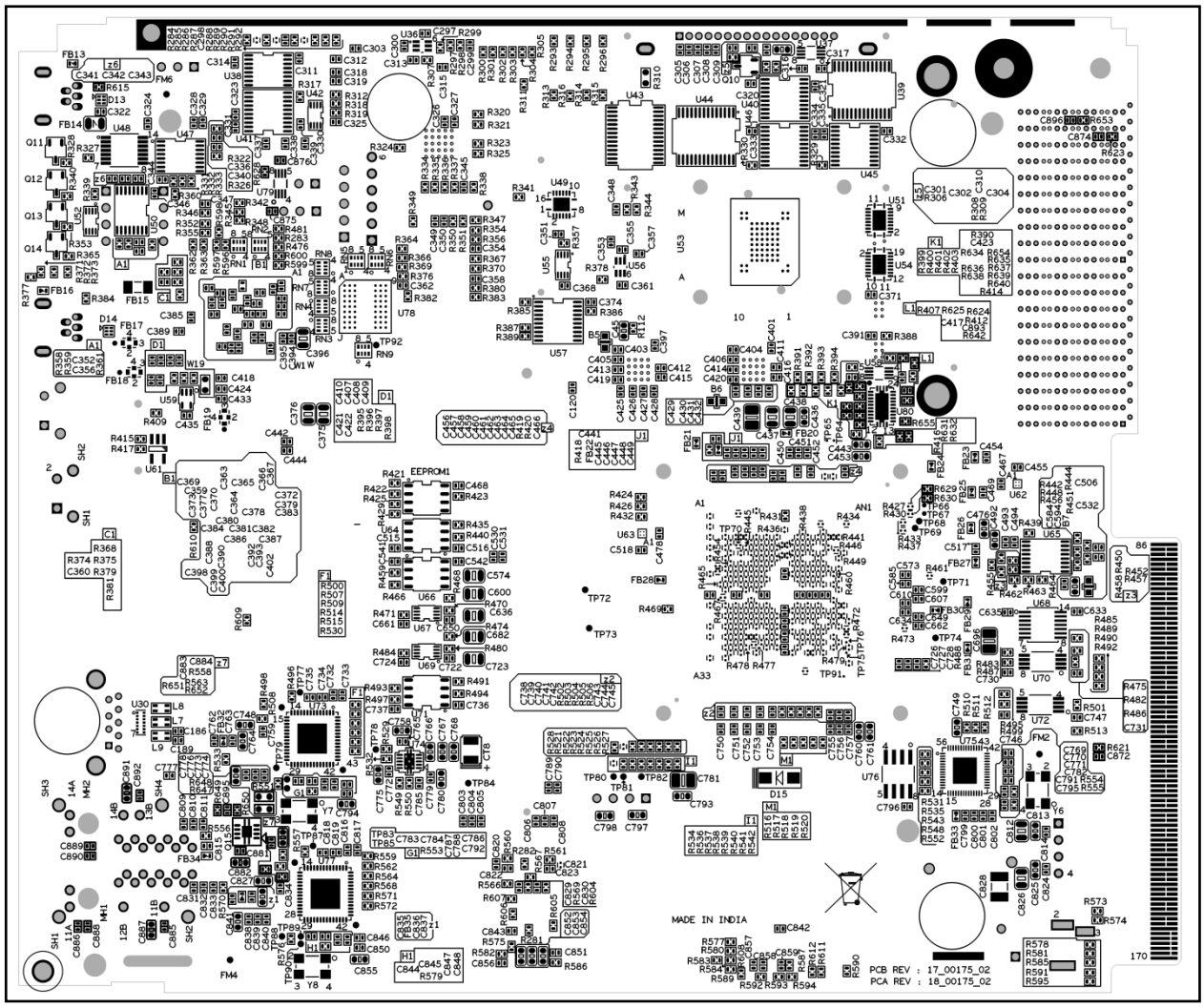

Figure 3.2: EVMK2E Board layout – Bottom view

3.2 Connector Index

The EVM Board has several connectors which provide access to various interfaces on the board.

Table 3.1: EVMK2E Board Connectors

Connector	Pins	Function
AMC1	170	AMC EDGE connector
CN1	3	BMC VBAT supply
CN7	120	Expansion Header (EMIF-16, SPI, GPIO, Timer I/O, I2C, and UART)
CN6	3	BMC wake up
CN4	2	BMC boot select
J9	32	Dual stacked Ethernet connector
CN3	10	BMC JTAG connector
DIMM1	204	DDR3 SODIMM connector
J11	3	DC power input jack connector
EMU1	60	MIPI 60-pin SoC JTAG connector
FAN1	4	FAN connector for +12Vdc fan
J1	5	Mini USB connector for CP2105
J2	160	uTCA.4 Edge Connector for Hyperlink SerDes
J4	160	uTCA.4 Edge Connector for XFI and SGMII
COM1 and COM2	4	UART 4-Pin connector
PMBUS1	5	PMBUS1 power Sequence control connected to UCD9090
J7	9	USB3.0 type A
J6	10	USB3.0 micro AB connector
J3	5	Mini USB connector for on board xds200 circuit

3.2.1 AMC1, AMC Edge Connector

The AMC card edge connector plugs into an AMC compatible carrier board and provides 2 PCIe lanes, 2 SGMII port, 1 SATA port, TSIP and system interfaces to the carrier board. This connector is the 170 pin B+ style. The signals on this connector are shown in the Table 3.2 below.

Table 3.2: AMC Edge Connector

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground Signal	170	GND	Ground Signal
2	VCC12	+12V Power	169	AMC_JTAG_TDI	JTAG Data In
3	PS1#	Presence 1	168	AMC_JTAG_TDO	JTAG Data Out
4	MP	Management Power	167	AMC_JTAG_RST#	JTAG Reset
5	GA0	Geographic Address 0	166	AMC_JTAG_TMS	JTAG TMS
6	RSVD	Reserved	165	AMC_JTAG_TCK	JTAG Clock
7	GND	Ground Signal	164	GND	Ground Signal
8	RSVD	Reserved	163	NC	
9	VCC12	+12V Power	162	NC	
10	GND	Ground Signal	161	GND	Ground Signal
11	AMC0_SGMII2_TX_DP	SGMII Port 2-TX	160	EXP_SCL2_3V3	I2C_CLK
12	AMC0_SGMII2_TX_DN	SGMII Port 2-TX	159	EXP_SDA2_3V3	I2C_DATA
13	GND	Ground Signal	158	GND	Ground Signal
14	AMC0_SGMII2_RX_DP	SGMII Port 2-TX	157	NC	
15	AMC0_SGMII2_RX_DN	SGMII Port 2-TX	156	NC	
16	GND	Ground Signal	155	GND	Ground Signal
17	GA1	Geographic Address 1	154	NC	
18	VCC12	+12V Power	153	NC	
19	GND	Ground Signal	152	GND	Ground Signal
20	AMC0_SGMII3_TX_DP	SGMII Port 3-TX	151	NC	
21	AMC0_SGMII3_TX_DN	SGMII Port 3-TX	150	NC	
19	GND	Ground Signal	149	GND	Ground Signal
23	AMC0_SGMII3_RX_DP	SGMII Port 3-TX	148	NC	
24	AMC0_SGMII3_RX_DN	SGMII Port 3-TX	147	NC	
25	GND	Ground Signal	146	GND	Ground Signal
26	GA2	Geographic Address 2	145	NC	
27	VCC12	+12V Power	144	NC	
28	GND	Ground Signal	143	GND	Ground Signal
29	AMC2_SATA0_TX_DP	Seaport 0- TX	142	NC	
30	AMC2_SATA0_TX_DN	SATA_Port 0- TX	141	NC	
31	GND	Ground Signal	140	GND	Ground Signal
32	AMC2_SATA0_RX_DP	SATA_Port 0- RX	139		
33	AMC2_SATA0_RX_DN	SATA_Port 0- RX	138		
34	GND	Ground Signal	137	GND	Ground Signal
35	NC		136	TCLKC_FS_P	Telecom Frame Sync
36	NC		135	TCLKC_FS_N	Telecom Frame Sync
37	GND	Ground Signal	134	GND	Ground Signal
38	NC		133	NC	
39	NC		132	NC	

40	GND	Ground Signal	131	GND	Ground Signal
41	ENABLE#	Enable Signal	130	PHY_MDIO_2V5	MDIO Data
42	VCC12	+12V Power	129	AMC_MDC_2V5	MDIO Clock
43	GND	Ground Signal	128	GND	Ground Signal
44	AMC4_PCIe0_TX0P	PCIe Port 0-TX	127	NC	
45	AMC4_PCIe0_TX0N	PCIe Port 0-TX	126	NC	
46	GND	Ground Signal	125	GND	Ground Signal
47	AMC4_PCIe0_RX0P	PCIe Port 0-RX	124	NC	
48	AMC4_PCIe0_RX0N	PCIe Port 0-RX	123	NC	
49	GND	Ground Signal	122	GND	Ground Signal
50	AMC4_PCIe0_TX1P	PCIe Port 1-TX	121	NC	
51	AMC4_PCIe0_TX1N	PCIe Port 1-TX	120	NC	
52	GND	Ground Signal	119	GND	Ground Signal
53	AMC4_PCIe0_RX1P	PCIe Port 1-RX	118	NC	
54	AMC4_PCIe0_RX1N	PCIe Port 1-RX	117	NC	
55	GND	Ground Signal	116	GND	Ground Signal
56	SMB_SCL_IPMBL		115	TSIP0_RX1_TX0	TSIP_RX0
57	VCC12	+12V Power	114	TSIP0_TX1_RX0	TSIP_TX1
58	GND	Ground Signal	113	GND	Ground Signal
59	NC		112	TSIP0_RX0_TX1	TSIP_RX0
60	NC		111	TSIP0_TX0_RX1	TSIP_TX0
61	GND	Ground Signal	110	GND	Ground Signal
62	NC		109	NC	
63	NC		108	NC	
64	GND	Ground Signal	107	GND	Ground Signal
65	NC		106	NC	
66	NC		105	NC	
67	GND	Ground Signal	104	GND	Ground Signal
68	NC		102	NC	
69	NC		101	NC	
70	GND	Ground Signal	101	GND	Ground Signal
71	SDA_IPMB		100	NC	
72	VCC12	+12V Power	99	NC	
73	GND	Ground Signal	98	GND	Ground Signal
74	TCLKA_P	Telecom Clock A	97	NC	
75	TCLKA_N	Telecom Clock A	96	NC	
76	GND	Ground Signal	95	GND	Ground Signal
77	TCLKB_P	Telecom Clock B	94	NC	
78	TCLKB_N	Telecom Clock B	93	NC	
79	GND	Ground Signal	92	GND	Ground Signal
80	PCIe_REF_CLK_P	PCIe Ref clock	91	NC	
81	PCIe_REF_CLK_N	PCIe Ref clock	90	NC	
82	GND	Ground Signal	89	GND	Ground Signal
83	PS0#	Presence 0	88	NC	
84	VCC12	+12V Power	87	NC	
85	GND	Ground Signal	86	GND	Ground Signal

3.2.2 CN1, BMC VBAT Supply

CN1 is 3-pin male connector for BMC Power source for the Hibernation module. It is normally connected to the positive terminal of a battery and serves as the battery backup/Hibernation module power-source supply. A jumper to pull up VCC3V3_MP is supplied with EVM to normal work.

Table 3.3: VBAT Supply Connector pin out

Pin #	Signal Name
1	VCC3V3_MP
2	VBAT
3	Ground

3.2.3 CN7, Expansion Header (EMIF-16, SPI, GPIO, Timer I/O, I2C, and UART)

CN7 is an expansion header for several interfaces on the SoC. They are 16-bit EMIF, SPI, GPIO, Timer, I2C, and UART. The signal connections to the test header are as shown in a Table 3.4 below:

Table 3.4: Expansion Connector pin out

Pin	Signal	Description	Pin	Signal	Description
1	VCC1V8	1.8V Supply	2	VCC1V8	1.8V Supply
3	GND	Ground	4	GND	Ground
5	EXP_SDA_3V3	SoC I2C data	6	SoC_EMIFA00	EMIF addr0
7	EXP_SCL_3V3	SoC I2C clock	8	SoC_EMIFA01	EMIF addr1
9	SoC_EMIFD0	EMIF data0	10	SoC_EMIFA02	EMIF addr2
11	SoC_EMIFD1	EMIF data1	12	SoC_EMIFA03	EMIF addr3
13	SoC_EMIFD2	EMIF data2	14	SoC_EMIFA04	EMIF addr4
15	SoC_EMIFD3	EMIF data3	16	SoC_EMIFA05	EMIF addr5
17	SoC_EMIFD4	EMIF data4	18	SoC_EMIFA06	EMIF addr6
19	SoC_EMIFD5	EMIF data5	20	SoC_EMIFA07	EMIF addr7
21	SoC_EMIFD6	EMIF data6	22	SoC_EMIFA08	EMIF addr8
23	SoC_EMIFD7	EMIF data7	24	SoC_EMIFA09	EMIF addr9
25	SoC_EMIFD8	EMIF data8	26	SoC_EMIFA10	EMIF addr10
27	SoC_EMIFD9	EMIF data9	28	SoC_EMIFA11	EMIF addr11
29	SoC_EMIFD10	EMIF data10	30	SoC_EMIFA12	EMIF addr12
31	SoC_EMIFD11	EMIF data11	32	SoC_EMIFA13	EMIF addr13
33	SoC_EMIFD12	EMIF data12	34	SoC_EMIFA14	EMIF addr14
35	SoC_EMIFD13	EMIF data13	36	SoC_EMIFA15	EMIF addr15
37	SoC_EMIFD14	EMIF data14	38	SoC_EMIFA16	EMIF addr16
39	SoC_EMIFD15	EMIF data15	40	SoC_EMIFA17	EMIF addr17
41	NC	Reserve	42	SoC_EMIFA18	EMIF addr18
43	SoC_EMIFCE1z	EMIF Space Enable1	44	SoC_EMIFA19	EMIF addr19
45	SoC_EMIFCE2z	EMIF Space Enable2	46	SoC_EMIFA20	EMIF addr20
47	SoC_EMIFCE3z	EMIF Space Enable3	48	SoC_EMIFA21	EMIF addr21
49	SoC_EMIFBE0z	EMIF Byte Enable0	50	SoC_EMIFA22	EMIF addr22
51	SoC_EMIFBE1z	EMIF Byte Enable1	52	SoC_EMIFA23	EMIF addr23
53	SoC_EMIFOEz	EMIF Output Enable	54	SoC_GPIO_00	SoC GPIO0
55	SoC_EMIFWEz	EMIF Write Enable	56	SoC_GPIO_01	SoC GPIO1
57	GND	Ground	58	GND	Ground
59	VCC5	5V Supply	60	VCC5	5V Supply

61	VCC3V3_AUX	3.3V Supply	62	VCC3V3_AUX	3.3V Supply
63	GND	Ground	64	GND	Ground
65	SoC_EMIFRNW	EMIF Read/Write	66	SoC_GPIO_02	SoC GPIO2
67	NC	Reserve	68	SoC_GPIO_03	SoC GPIO3
69	SoC_EMIFWAIT1	EMIF Wait	70	SoC_GPIO_04	SoC GPIO4
71	SoC_TIMO0	Timer input 0	72	SoC_GPIO_05	SoC GPIO5
73	EXP_TIMO0	Timer output 0	74	SoC_GPIO_06	SoC GPIO6
75	SoC_TIMO1	Timer input 1	76	SoC_GPIO_07	SoC GPIO7
77	EXP_TIMO1	Timer output 1	78	SoC_GPIO_08	SoC GPIO8
79	SoC_SSP2_MOSI	SPI data input	80	SoC_GPIO_09	SoC GPIO9
81	SoC_SSP2_MISO	SPI data output	82	SoC_GPIO_10	SoC GPIO10
83	SoC_SSP2_CS0	SPI chip select	84	SoC_GPIO_11	SoC GPIO11
85	SoC_SSP2_CS1	SPI chip select	86	SoC_GPIO_12	SoC GPIO12
87	SoC_SSP2_CS2	SPI chip select	88	SoC_GPIO_13	SoC GPIO13
89	SoC_SSP2_CS3	SPI chip select	90	SoC_GPIO_14	SoC GPIO14
91	SoC_SSP2_CLK	SPI clock	92	SoC_GPIO_15	SoC GPIO15
93	EXP_UART1_TXD_ 3V3	UART Serial Data Out (+3.3v)	94	SoC_GPIO_16	SoC GPIO16
95	EXP_UART1_RXD _3V3	UART Serial Data In (+3.3v)	96	EXP_TP0	Test point
97	SoC_UARTRTS	UART Request To	98	EXP_TP1	MCU Resetstatz
99	SoC_UARTCTS	UART Cear To Send (+3.3v)	100	EXP_TP2	EXT_PS#
101	TSRX_CLK0N	SerDes recovered clock for SyncE	102	BD_PRESENT	Board Present
103	TSRX_CLK0P	SerDes recovered clock for SyncE	104	BD_ID0	Board ID
105	TSRX_CLK1N	SerDes recovered clock for SyncE	106	BD_ID1	Board ID
107	TSRX_CLK1P	SerDes recovered clock for SyncE	108	BD_ID2	Board ID
109	TSPUSHEVt0_E	PPS push event from GPS for IEEE1588	110	RSV_CLKN	Output Clock
111	TSPUSHEVt1_E	Push event from BCN for IEEE1588	112	RSV_CLKP	Output Clock
113	TSCOMPOUT_E	IEEE1588 compare output.	114	TSPUSHEVt0	PPS push event from GPS for IEEE1588
115	TSSYNCEVT_E	IEEE1588 sync event output.	116	TSCOMPOUT_E	IEEE1588 compare output.
117	GND	Ground	118	GND	Ground
119	VCC3V3_AUX	3.3V Supply	120	VCC3V3_AUX	3.3V Supply

3.2.4 CN6, BMC wake up

CN6 is 3-pin male connector for BMC wake up from sleep mode. It is through jumper to enable. Normally is jumper to GND.

Table 3.5: BMC WAKE UP Connector pin out

Pin #	Signal Name
1	FUILL_RESETz
2	MCU_WAKEz
3	Ground

3.2.5 CN4, BMC Boot select

CN9 is 2-pin male connector for BMC boot select. It is through jumper to enable. Normally is jumper to GND.

Table 3.6: Boot select Connector pin out

Pin #	Signal Name
1	MCU_Bootselect
2	Ground

3.2.6 J9, Ethernet connector

J9 is double Gigabits RJ45 Ethernet connector with integrated magnetics. It is driven by Two Marvell Gigabit Ethernet transceiver 88E1514/12. The connections are shown in the Table 3.7 below:

Table 3.7: Ethernet Connector pin out

Pin #	Signal Name	Pin #	Signal Name
1A	PHY1_MDI0_N	1B	PHY2_MDI0_N
2A	PHY1_MDI0_P	2B	PHY2_MDI0_P
3A	PHY1_MDI1_N	3B	PHY2_MDI1_N
4A	PHY1_MDI1_P	4B	PHY2_MDI1_P
5A	PHY1_MDI2_N	5B	PHY2_MDI2_N
6A	PHY1_MDI2_P	6B	PHY2_MDI2_P
7A	PHY1_MDI3_N	7B	PHY2_MDI3_N
8A	PHY1_MDI3_P	8B	PHY2_MDI3_P
9A	Center Tap	9B	Center Tap
10A	GND	10B	GND
11A	Phy1_LED0+	11B	Phy2_LED0+
12A	Phy1_LED0-	12B	Phy2_LED0-
13A	Phy1_LED1+	13B	Phy2_LED1+
14A	Phy1_LED1-	14B	Phy2_LED1-
SH1	Shield1	SH3	Shield3
SH2	Shield2	SH4	Shield4

3.2.7 CN3, BMC JTAG Connector

CN3 is a 10-pin JTAG connector for ICDI (In Circuit Debug Interface) of BMC emulation. The pin out for the connector is shown in Table 3.8 below:

Table 3.8: BMC JTAG Connector pin out

Pin #	Signal Name	Pin #	Signal Name
1	VCC3V3_MP	2	BSC_JTAG_TMS
3	Ground	4	BSC_JTAG_TCK
5	Ground	6	BSC_JTAG_TDO
7	NC	8	BSC_JTAG_TDI
9	Ground	10	BSC_JTAG_SRSTN

3.2.8 DIMM1, DDR3 SO-DIMM Socket

DIMM1 is 204-pin DDR3 Socket type for external expansion. For compatibility, you can only use the DDR3 SO-DIMM of ECC type. If you use the general standard type will cause not compatible. ECC and non-ECC different pin definitions, please refer to the specification of the SO-DIMM module.

3.2.9 J11, DC Power Input Jack Connector

J11 is a DC Power-in Jack Connector for the stand-alone application of EVM. It is a 2.5mm power jack with positive center tip polarity. Do not use this connector if EVM is inserted into MicroTCA chassis or AMC carrier backplane.

Table 3.9: J11 Connector pin out

Pin #	Signal Name
1	+12V
2	Ground
3	Ground

3.2.10 EMU1, MIPI 60-Pin SoC JTAG Connector

EMU1 is a high speed system trace capable MIPI 60-pin JTAG connector for XDS200 type of SoC emulation. The on board switch multiplexes this interface with external type emulator through AMC edge. Whenever an external emulator is plugged into EMU1, the external emulator connection will be switched to the SoC. The I/O voltage level on these pins is 1.8V. So any 1.8 V level compatible emulators can be used to interface with the SoC. It should be noted that when an external emulator is plugged into this connector (EMU1), from AMC edge type emulation circuitry will be disconnected from the SoC. when on board emulators and AMC emulates present then SoC give on board emulators as first priority. The pin out for the connector is shown in Table 3.10 below:

Table 3.10: SoC JTAG Connector pin out

Pin #	Signal Name	Pin #	Signal Name
1	TVD (+1.8V)	2	TMS
3	TCLK	4	TDO
5	TDI	6	TRGRST#
7	TCLKRTN	8	EMU_TRST#
9	nTRST(NC)	10	NC
11	NC	12	TVD
13	EMU2	14	TRC_CLK1(NC)
15	TDIS	16	Ground
17	EMU3	18	EMU21
19	EMU0	20	EMU22
21	EMU1	22	EMU23
23	EMU4	24	EMU24
25	EMU5	26	EMU25
27	EMU6	28	EMU26
29	EMU7	30	EMU27
31	EMU8	32	EMU28
33	EMU9	34	EMU29
35	EMU10	36	EMU30
37	EMU11	38	EMU31
39	EMU12	40	EMU32
41	EMU13	42	EMU33
43	EMU14	44	NC
45	EMU15	46	NC
47	EMU16	48	NC
49	EMU17	50	NC
51	EMU18	52	NC
53	EMU19	54	NC
55	EMU20	56	NC
57	Ground	58	EXT_EMU_DET
59	TRC_CLK(NC)	60	NC

3.2.11 FAN1, FAN Connector

The EVM incorporates a dedicated cooling fan. This fan has the capability of easily being removed when the EVM is inserted into an AMC backplane which uses forced air cooling.

The fan selected provides maximum cooling (CFM) and operates on 12Vdc. FAN1 will be connected to provide 12Vdc to the fan.

Table 3.11: FAN1 Connector pin out

Pin #	Signal Name
1	GND
2	+12Vdc
3	NC
4	FAN_PWM

3.2.12 J1, Mini-USB Connector for CP2105

J1 is a 5-pin Mini-USB connector to connect Code Composer Studio with SoC using UART Console type on-board emulation circuitry. Below Table 3.12 shows the pin outs of the Mini-USB connector.

Table 3.12: Mini USB Connector pin out

Pin #	Signal Name
1	VBUS
2	USB D-
3	USB D+
4	Ground
5	Ground

3.2.13 J4, uTCA.4 Edge Connector for Hyperlink SerDes

J4 is a ZD3 Plus connector. The RTM edge connector plugs into an RTM compatible carrier board and provides one Hyperlink Group and system interfaces to the carrier board. This connector is the 160 pin style. The signals on this connector are shown in the Table 3.13 below:

Table 3.13: uTCA.4 Connector pin out

Pin	Signal	Description	Pin	Signal	Description
GB1	GND	Ground	B4	HYPERLINK0_RXN0	HyperLink0 receive data
GB2	GND	Ground	B6	HYPERLINK0_RXN1	
GB3	GND	Ground	B8	HYPERLINK0_RXN2	
GB4	GND	Ground	B10	HYPERLINK0_RXN3	
GB5	GND	Ground	A4	HYPERLINK0_RXP0	
GB6	GND	Ground	A6	HYPERLINK0_RXP1	
GB7	GND	Ground	A8	HYPERLINK0_RXP2	
GB8	GND	Ground	A10	HYPERLINK0_RXP3	
GB9	GND	Ground	C3	HYPERLINK0_RXFLCLK	HyperLink0 sideband signals
GB10	GND	Ground	D3	HYPERLINK0_RXFLDAT	
GD1	GND	Ground	C5	HYPERLINK0_RXPMCLK	
GD2	GND	Ground	D5	HYPERLINK0_RXPMDAT	
GD3	GND	Ground	C4	HYPERLINK0_TXFLCLK	
GD4	GND	Ground	C6	HYPERLINK0_TXPMCLK	
GD5	GND	Ground	D6	HYPERLINK0_TXPMDAT	
GD6	GND	Ground	D4	HYPERLINK0_TXFLDAT	
GD7	GND	Ground	B3	HYPERLINK0_TXN0	HyperLink0 transmit data
GD8	GND	Ground	B5	HYPERLINK0_TXN1	
GD9	GND	Ground	B7	HYPERLINK0_TXN2	
GD10	GND	Ground	B9	HYPERLINK0_TXN3	
GF1	GND	Ground	A3	HYPERLINK0_TXP0	
GF2	GND	Ground	A5	HYPERLINK0_TXP1	
GF3	GND	Ground	A7	HYPERLINK0_TXP2	
GF4	GND	Ground	A9	HYPERLINK0_TXP3	
GF5	GND	Ground	G3	NC	
GF6	GND	Ground	H3	NC	
GF7	GND	Ground	G4	NC	
GF8	GND	Ground	H4	NC	
GF9	GND	Ground	G5	NC	
GF10	GND	Ground	H5	NC	
GH1	GND	Ground	G6	NC	
GH2	GND	Ground	H6	NC	
GH3	GND	Ground	G7	NC	
GH4	GND	Ground	H7	NC	
GH5	GND	Ground	G8	NC	
GH6	GND	Ground	H8	NC	
GH7	GND	Ground	E10	NC	
GH8	GND	Ground	E3	NC	
GH9	GND	Ground	F3	NC	

Pin	Signal	Description	Pin	Signal	Description
GH10	GND	Ground	E4	NC	
GA1	GND	Ground	E6	NC	
GA2	GND	Ground	E7	NC	
GA3	GND	Ground	F6	NC	
GA4	GND	Ground	E9	NC	
GA5	GND	Ground	F8	NC	
GA6	GND	Ground	F9	NC	
GA7	GND	Ground	C8	NC	
GA8	GND	Ground	C9	NC	
GA9	GND	Ground	C7	NC	
GA10	GND	Ground	D8	NC	
GC1	GND	Ground	F10	NC	
GC2	GND	Ground	C10	NC	
GC3	GND	Ground	F7	NC	
GC4	GND	Ground	D9	NC	
GC5	GND	Ground	F4	NC	
GC6	GND	Ground	E5	NC	
GC7	GND	Ground	D10	NC	
GC8	GND	Ground	F5	NC	
GC9	GND	Ground	E8	NC	
GC10	GND	Ground	D7	NC	
GE1	GND	Ground	E2	NC	
GE2	GND	Ground	F2	NC	
GE3	GND	Ground	C2	NC	
GE4	GND	Ground	E1	NC	
GE5	GND	Ground	F1	NC	
GE6	GND	Ground	H9	NC	
GE7	GND	Ground	G10	NC	
GE8	GND	Ground	H10	NC	
GE9	GND	Ground	G9	NC	
GE10	GND	Ground	G1	NC	
GG1	GND	Ground	H1	NC	
GG2	GND	Ground	G2	NC	
GG3	GND	Ground	H2	NC	
GG4	GND	Ground	D2	SOC_SCL_RTM	I2C SCL
GG5	GND	Ground	D1	SOC_SDA_RTM	I2C SDA
GG6	GND	Ground	C1	URTM_PS#_R	PS#

Pin	Signal	Description	Pin	Signal	Description
GG7	GND	Ground	A1	VCC12	RTM PWR (12V)
GG8	GND	Ground	B1	VCC12	
GG9	GND	Ground	A2	VCC12	
GG10	GND	Ground	B2	VCC12	

3.2.14 J2, uTCA.4 Edge Connector for XFI and SGMII

J2 is a ZD3 Plus connector. The RTM edge connector plugs into an RTM compatible carrier board and provides 2 XFI port and 4 SGMII Ports to the carrier board. This connector is the 160 pin style. The signals on this connector are shown in the Table 3.14 below:

Table 3.14: uTCA.4 Connector pin out

Pin	Signal	Description	Pin	Signal	Description
GB1	GND	Ground	G1	NC	
GB2	GND	Ground	H1	NC	
GB3	GND	Ground	G2	NC	
GB4	GND	Ground	H2	NC	
GB5	GND	Ground	G3	NC	
GB6	GND	Ground	H3	NC	
GB7	GND	Ground	G4	NC	
GB8	GND	Ground	H4	NC	
GB9	GND	Ground	G5	NC	
GB10	GND	Ground	H5	NC	
GD1	GND	Ground	G6	NC	
GD2	GND	Ground	H6	NC	
GD3	GND	Ground	G7	NC	
GD4	GND	Ground	H7	NC	
GD5	GND	Ground	G8	NC	
GD6	GND	Ground	H8	NC	
GD7	GND	Ground	C8	NC	
GD8	GND	Ground	F1	NC	
GD9	GND	Ground	C5	NC	
GD10	GND	Ground	F4	NC	
GF1	GND	Ground	F3	NC	
GF2	GND	Ground	E1	NC	
GF3	GND	Ground	C7	NC	
GF4	GND	Ground	D6	NC	
GF5	GND	Ground	D7	NC	
GF6	GND	Ground	F5	NC	

Pin	Signal	Description	Pin	Signal	Description
GF7	GND	Ground	F8	NC	
GF8	GND	Ground	F6	NC	
GF9	GND	Ground	E4	NC	
GF10	GND	Ground	E5	NC	
GH1	GND	Ground	D8	NC	
GH2	GND	Ground	E2	NC	
GH3	GND	Ground	F2	NC	
GH4	GND	Ground	F7	NC	
GH5	GND	Ground	D5	NC	
GH6	GND	Ground	E8	NC	
GH7	GND	Ground	E3	NC	
GH8	GND	Ground	E7	NC	
GH9	GND	Ground	C6	NC	
GH10	GND	Ground	E6	NC	
GA1	GND	Ground	A10	NC	
GA2	GND	Ground	B10	NC	
GA3	GND	Ground	C10	NC	
GA4	GND	Ground	D10	NC	
GA5	GND	Ground	F9	NC	
GA6	GND	Ground	E10	NC	
GA7	GND	Ground	F10	NC	
GA8	GND	Ground	E9	NC	
GA9	GND	Ground	H9	NC	
GA10	GND	Ground	G9	NC	
GC1	GND	Ground	G10	NC	
GC2	GND	Ground	H10	NC	
GC3	GND	Ground	A9	PHY_MDIO_2V5	SGMII MDIO Data
GC4	GND	Ground	B9	RTM_MDC_2V5	SGMII MDIO CLK
GC5	GND	Ground	B2	UTCA_SGMII4_RX_DN	SGMII4 receive data
GC6	GND	Ground	A2	UTCA_SGMII4_RX_DP	
GC7	GND	Ground	B1	UTCA_SGMII4_TX_DN	SGMII4 transmit data
GC8	GND	Ground	A1	UTCA_SGMII4_TX_DP	
GC9	GND	Ground	B4	UTCA_SGMII5_RX_DN	SGMII5 receive data
GC10	GND	Ground	A4	UTCA_SGMII5_RX_DP	
GE1	GND	Ground	B3	UTCA_SGMII5_TX_DN	SGMII5 transmit data
GE2	GND	Ground	A3	UTCA_SGMII5_TX_DP	
GE3	GND	Ground	B6	UTCA_SGMII6_RX_DN	SGMII6 receive data
GE4	GND	Ground	A6	UTCA_SGMII6_RX_DP	
GE5	GND	Ground	B5	UTCA_SGMII6_TX_DN	SGMII6 transmit data
GE6	GND	Ground	A5	UTCA_SGMII6_TX_DP	

Pin	Signal	Description	Pin	Signal	Description
GE7	GND	Ground	B8	UTCA_SGMII7_RX_DN	SGMII7 receive data
GE8	GND	Ground	A8	UTCA_SGMII7_RX_DP	
GE9	GND	Ground	B7	UTCA_SGMII7_TX_DN	SGMII7 transmit data
GE10	GND	Ground	A7	UTCA_SGMII7_TX_DP	
GG1	GND	Ground	D2	SOC_XFI_RX_DN0	XGMII receive data
GG2	GND	Ground	D4	SOC_XFI_RX_DN1	
GG3	GND	Ground	C2	SOC_XFI_RX_DP0	
GG4	GND	Ground	C4	SOC_XFI_RX_DP1	
GG5	GND	Ground	D1	SOC_XFI_TX_DN0	XGMII transmit data
GG6	GND	Ground	D3	SOC_XFI_TX_DN1	
GG7	GND	Ground	C1	SOC_XFI_TX_DP0	
GG8	GND	Ground	C3	SOC_XFI_TX_DP1	
GG9	GND	Ground	D9	EXP_XFI_MDC_2V5	XFI Clock Signal
GG10	GND	Ground	C9	EXP_XFI_MDIO_2V5	XFI MDIO Signal

BMC and SoC have 4-pin male connector for RS232 serial interface. A 4-Pin female to 9-Pin DTE female cable is supplied with EVM to connect with the PC.

Table 3.15: UART Connector pin out

Pin #	Signal Name
1	Detect
2	Ground
3	Transmit
4	Receiver

3.2.15 PMBUS1, PMBUS Connector for Smart-Reflex and sequence Control

The SoC core power and peripheral power is supplied by Sequence control UCD9090 and TPS544C24 and Quad switcher IC LM26430. PMBUS1 provides a connection between UCD9090 and remote connection during development. Through the USB to GPIO pod provided by TI, the user can trace and configure the parameters in TPS544C24 and LM26430 with the Smart-Fusion GUI. The pin out of PMBUS1 is shown in below Table 3.16.

Table 3.16: PMBUS Connector Pin Out

Pin #	Signal Name
1	PMBUS_CLK
2	PMBUS_DAT
3	PMBUS_ALT
4	PMBUS_CTL
5	Gnd

3.2.16 J7 Port-0, USB3.0 Type A Connector

J7 is a 9-pin USB3 type A connector for the USB3.0 (SoC Port 0) interface The pin out for the connector is shown in the Table 3.17 below:

Table 3.17: Type A USB Connector Pin Out

Pin #	Signal Name
1	VBUS
2	D-
3	D+
4	GND
5	SSRX-
6	SSRX+
7	GND
8	SSTX-
9	SSTX+

3.2.17 J6 Port-1, USB3.0 Micro AB Connector

J6 is a 10-pin USB3.0 Micro AB connector for the USB3.0 (SoC Port 1) interface The pin out for the connector is shown in the Table 3.18 below:

Table 3.18: Micro AB USB Connector Pin Out

Pin #	Signal Name
1	VBUS
2	D-
3	D+
4	ID
5	GND
6	SSTX-
7	SSTX+
8	GND
9	SSRX-
10	SSRX+

3.2.18 J3, Mini USB Connector for XDS200 on board emulator

J3 is a 5 pin Mini-USB connector to connect Code Composer Studio with EVM DSP using XDS200 type on-board emulation circuitry. Below Table 3.19 shows the pin out of Mini-USB connector.

Table 3.19: Mini-USB Connector pin out

Pin #	Signal Name
1	VBUS
2	D-
3	D+
4	ID (NC)
5	Ground

3.2.19 J5, XDS200 MCU JTAG Connector

J5 is the 20-pin JTAG connector for debugging of XDS200 processor (AM1802BZWTD3). The pin outs for this Connector is shown in below Table 3.20:

Table 3.20: Mini-USB Connector pin out

Pin #	Signal Name	Pin #	Signal Name
1	DBG_TMS	2	DBG_TRSTn
3	DBG_TDI	4	Ground
5	EMU_TVD	6	NC
7	DBG_TDO	8	Ground
9	DBG_RTCK	10	Ground
11	DBG_TCK	12	Ground
13	NC	14	NC
15	DBG_SRST	16	NC
17	NC	18	NC
19	NC	20	NC

3.3 DIP and Pushbutton Switches

The EVM has 3 push button switches, one Jumper header and one sliding actuator DIP switches. The PRW, ATT and MCU_RESET are push button switches; CN6 is Jumper header while SW1 are DIP switches. The function of each of the switches is listed in the Table 3.21 below:

Table 3.21: EVMK2E Board Switches

Switch	Function
PWR	Full Reset Event
MCU_RESET	MCU Reset Event
ATT	Warm Reset Event
CN6	MCU Wake Evant
SW1	SoC Boot mode Configuration

3.3.1 PWR, Full Reset

Pressing the PWR button performs different functions based on how many times the button was pressed. The button must be pressed again within 0.5 seconds for it to register as a sequential click.

1 press: Graceful Shutdown

2 presses: Warm Reset

3 presses: Full Reset

4 presses: Cancel action

If the button is pressed and held for longer than 3 seconds, the board will be forcefully shutdown.

3.3.2 MCU_RESET, BMC Reset

Pressing the MCU_RESET button switch will issue RST # to the BMC. It will reset BMC and other peripherals. This switch act as global reset switch for board.

3.3.3 ATT, Warm Reset

Not currently implemented.

3.3.4 CN6, Wake

The button is reserved for future use.

3.3.5 SW1, SoC Boot mode Configurations

SW1 are 4-position DIP switches, which are used for selecting the boot mode. Please refer to the SoC Data Manual to get more details about the SoC Boot modes and their configuration, the diagram of the DSP no-boot setting on these switches is shown below:

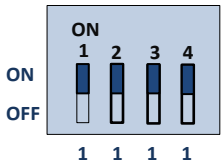

Figure 3.3: SW1 default settings

Note: Switch at ON position should be considered as '1' and OFF as '0'.

The following Table 3.22 describes the positions and corresponding function on SW1.

Table 3.22: SW1, DSP Boot Mode Selection Switch

DIP Switch settings	Selected bootmode
0000	ARM NAND
0001	DSP No Boot
0010	ARM SPI
0011	ARM I2C Master
0100	ARM UART Master
0101	ARM RBL EthNet
0110	Sleep with Max pll & ARM Bypass
0111	Sleep with Max pll
1000	DSP NAND
1001	SLEEP W/ SLOW PLL & ARM BYPASS
1010	DSP SPI-boot
1011	ARM I2C Master
1100	DSP UART boot
1101	DSP RBL ENET
1110	SLEEP W/ SLOW PLL & SLOW ARM PLL
1111	DSP No-Boot

3.4 Test Points

The EVM Board has 107 test points. The position of each test point is shown in the Figure 3.4 and Figure **3.5** below.

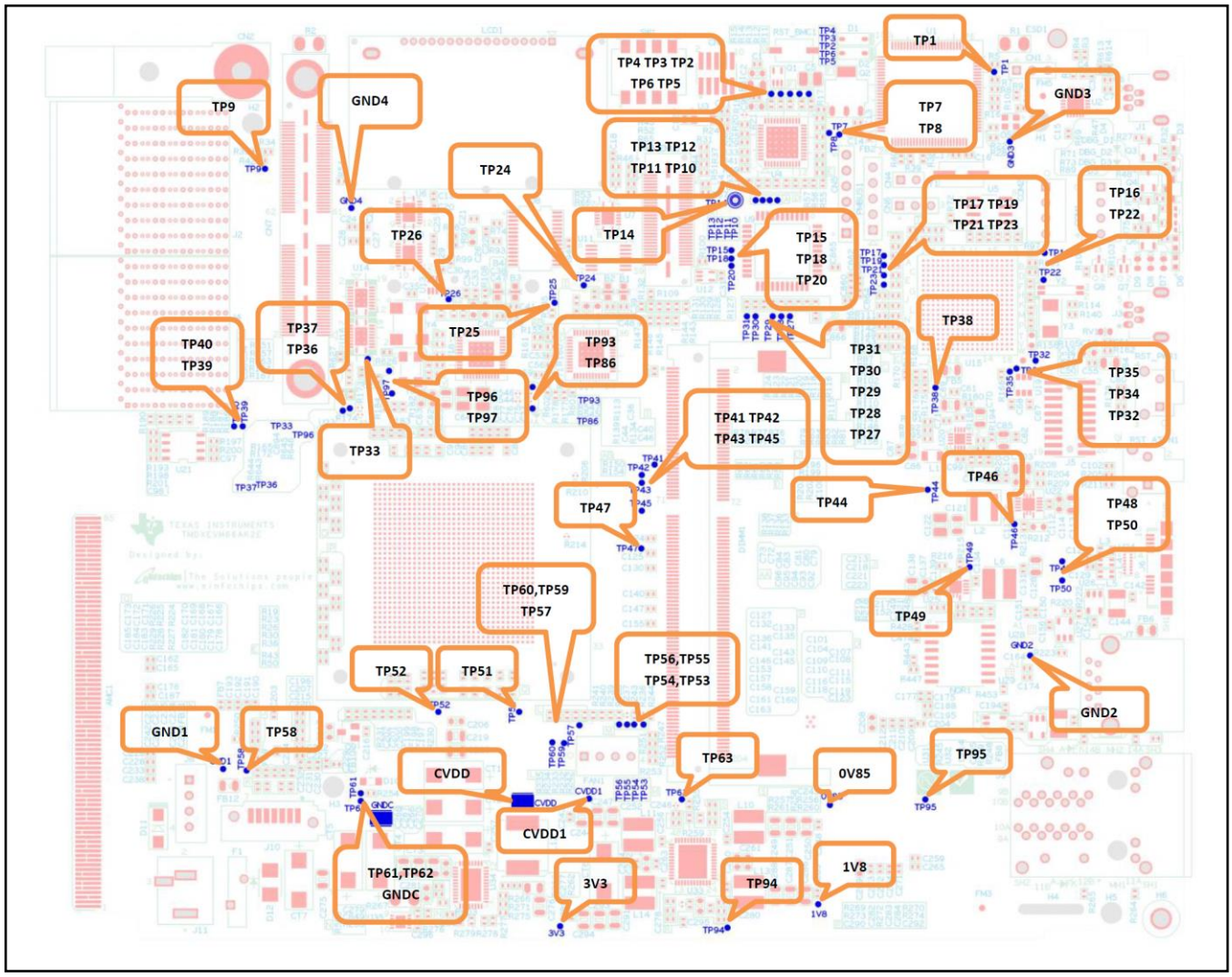

Figure 3.4: Board Test Points (Top)

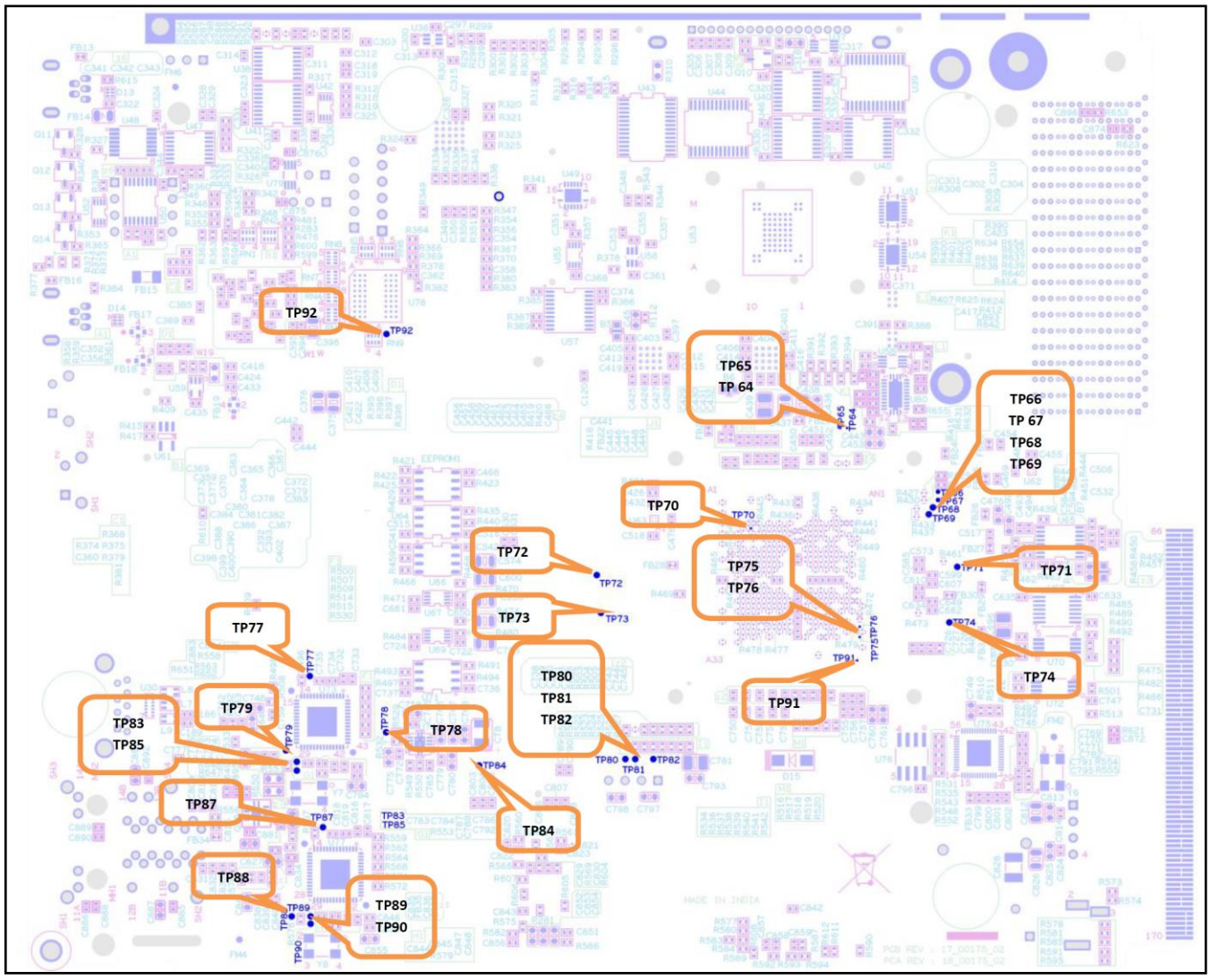

Figure 3.5: Board Test Points (Bottom)

Table 3.23: EVMK2E Board Test Points

Test Point	Signal
GNDC	Test point for GND
CVDD	Test point for CVDD supply
TP1	Test point for BMC UART1 TX Pin(MCU_U1TX)
GND1	Test point for GND
CVDD1	Test point for CVDD1 supply
TP2	Reserved for UCD9090 JTAG pin 29 (JTAG_TDI)
GND2	Test point for GND
TP3	Reserved for UCD9090 JTAG pin 30 (JTAG_TMS)
GND3	Test point for GND
TP4	Reserved for UCD9090 JTAG pin 31 (JTAG_TRST)
GND4	Test point for GND
TP5	Reserved for UCD9090 JTAG pin 27 (JTAG_TCK)
TP6	Reserved for UCD9090 JTAG pin 28 (JTAG_TDO)
TP7	Test point for GND
TP8	Test point for VCC3V3_MP_ALT supply
TP9	Reserved for expansion header pin96 (EXP_TP0)
TP10	Test point for XDS_VCC3V3 supply
TP11	Test point for XDS200 JTAG pin CPLD_TDI
TP12	Test point for XDS200 JTAG pin CPLD_TMS
TP13	Test point for XDS200 JTAG pin CPLD_TCK
TP15	Reserved for U9 pin 18 (uTDIS)
TP16	Reserved for U15 pin F16.
TP17	Reserved for U15 pin C5.
TP18	Reserved for U9 pin 19 (SPARE1)
1V8	Test point for VCC1V8 supply
TP19	Reserved for U15 pin C3.
TP20	Reserved for U9 pin 20 (SPARE0)
TP21	Reserved for U15 pin D4.
TP22	Reserved for U15 pin F17.
TP23	Reserved for U15 pin E5.
TP24	Test point for GND
TP25	Test point for U17 (CDCM6208) pin 45 (STATUS1/PIN0)
TP26	Test point for U18 (CDCM6208) pin 45 (STATUS1/PIN0)
TP27	Reserved for U9 pin 29 (uEXP0)
TP28	Reserved for U9 pin 28 (uEXP1)
TP29	Reserved for U9 pin 27 (uEXP2)
TP30	Test point for XDS200 JTAG pin CPLD_TDO
TP31	Reserved for U9 pin 23 (uEXP3)
TP32	Reserved for U15 pin T19 .

Test Point	Signal
TP33	Reserved for SoC SYSCLKOUT
3V3	Test point for VCC3V3_AUX supply
TP34	Reserved for U15 pin T18
TP35	Reserved for U15 pin T17
TP36	Reserved
TP37	Reserved
TP38	Test point for GND
TP39	Test point for VDD33 supply
TP40	Test point for GND
TP41	Test point for GND
TP42	Reserved
TP43	Reserved
TP44	Test point for VCC1V5 supply
TP45	Test point for VPP1V8 supply
TP46	Reserved for U22 pin 14 (PWRGD)
TP47	Reserved
TP48	Test point for GND
TP49	Reserved for U25 pin 14 (PWRGD)
TP50	Test point for VCC5V supply
TP51	Test point for CVDD supply
TP52	Test point for GND
TP53	Reserved
TP54	Reserved for SoC USIMIO
TP55	Reserved
TP56	Reserved for SoC USIMCLK
TP57	Reserved for SoC SPI0SCS3
TP58	Test point for U75(88SE9182 IC)
TP59	Reserved for SoC SPI0SCS2
TP60	Reserved for SoC SPI0SCS1
TP61	Test point for VCC12 supply
TP62	Test point for GND
TP63	Reserved for U33 (LM26430) pin 44 (CLK_OUT)
TP68	Reserved
TP69	Reserved
TP71	Reserved
TP72	Reserved
TP73	Reserved
TP74	Reserved
TP77	Reserved for U73 (88E1514) pin 9 (CLK125)
TP78	Reserved for U74 pin 9 (PGOOD)

Test Point	Signal
TP79	Reserved for U73 (88E1514) pin 29 (TSTPT)
TP80	Reserved
TP81	Reserved
TP82	Reserved for SoC USIMRST
TP83	Reserved for U73 (88E1514) pin 31 (HSDAC_N)
TP84	Test point for VCC0V75 supply
TP85	Reserved for U73 (88E1514) pin 32 (HSDAC_P)
0V85	Test point for VCC0V85 supply
TP86	Reserved for U34 pin 31 (VDDCMON)
TP87	Reserved for U77 (88E1514) pin 9 (CLK125)
TP88	Reserved for U77 (88E1514) pin 29 (TSTPT)
TP89	Reserved for U77 (88E1514) pin 31 (HSDAC_N)
TP90	Reserved for U77 (88E1514) pin 32 (HSDAC_P)
TP92	Reserved for U15 pin D13
TP93	Reserved for U34 pin 32 (VSSCMON)
TP94	Reserved for U33 (LM26430) pin 23 (CE)
TP95	Test point for VCC2V5 supply
TP96	Test point for SOC_SGMII_MDC signal
TP97	Test point for SOC_XFIMDC signal
TP14	Test point for GND
TP64	Reserved
TP65	Reserved
TP70	Reserved
TP75	Reserved
TP76	Reserved
TP91	Test point for SOC_TCK signal
TP66	Reserved
TP67	Reserved

3.5 System LEDs

The EVM board has seven LEDs. Their positions on the board are indicated in Figure 3.6. The description of each LED is listed in Table 3.24 below:

Table 3.24: EVMK2E Board LEDs

LED#	Color	Description
D3	Red	Failure and Out of service status in AMC chassis
D4	Blue	Hot Swap status in AMC chassis
Dbg_D1	Red	SoC Dual colors Debug LEDs.
	Green	
Dbg_D2	Blue	SoC Debug LEDs.
Dbg_D3	Blue	SoC Debug LEDs.
D5	Red	SoC RESETSTATZ
D6	Green	PLLLOCK LED

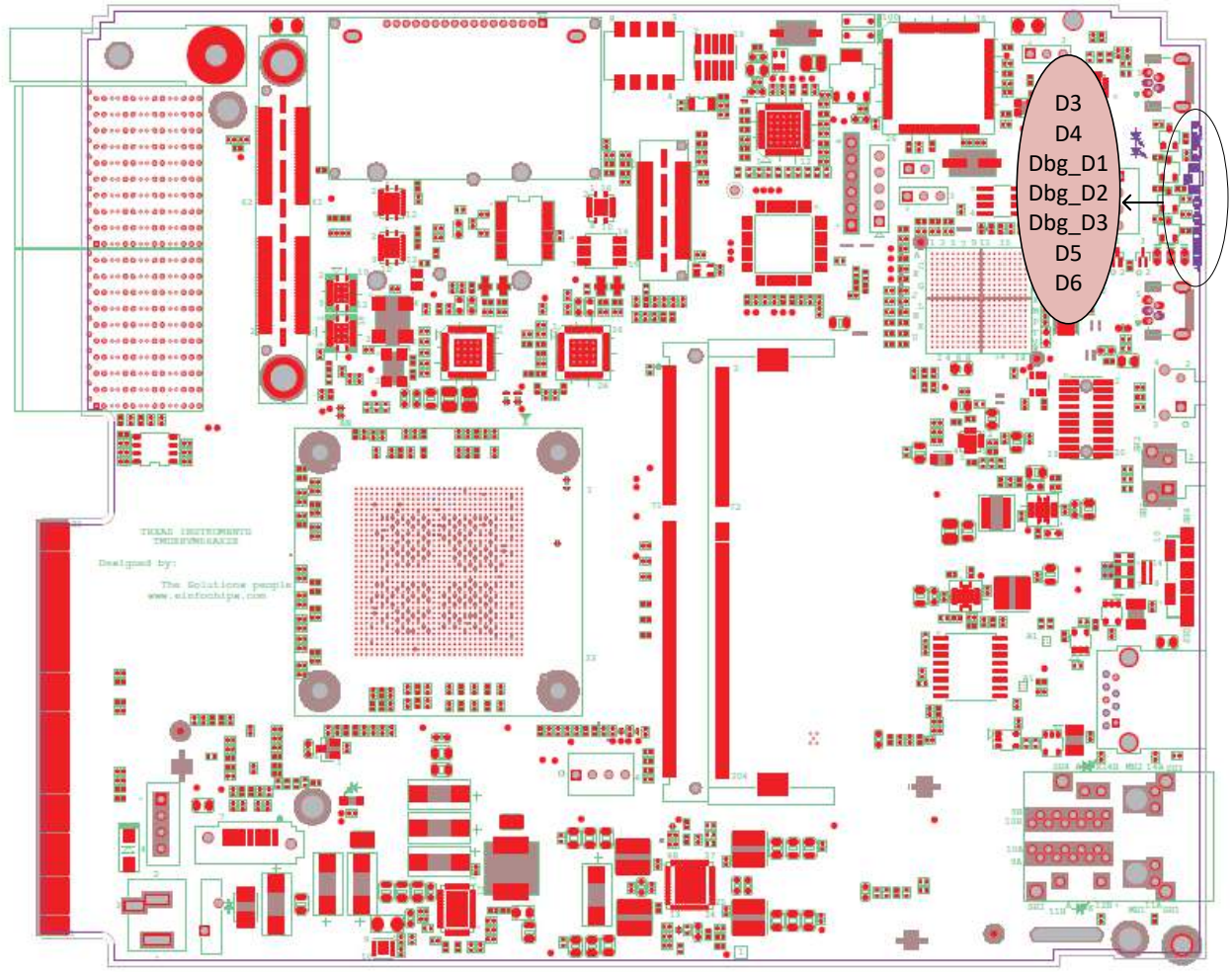

Figure 3.6: Board LEDs

4. System Power Requirements

This chapter describes the power design of the EVM board. It contains:

- Power Requirements
- Power Supply Distribution
- Power Supply Boot Sequence

4.1 Power Requirements

Note that the power estimates stated in this section are maximum limits used in the design of the EVM. They have margin added to allow the EVM to support early silicon samples that normally have higher power consumption than eventual production units. Please use power estimation tool for proper power budgeting of your application.

The maximum EVM power requirements (including 5% margin) are estimated to be:

- EVM BMC – 0.448W
- SoC Cooling Fans – 1.2W (+12Vdc/0.1A)
- Clock Generators & clock sources – 1.98W
- SoC – 20.31W [worse case]
  Core supplies: 16W
  Peripheral supplies: 4.31W
- DDR3 – 3.58W
  1 SO-DIMM to support 72-bit with ECC of the SoC
- NOR Flash – 0.036W
- NAND Flash – 0.072W
- Misc – 0.66W
- SGMII PHY – 1.46W
- LCD Display – 0.135W
- XDS200 circuitry – 0.680W
- UART to USB Converter – 0.148W
- USB3.0 connector – 4.500W
- Power Sequence Circuit – 0.198W
- EVM board total: 60W

Total EVM Board Consumption is 60W approx. Hence, the selected AC/DC 12V adapter should be rated for a minimum of 60 Watts.

Table 4.1: Current Consumption on Each Voltage Rail

Device	Net Name	Voltage	Current	Qty	Power Usage		Description
Input	3.3V_MP_AMC	+3.30V					MMC Management Power
	VCC12	+12.00V					Payload Power to AMC
Management	VCC3V3_AUX	+3.30V					3.3V Power Rail
66AK2E05	CVDD	+1.00V	16.00A	1	16.0W	20.31W	DSP Core Power
	CVDD1	+0.95V	1.800A	1	1.71W		ARM Fixed Core Power
	VCC1V8	+1.80V	1.0A	1	1.8W		DSP I/O Power
	VCC1V5	+1.50V	0.80A	1	1.2W		DSP DDR3 & SERDES Power
	VCC0V85	+0.85V	1.2A	1	1.0W		
DDR3 Memory	VCC1V5	+1.50V	2.088A	1	3.13W	3.58W	DDR3 SODIMM Power
	VCC0V75	+0.75V	0.60A	1	0.45W		DDR3 Termination Power
NAND Flash	VCC1V8	+1.80V	0.1A	1	0.18W	0.18W	NAND Flash Power
NOR Flash	VCC1V8	+1.80V	0.020A	1	0.03W	0.03W	SPI NOR Flash Power
CDCM6208	VCC3V3_AUX	+3.30V	0.600A	2	1.98W	1.98W	Clock Gen Power
PHY (88E1514)	VCC2V5	+2.50V	0.08A	1	0.08W	1.46W	PHY Analog & I/O Power
	VCC3V3	+3.30V	1.37A	1	1.37W		PHY Core Power
CP2105	VCC3V3_AUX	+3.30V	0.200A	1	0.66W	0.66W	USB to dual UART controller
BMC	VCC3V3_ALT	+3.30V	0.136A	1	0.448W	0.448W	BMC +3.3V I/O Power
Misc. Logic	VCC3V3_AUX	+3.30V	0.100A	1	0.33W	0.66W	Translator & Logic Power
	VCC1V8	+1.80V	0.100A	1	0.18W		Translator & Logic Power
	VCC1V5_AUX	+1.50V	0.100A	1	0.15W		Translator & Logic Power

4.2 Power Supply Distribution

A high-level block diagram of the power supplies is shown in Figure 4.1. It is also shown in the schematic. In Figure 4.1 the Auxiliary power rails are always on after payload power is supplied. These regulators support all control, sequencing, and boot logic. The Auxiliary Power rails contain:

- VCC3V3_AUX
- VCC3V3_MP

The maximum allowable power is 60W from the external AC brick supply or from the 8 AMC header pins 4 uTCA.4 connector pins.

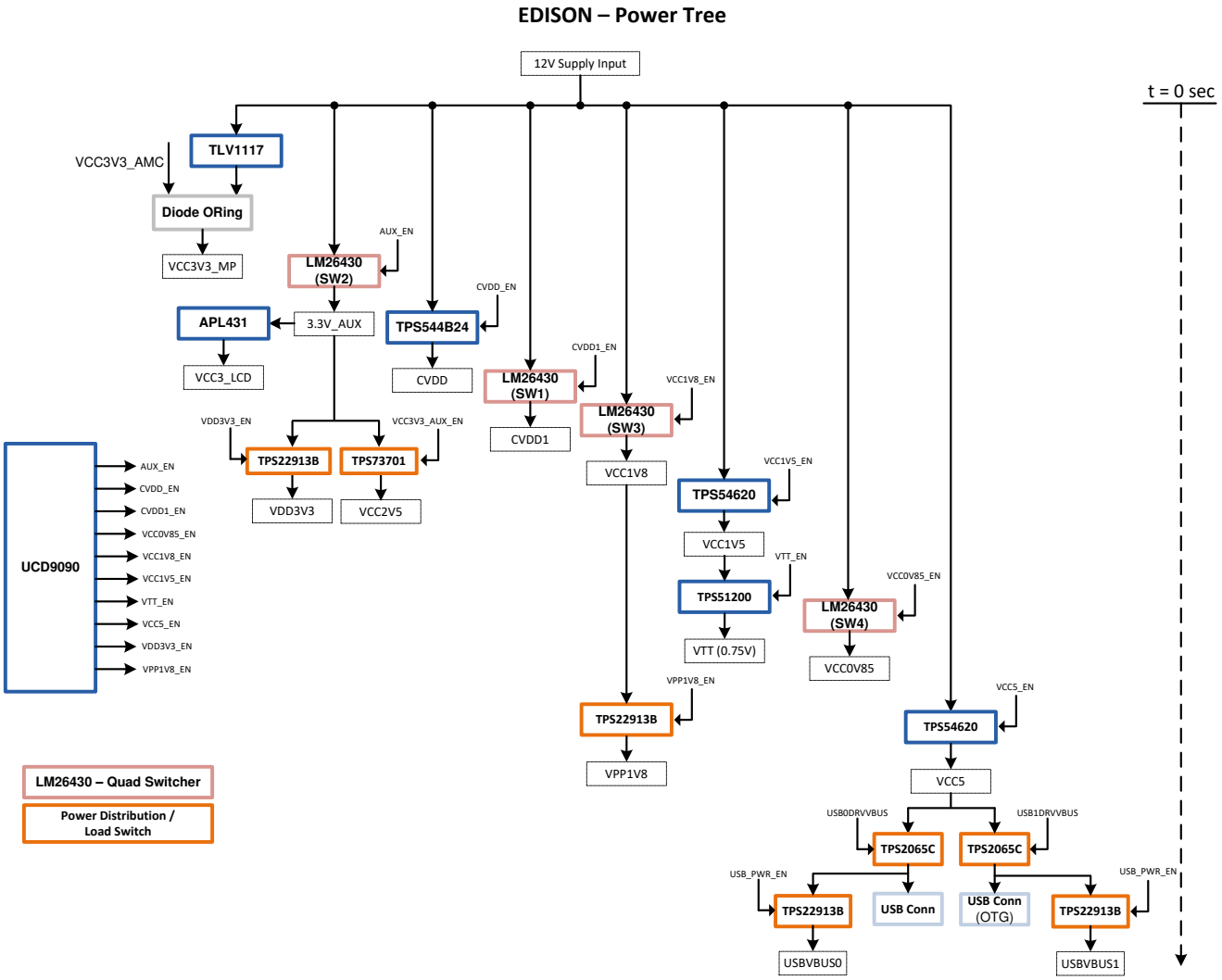

Figure 4.1: EVM Power Generation Topology

Individual control for each (remaining) voltage regulator is provided to allow flexibility in how the power planes are sequenced (Refer to section 4.3 for specific details). The goal of all power supply designs is to support the ambient temperature range of 0°C to 60°C.

The SoC core power is supplied using dedicated high current switching regulator i.e. Top Avatar TPS544C24. This regulator can supply up to 30A load. The output voltage is controlled by point of load controller, Smart reflex enabled, VID supported regulator LM10011. The 66AK2E05 supports a VID interface to enable Smart-Reflex® power supply control for its primary core logic supply. Other SoC supply voltages are provided through other TI switching regulators.

The EVM power topology is a combination of switching supplies and linear supplies. The linear supplies are used to save space for small loads. The switching supplies are implemented for larger loads. The switching supplies are listed below followed by explanations of critical component selection:

- CVDD (AVS core power for 66AK2EX)
- CVDD1 (0.95V fixed core power for 66AK2EX)
- VCC0V85(0.85V power for 66AK2EX)
- VCC1V8(1.8V power for 66AK2EX)
- VCC3V3_AUX (3.3V power for peripherals)
- VCC1V5 (1.5V DDR3 power for 66AK2EX and DDR3 SODIMM Module)
- VCC5 (5.0V power for the USB3.0 connector)

4.2.1 CVDD Design

The variable core power supply rail "**CVDD"** is regulated by "point of load controller" LM10011. The LM10011 is Connected with 66Ak2E05's VID interface through which voltage can be controlled by SoC.

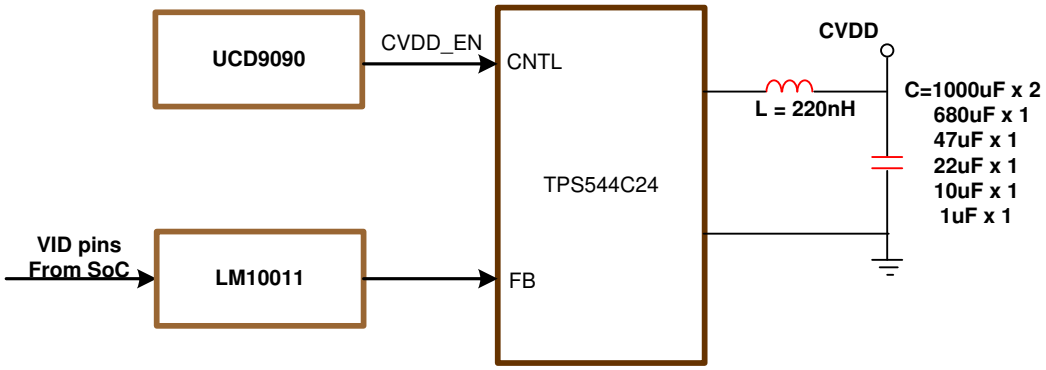

Figure 4.2: CVDD on EVMK2E

CVDD Inductor Calculation	**CVDD Capacitor Calculation**
$L = ((V_{in(max)} - V_{out})/\Delta I_{out}) * V_{out}/(V_{in(max)} * F_{sw})$ = ((12.5 - 1)/(8) * (1 / (12.5 * 1MHz)) = (11.5/8) * (1 / (12.5M)) = (1.4375) * (0.08u) ≈ 115nH Reference Inductor = 220nH	$C = (\Delta Iout^2 * L) / (Vout * \Delta Vout)$ = (10^2 * 220nH) / (1*10m) = 22000n / 10m = 2200 uF Total Caps connected = 2760uF

4.2.2 VCC5 Design

The VCC5 power rail is regulated by TI 6A Synchronous Step Down SWIFT™ Converters, TPS54620, to supply the power of the USB3.0 connector on EVM.

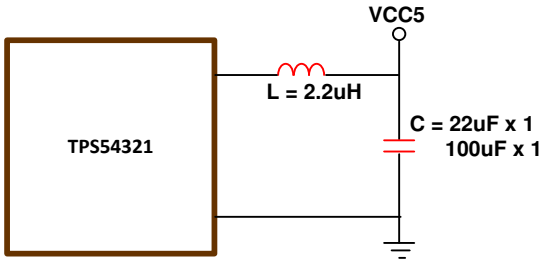

Figure 4.3: VCC5 Power Design on EVMK2E

Output Capacitor Calculation	**Inductor Calculation**
$C_{out(min)} = (2*\Delta I_{out}) / (F_{sw}*\Delta V_{out})$ $= (2*1)/(900kHz*0.25)$ $\approx 9uF$ Reference Capacitor = 22uF + 100uF	L = (Vin - Vout)/(Iout * Kind) *(Vout / (Vin * Fsw)) = (12 - 1.5)/(3 * 0.3) * (5 / (12 * 900KHz)) = 7.78 * 0.46u = ~ 3.6uH Reference Inductor = 2.2uH

4.2.3 VCC1V5 Design

The VCC1V5 power rail is regulated by TI 6A Synchronous Step Down SWIFT™ Converters, TPS54620, to supply the power of the SoC DDR3 controller and DDR3 SODIMM module on EVM.

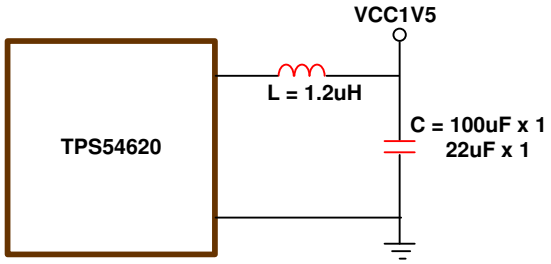

Figure 4.4: VCC1V5 Power Design on EVMK2E

Output Capacitor Calculation	**Inductor Calculation**
$C_{out(min)} = (2*\Delta I_{out}) / (F_{sw}*\Delta V_{out})$ $= (2*1)/(700kHz*0.125)$ $\approx 38uF$ Reference Capacitor = 100uF + 22uF	$L = ((V_{in(max)} - V_{out})/(I_{out} * K_{ind})) * (V_{out}/(V_{in(max)} * F_{sw}))$ = (12 - 1.5)/(4.5 * 0.3) * (1.5 / (12 * 700KHz)) = 7.78 * 0.18u = ~ 1.38uH Reference Inductor = 1.2uH

4.3 Power Supply Boot Sequence

Specific power supply and clock timing sequences are identified below. The 66AK2EX DSP requires specific power up and power down sequencing. Figure 4.5 and Figure 4.6 illustrate the proper boot up and down sequence. Table 4.2 provides specific timing details for Figure 4.5 and Figure 4.6.

Refer to 66AK2EX data manual for confirmation of specific sequencing and timing requirements.

Table 4.2: Power-up and down timing on EVMK2E

Step	Power Rails	Timing	Description
	Power-Up		
1	VCC12 (AMC Payload power), VCC3V3_MP_ALT, VCC3_LCD	Auto	When the 12V power is supplied to the EVM, the VCC3V3_MP supplies to the MCU and UCD9090 power will turn on. The 3V supplies to the LCD power will Turn on.
2	VCC3V3_AUX,,VCC2V5	0ms	VCC3V3_AUX and VCC2V5 would be turned on first
3	CVDD (SoC AVS core power)	15ms	Enable CVDD (UCD9090 power rail#1) After 3.3V AUX is stable for 15ms.
4	CVDD1 (SoC CVDD1 fixed core power)	5ms	Enable CVDD1 (UCD9090 power rail#2) 5ms after CVDD has stabilized.
5	VCC1V8	5ms	Turn on VCC1V8 (UCD9090 power rail#3) After CVDD1 is stable for 5ms.
6	VCC1V5 (DDR3 power)	5ms	Turn on VCC1V5 (UCD9090 power rail#4) After VCC1V8 is stable for 5ms.
7	VCC0V75	5ms	Turn on VCC0V75 (UCD9090 power rail#5) After VCC1V5 is stable for 5ms.
8	VCC0V85	5ms	Turn on VCC0V85 (UCD9090 power rail#6) After VCC0V75 is stable for 5ms.
9	VDD3V3	5ms	Turn on VDD3V3 (UCD9090 power rail#7) After VCC0V85 is stable for 5ms.
10	VCC5V	5ms	Turn on VCC5V (UCD9090 power rail#8) After VDD3V3 is stable for 5ms.
11	CDCM6208#1/#2 Initialization BMC Output	5ms	Initialize the CDCE6208s after VCC5 Stable for 5mS. De-assert CDCM6208 power down pins (PD#), initialize the CDCM6208s.
12	RESETz Other reset and NMI pins	1ms	De-asserted RESETz and unlock other reset and NMI pins for the SoC after SOC_Power_GOOD stable and CDCE6208s PLLs locked for 5mS. In the meanwhile, the MCU will driving the boot Configurations to the SoC GPIO pins.
	PORz		De-asserts PORz after RESETz is deasserted for 5ms.
	RESETFULLz		De-asserts RESETFULLz after PORz is de-asserted for 5ms.

	Power-Down		
13	RESETFULLz PORz	0ms	If there is a power failure or AMC payload is powered off, BMC will assert RESETFULLz and PORz signals to SoC.
14	BMC 3.3V outputs CDCM6208 PD# pins	5ms	Locked 3.3V output pins on the BMC and pull the CDCM6208 PD# pins to low to disable SoC clocks.
15	VCC3V3_AUX VCC2V5 CVDD CVDD1 VCC1V8 VCC1V5 VCC0V75 VCC0V85 VDD3V3 VCC5	0ms	Turns off all main power rails.

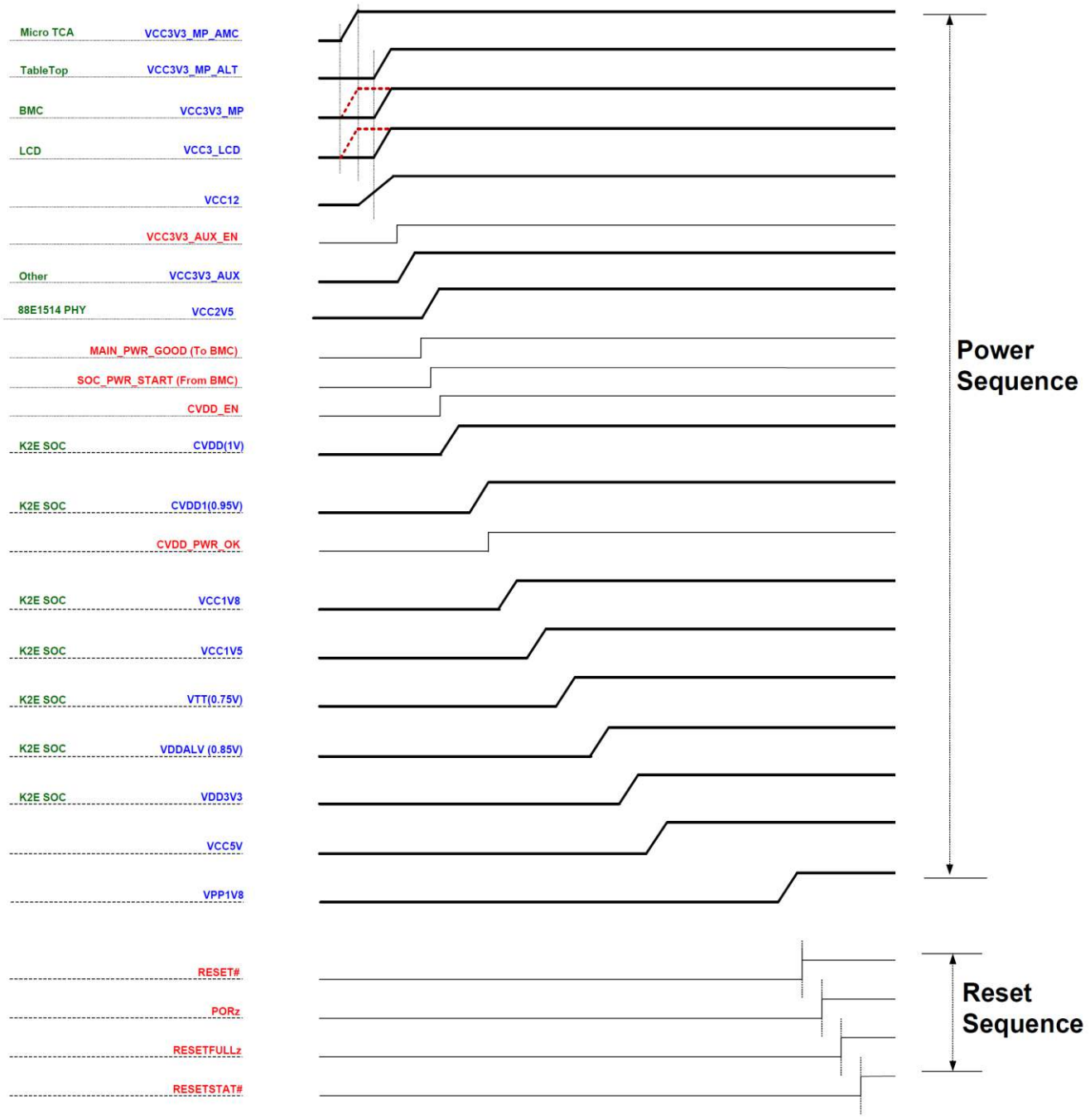

Figure 4.5: Initial Power up Sequence Timing Diagram

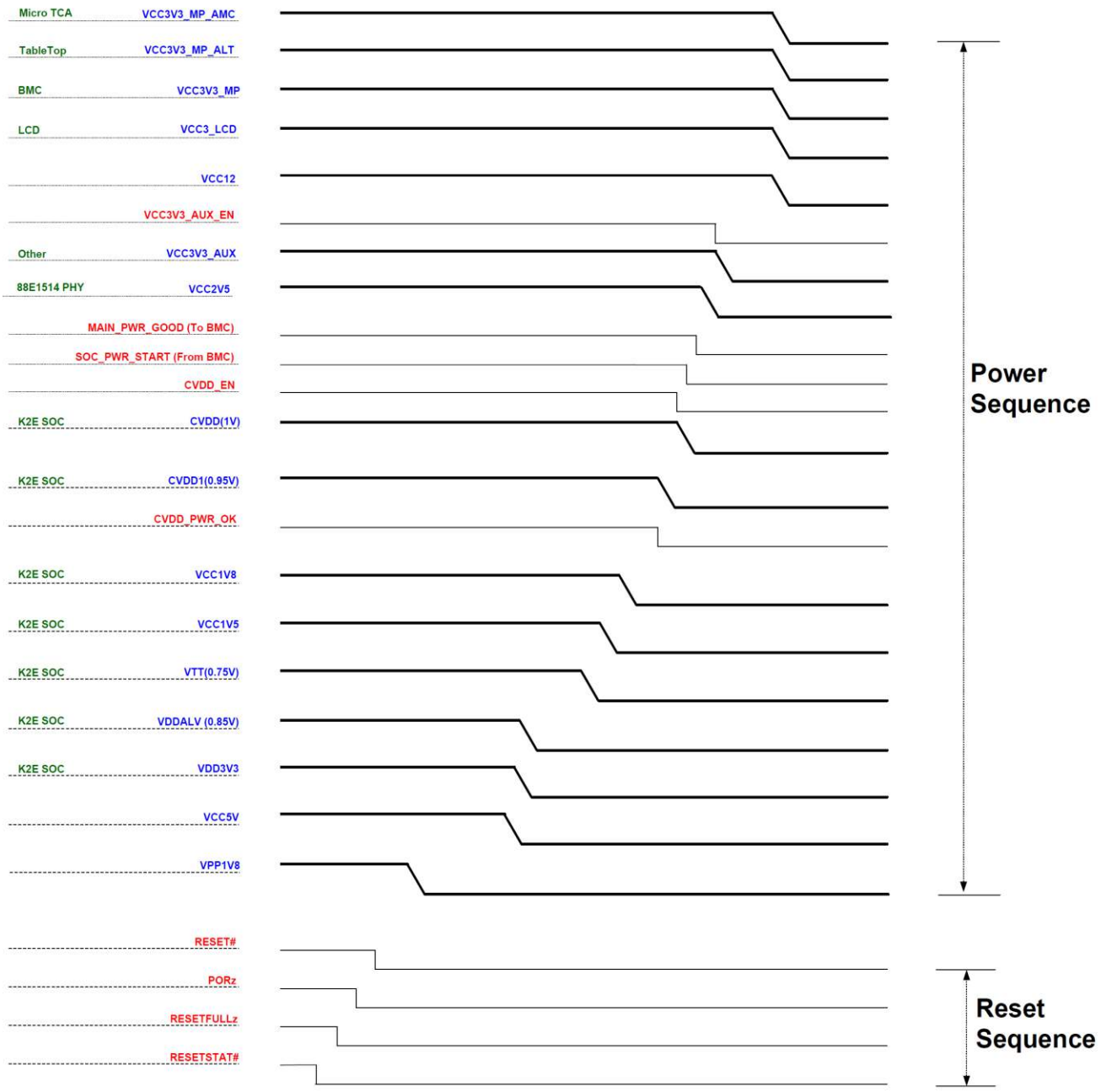

Figure 4.6: Power down Sequence Timing Diagram

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
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西新宿三井ビル

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

   6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

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7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

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