TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74LCX00F,TC74LCX00FN,TC74LCX00FT,TC74LCX00FK

#### Low-Voltage Quad 2-Input NAND Gate with 5-V Tolerant Inputs and Outputs

The TC74LCX00 is a high-performance CMOS 2-input NAND gate. Designed for use in 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

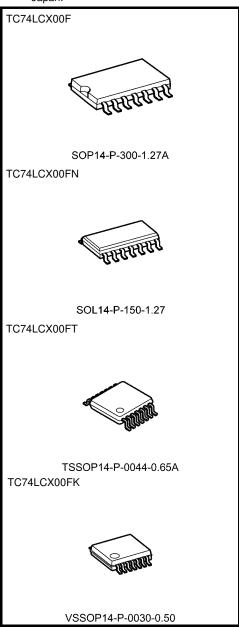
The device is designed for low-voltage (3.3 V) VCC applications, but it could be used to interface to 5 V supply environment for inputs.

All inputs are equipped with protection circuits against static discharge.

#### **Features**

- Low-voltage operation: VCC = 2.0 to 3.6 V
- High-speed operation:  $t_{pd} = 5.2 \text{ ns (max) (V}_{CC} = 3.0 \text{ to } 3.6 \text{ V)}$
- Output current:  $|I_{OH}|/I_{OL} = 24 \text{ mA (min)} (V_{CC} = 3.0 \text{ V})$
- Latch-up performance: -500 mA
- Available in JEDEC SOP, JEITA SOP, TSSOP and VSSOP (US)
- Power-down protection provided on all inputs and outputs
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 00 type

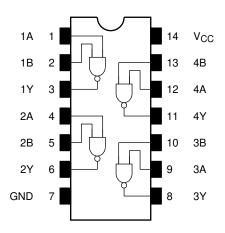
Note: xxxFN (JEDEC SOP) is not available in Japan.



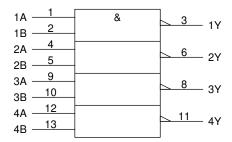
Weight

SOP14-P-300-1.27A : 0.18 g (typ.) SOL14-P-150-1.27 : 0.12 g (typ.) TSSOP14-P-0044-0.65A : 0.06 g (typ.) VSSOP14-P-0030-0.50 : 0.02 g (typ.)

#### Pin Assignment (top view)



#### **IEC Logic Symbol**



#### **Truth Table**

Inp	uts	Outputs
Α	В	Y
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	L

### **Absolute Maximum Ratings (Note 1)**

Characteristics	Symbol	Rating	Unit	
Power supply voltage	V <sub>CC</sub>	-0.5 to 7.0	V	
DC input voltage	V <sub>IN</sub>	-0.5 to 7.0	V	
		-0.5 to 7.0 (Note 2)		
DC output voltage	V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> + 0.5 (Note 3)	V	
Input diode current	lik	-50	mA	
Output diode current	lok	±50 (Note 4)	mA	
DC output current	I <sub>OUT</sub>	±50	mA	
Power dissipation	P <sub>D</sub>	180	mW	
DC V <sub>CC</sub> /ground current	I <sub>CC</sub> /I <sub>GND</sub>	±100	mA	
Storage temperature	T <sub>stg</sub>	-65 to 150	°C	

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2:  $V_{CC} = 0 V$ 

Note 3: High or low state. IOUT absolute maximum rating must be observed.

Note 4:  $V_{OUT} < GND, V_{OUT} > V_{CC}$ 



## **Operating Ranges (Note 1)**

Characteristics	Symbol	Rating	Unit
Power supply voltage	V <sub>CC</sub>	2.0 to 3.6	V
Fower supply voltage	V CC	1.5 to 3.6 (Note 2)	V
Input voltage	V <sub>IN</sub>	0 to 5.5	V
Output voltage	V <sub>OUT</sub>	0 to 5.5 (Note 3)	V
Output voltage	<b>V</b> OU1	0 to V <sub>CC</sub> (Note 4)	V
Output ourront	I <sub>OH</sub> /I <sub>OL</sub>	±24 (Note 5)	mA
Output current	IOH/IOL	±12 (Note 6)	ША
Operating temperature	T <sub>opr</sub>	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 7)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs must be tied to either VCC or GND.

Note 2: Data retention only

Note 3:  $V_{CC} = 0 V$ 

Note 4: High or low state

Note 5:  $V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$ 

Note 6:  $V_{CC} = 2.7 \text{ to } 3.0 \text{ V}$ 

Note 7:  $V_{IN} = 0.8$  to 2.0 V,  $V_{CC} = 3.0$  V

#### **Electrical Characteristics**

#### DC Characteristics ( $Ta = -40 \text{ to } 85^{\circ}\text{C}$ )

Characteri	stics	Symbol	Test Condition		V <sub>CC</sub> (V)	Min	Max	Unit
	H-level	V <sub>IH</sub>				2.0		
Input voltage	L-level	VIL			2.7 to 3.6 2.7 to 3.6		0.8	V
	L-level	VIL		_	2.7 10 3.0		0.0	
			$I_{OH} = -100 \mu A$	2.7 to 3.6	V <sub>CC</sub> - 0.2	_		
	H-level	V <sub>OH</sub>	VIN = VIH or VIL	$I_{OH} = -12 \text{ mA}$	2.7	2.2	_	V
				$I_{OH} = -18 \text{ mA}$	3.0	2.4		
Output voltage  L-level				$I_{OH} = -24 \text{ mA}$	3.0	2.2	_	
			VIN = VIH	I <sub>OL</sub> = 100 μA	2.7 to 3.6	_	0.2	
	Llovol	V <sub>OL</sub>		$I_{OL} = 12 \text{ mA}$	2.7	_	0.4	
	L-level	VOL		I <sub>OL</sub> = 16 mA	3.0	_	0.4	
				I <sub>OL</sub> = 24 mA	3.0	_	0.55	
Input leakage curre	nt	I <sub>IN</sub>	V <sub>IN</sub> = 0 to 5.5 V		2.7 to 3.6	_	±5.0	μА
Power off leakage of	current	I <sub>OFF</sub>	V <sub>IN</sub> /V <sub>OUT</sub> = 5.5 V		0	_	10.0	μА
Ouisseent supply suggest		Icc	V <sub>IN</sub> = V <sub>CC</sub> or GND		2.7 to 3.6	_	10.0	
Quiescent supply current	V <sub>IN</sub> = 3.6 to 5.5 V		2.7 to 3.6	_	±10.0	μΑ		
Increase in Icc per i	nput	Δlcc	$V_{IH} = V_{CC} - 0.6 V$		2.7 to 3.6		500	

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## AC Characteristics ( $Ta = -40 \text{ to } 85^{\circ}\text{C}$ )

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Min	Max	Unit
Propagation delay time	t <sub>pLH</sub>	Figure 1, Figure 2	2.7		6.0	- ns
	t <sub>pHL</sub>		$3.3 \pm 0.3$	1.5	5.2	
Output to output skew	t <sub>osLH</sub>	(Note)	2.7	_		- ns
	t <sub>osHL</sub>		$3.3 \pm 0.3$		1.0	

Note: Parameter guaranteed by design.

 $(t_{OSLH} = |t_{DLHm} - t_{DLHn}|, t_{OSHL} = |t_{DHLm} - t_{DHLn}|)$ 

#### Dynamic Switching Characteristics (Ta = 25°C, input: $t_r = t_f = 2.5$ ns, $C_L = 50$ pF, $R_L = 500 \Omega$ )

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Тур.	Unit
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$	3.3	8.0	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$	3.3	0.8	٧

#### **Capacitive Characteristics (Ta = 25°C)**

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Тур.	Unit
Input capacitance	C <sub>IN</sub>	_	3.3	7	pF
Output capacitance	C <sub>OUT</sub>	_	0	8	pF
Power dissipation capacitance	C <sub>PD</sub>	$f_{IN} = 10 \text{ MHz}$ (No	e) 3.3	25	pF

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per gate)}$ 

#### **AC Test Circuit**

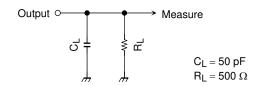


Figure 1

#### **AC Waveform**

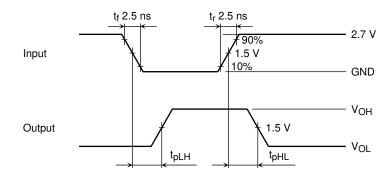
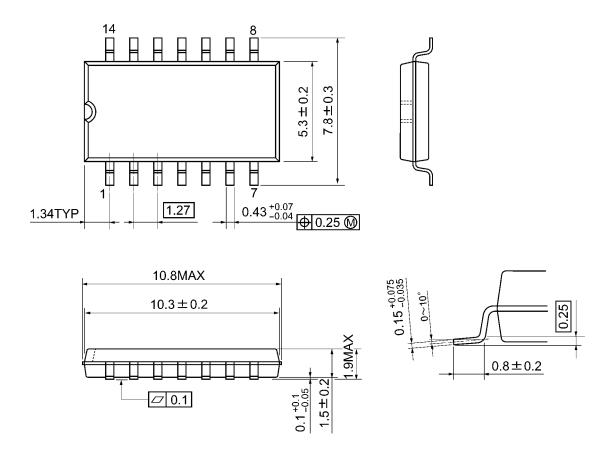


Figure 2 t<sub>pLH</sub>, t<sub>pHL</sub>

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# **Package Dimensions**

SOP14-P-300-1.27A Unit: mm



6

Weight: 0.18 g (typ.)

45°

0.7±0.3

# **Package Dimensions (Note)**

SOL14-P-150-1.27 Unit: mm 14 月月月月 H B 0.515TYP 0.42±0.07 **⊕** 0.25 **ω** 1.27 8.65±0.1

0.175±0.075

**2**0.1

This package is not available in japan. Note:

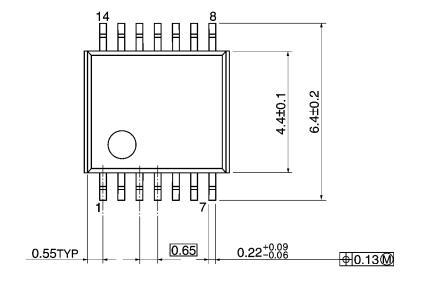
Weight: 0.12 g (typ.)

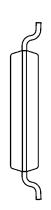
# Package Dimensions

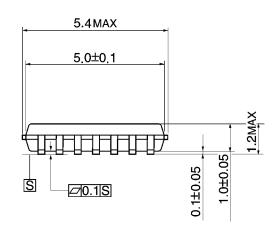
**TOSHIBA** 

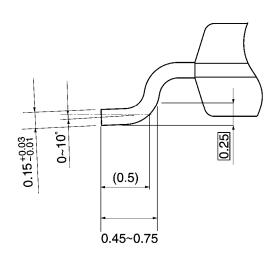
TSSOP14-P-0044-0.65A

Unit: mm





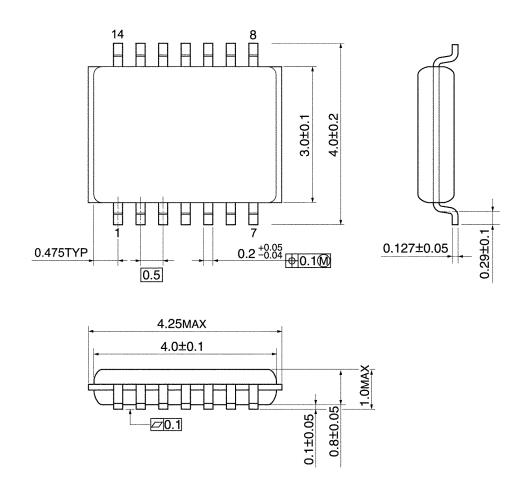




Weight: 0.06 g (typ.)

# **Package Dimensions**

VSSOP14-P-0030-0.50 Unit: mm



Weight: 0.02 g (typ.)

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