



# PHKD13N03LT

Dual N-channel TrenchMOS logic level FET

Rev. 5 — 27 December 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Dual logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Simple gate drive required due to low gate charge
- Suitable for high frequency applications due to fast switching characteristics

### 1.3 Applications

- DC-to-DC convertors
- Lithium-ion battery applications
- Notebook computers
- Portable equipment

### 1.4 Quick reference data

Table 1. Quick reference data

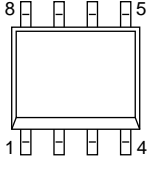
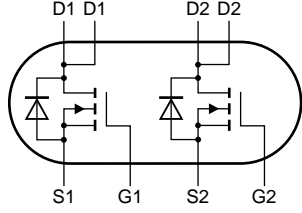
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	-	30	V
$I_D$	drain current	$T_{sp} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> ; <a href="#">[1]</a> see <a href="#">Figure 3</a>	-	-	10.4	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	3.57	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 8\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	17	20	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 5\text{ V}$ ; $I_D = 5\text{ A}$ ; $V_{DS} = 15\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 11</a>	-	3.9	-	nC

[1] Single device conducting.



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>SOT96-1 (SO8)</p>	 <p>mbk725</p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain		

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PHKD13N03LT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

## 4. Limiting values

Table 4. Limiting values

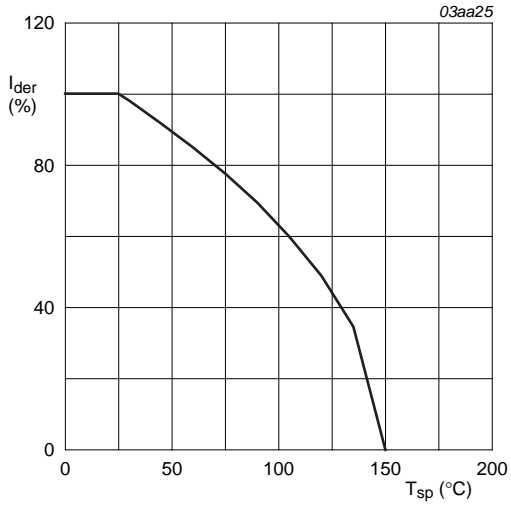
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C}$	-	30	V	
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C}; R_{GS} = 20\text{ k}\Omega$	-	30	V	
$V_{GS}$	gate-source voltage		-20	20	V	
$I_D$	drain current	$T_{sp} = 100\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a>	[1]	-	6.6	A
		$T_{sp} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	[1]	-	10.4	A
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ see <a href="#">Figure 3</a>	[1]	-	42	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C};$ see <a href="#">Figure 2</a>	-	3.57	W	
$T_{stg}$	storage temperature		-55	150	°C	
$T_j$	junction temperature		-55	150	°C	

### Source-drain diode

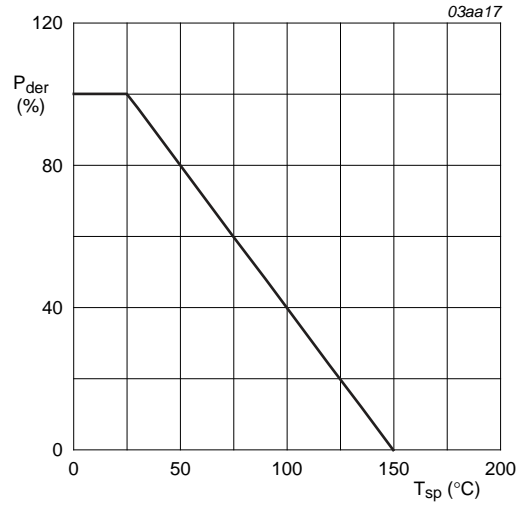
$I_S$	source current	$T_{sp} = 25\text{ °C}$	[1]	-	3.2	A
$I_{SM}$	peak source current	$T_{sp} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	[1]	-	42	A

[1] Single device conducting.



$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of solder point temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature

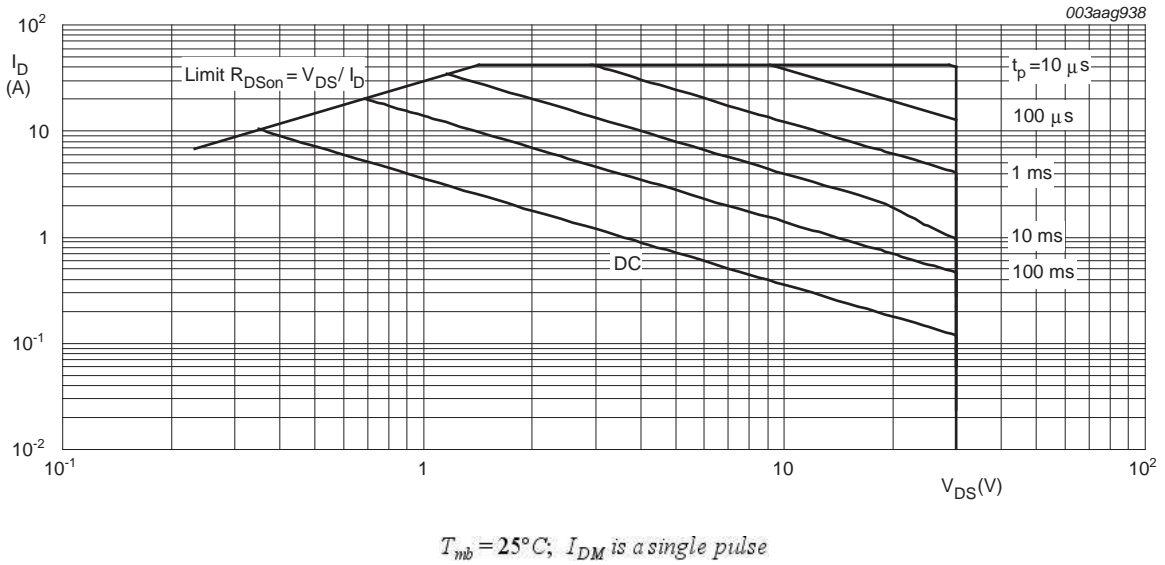


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see <a href="#">Figure 4</a>	-	-	35	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board	-	70	-	K/W

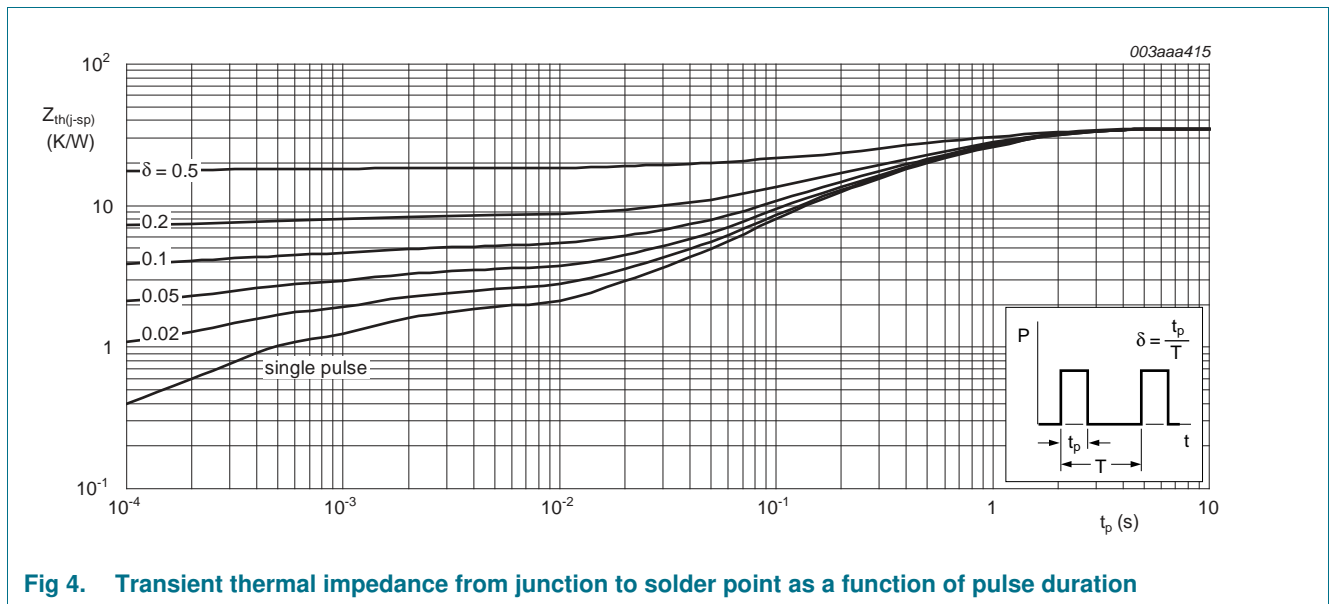


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

## 6. Characteristics

**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	27	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 250 \mu\text{A}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 8</a>	-	-	2.2	V
		$I_D = 250 \mu\text{A}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 8</a>	0.5	-	-	V
		$I_D = 250 \mu\text{A}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 8</a>	1	1.5	2	V
$I_{DSS}$	drain leakage current	$V_{DS} = 24 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 24 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 100 \text{ }^\circ\text{C}$	-	-	5	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 8 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	-	34	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 7 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a>	-	21	26	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 8 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	17	20	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 5 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a>	-	10.7	-	nC
$Q_{GS}$	gate-source charge		-	2.7	-	nC
$Q_{GD}$	gate-drain charge		-	3.9	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 15 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	752	-	pF
$C_{oss}$	output capacitance		-	200	-	pF
$C_{rss}$	reverse transfer capacitance		-	130	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 \text{ V}; R_L = 10 \text{ }^\circ\Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 6 \text{ }^\circ\Omega; T_j = 25 \text{ }^\circ\text{C}; I_D = 1.5 \text{ A}$	-	6	-	ns
$t_r$	rise time		-	7	-	ns
$t_{d(off)}$	turn-off delay time		-	23	-	ns
$t_f$	fall time		-	11	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 7 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a>	-	0.86	1.1	V
$t_{rr}$	reverse recovery time	$I_S = 7 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 30 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	25	-	ns
$Q_r$	recovered charge		-	5	-	nC

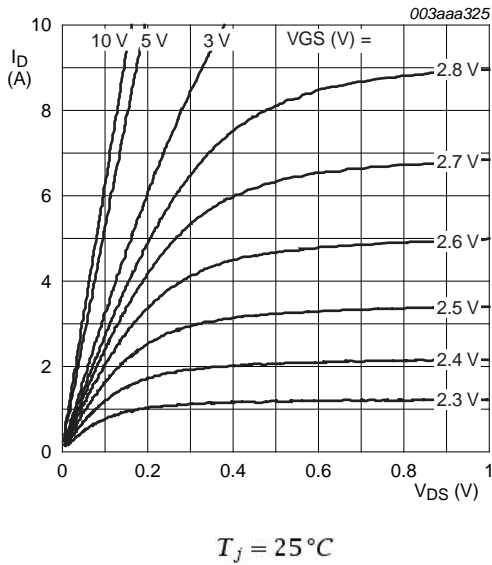


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

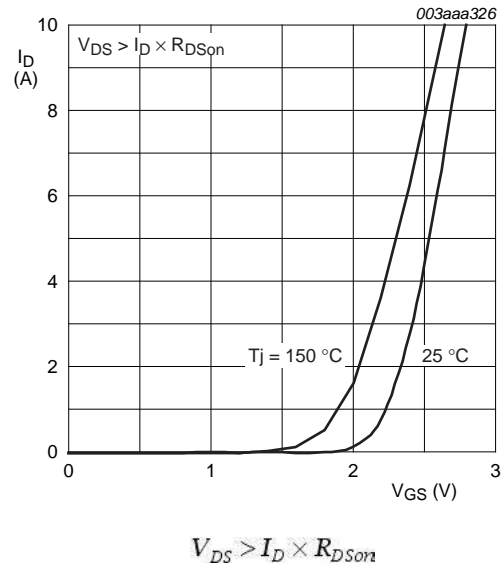


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

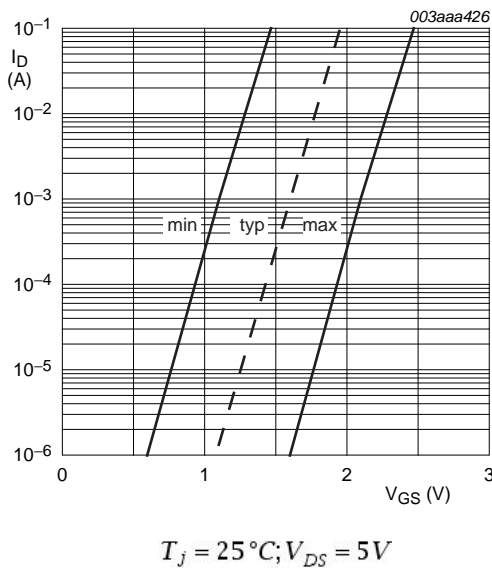


Fig 7. Sub-threshold drain current as a function of gate-source voltage

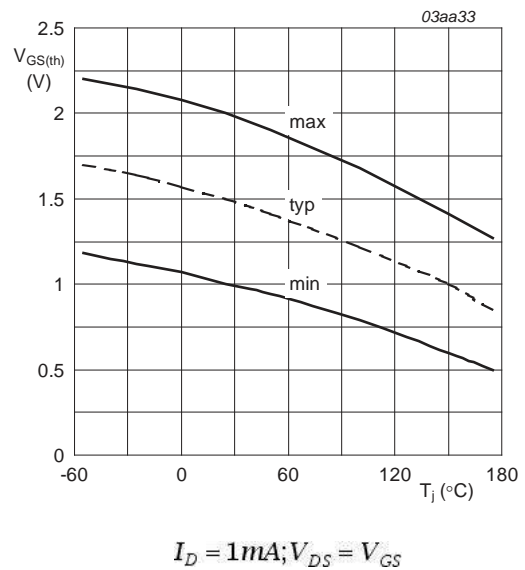
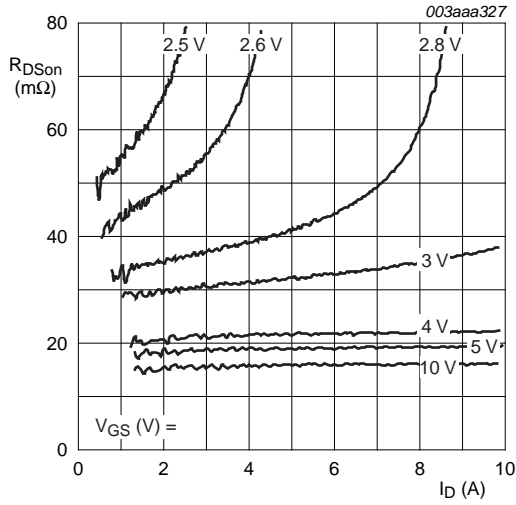
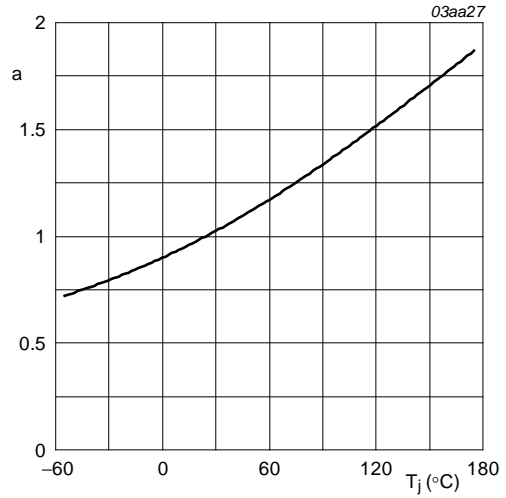


Fig 8. Gate-source threshold voltage as a function of junction temperature



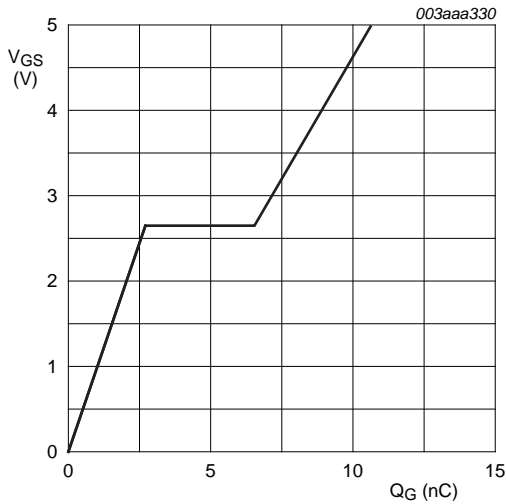
$T_j = 25^\circ\text{C}$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



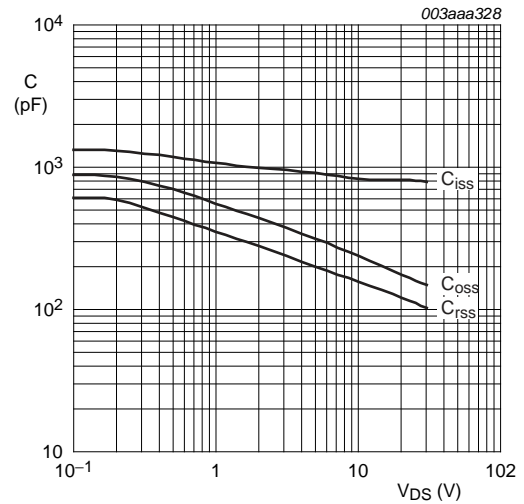
$$a = \frac{R_{DS(on)}}{R_{DS(on)@25^\circ\text{C}}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



$I_D = 8\text{A}; V_{DD} = 15\text{V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{V}; f = 1\text{MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

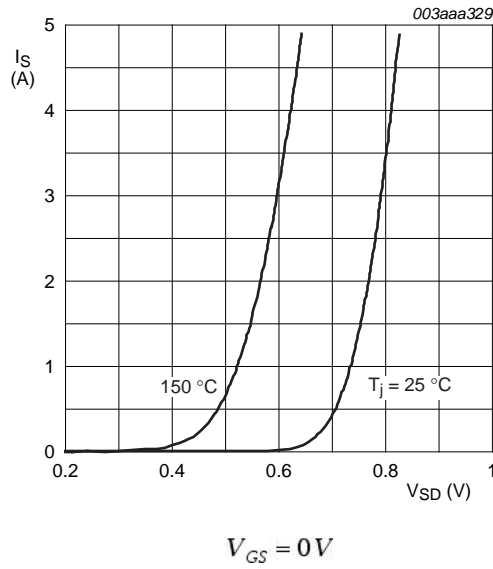


Fig 13. Source current as a function of source-drain voltage; typical values



7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

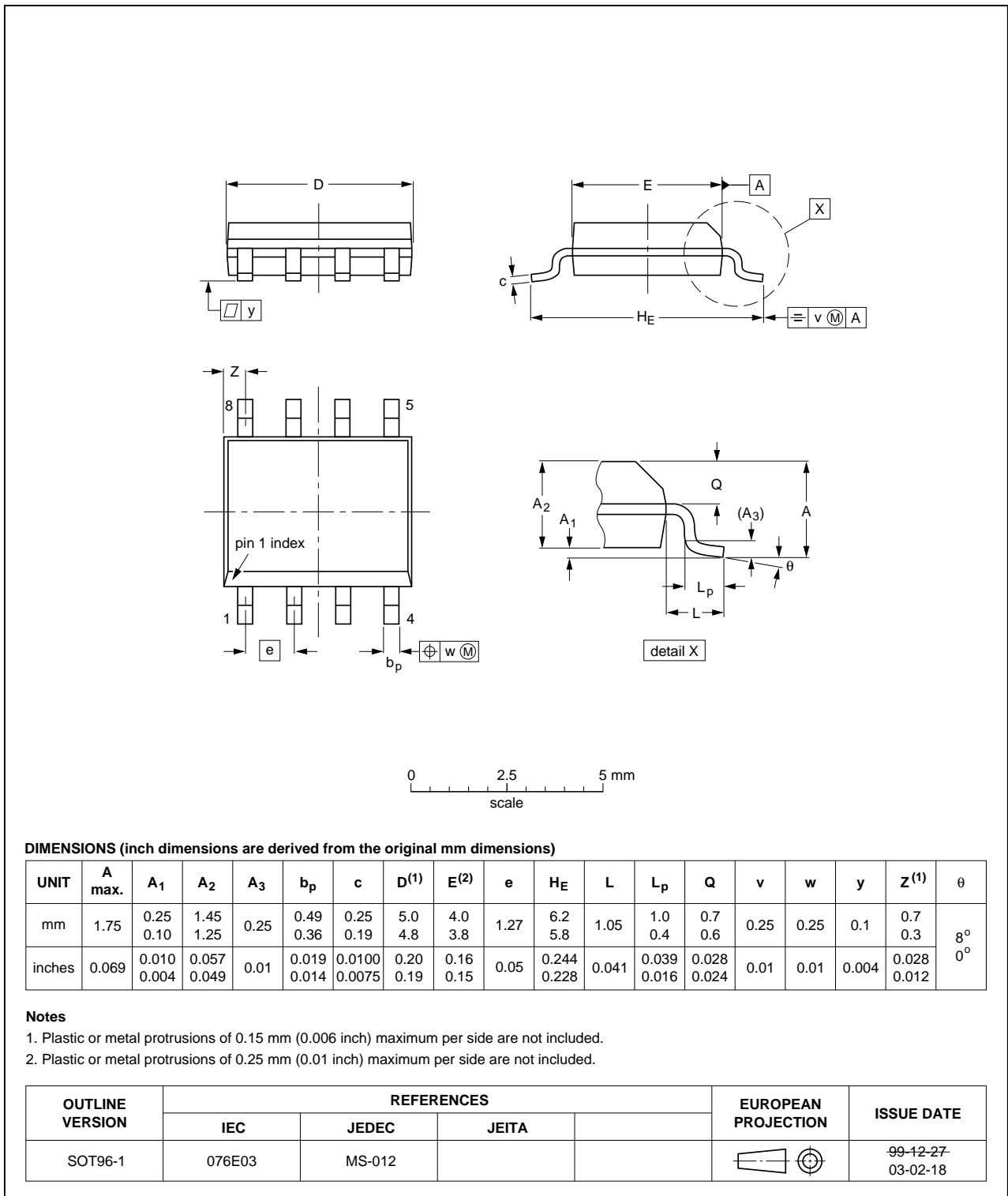


Fig 14. Package outline SOT96-1 (SO8)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHKD13N03LT v.5	20111227	Product data sheet	-	PHKD13N03LT v.4
Modifications:	• Various changes to content.			
PHKD13N03LT v.4	20111122	Product data sheet	-	PHKD13N03LT v.3

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### 9.1 Data sheet status

Document status <sup>[1]</sup> <sup>[2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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