FET BIAS CONTROLLER AND POLARITY SWITCH

ZNBG3010
ZNBG3011

ISSUE 1 - FEBRUARY 1998

DEVICE DESCRIPTION

The ZNBG series of devices are designed to meet the bias requirements of GaAs and HEMT FETs commonly used in satellite receiver LNBs, PMR cellular telephones etc. with a minimum of external components.

With the addition of two capacitors and a resistor, the devices provide drain voltage and current control for three external grounded source FETs, generating the regulated negative rail required for FET gate biasing whilst operating from a single supply. This negative bias, at -3 volts, can also be used to supply other external circuits.

The ZNBG3010/11 includes bias circuits to drive up to three external FETs. A control input to the device selects either one of two FETs as operational, the third FET is permanently active. This feature is particularly used as an LNB polarisation switch.

Drain current setting of the ZNBG3010/11 is user selectable over the range 0 to 15mA, this is achieved with addition of a single resistor. The series also offers the choice of drain voltage to be set for the FETs, the ZNBG3010 gives 2.2 volts drain whilst the ZNBG3011 gives 2 volts.

These devices are unconditionally stable over the full working temperature with the FETs in place, subject to the inclusion of the recommended gate and drain capacitors. These ensure RF stability and minimal injected noise.

It is possible to use less than the devices full complement of FET bias controls, unused drain and gate connections can be left open circuit without affecting operation of the remaining bias circuits.

In order to protect the external FETs the circuits have been designed to ensure that, under any conditions including power up/down transients, the gate drive from the bias circuits cannot exceed the range -3.5V to 1V. Furthermore if the negative rail experiences a fault condition, such as overload or short circuit, the drain supply to the FETs will shut down avoiding excessive current flow.

The ZNBG3010/11 are available in QSOP16 for the minimum in device size. Device operating temperature is -40 to 70°C to suit a wide range of environmental conditions.

FEATURES

- Provides bias for GaAs and HEMT FETs
- Drives up to three FETs
- Dynamic FET protection
- Drain current set by external resistor
- Regulated negative rail generator requires only 2 external capacitors
- Choice in drain voltage
- Wide supply voltage range
- Polarisation switch for LNBs
- QSOP surface mount package

APPLICATIONS

- Satellite receiver LNBs
- Private mobile radio (PMR)
- Cellular telephones

ZNBG3010
ZNBG3011

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.6V to 12V
Supply Current	100mA
Input Voltage (V_{POL})	25V Continuous
Drain Current (per FET) (set by R_{CAL})	0 to 15mA
Operating Temperature	-40 to 70°C
Storage Temperature	-50 to 85°C

Power Dissipation (T_{amb}= 25°C)

QSOP16	500mW

ELECTRICAL CHARACTERISTICS TEST CONDITIONS
(Unless otherwise stated):T_{amb}= 25°C,V_{CC}=5V,I_D=10mA (R_{CAL}=33kΩ)

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
V_{CC}	Supply Voltage		5		10	V
I_{CC}	Supply Current	I_{D1} to I_{D3}=0 I_{D2} and I_{D3}=10mA, V_{POL}=14V I_{D1} and I_{D3}=10mA, V_{POL}=15.5V			10 30 30	mA mA mA
V_{SUB}	Substrate Voltage (Internally generated)	I_{SUB}=0 I_{SUB}=-200μA	-3.5	-3.0	-2 -2	V V
	Output Noise					
E_{ND}	Drain Voltage	C_G=4.7nF, C_D=10nF			0.02	Vpkpk
E_{NG}	Gate Voltage	C_G=4.7nF, C_D=10nF			0.005	Vpkpk
f_O	Oscillator Frequency		200	350	800	kHz

GATE CHARACTERISTICS

I_{GO}	Output Current Range		-30		2000	μA
		I_{Dx} (mA) V_{POL} (V) I_{GOx} (μA)				
	Output Voltage					
V_{G1O}	Gate 1 Off	I_{D1}=0 V_{POL}=14 I_{GO1}=-10	-3.5	-2.9	-2.0	V
V_{G1L}	Low	I_{D1}=12 V_{POL}=15.5 I_{GO1}=-10	-3.5	-2.9	-2.0	V
V_{G1H}	High	I_{D1}=8 V_{POL}=15.5 I_{GO1}=0	0.4	0.75	1.0	V
	Output Voltage					
V_{G2O}	Gate 2 Off	I_{D2}=0 V_{POL}=15.5 I_{GO2}=-10	-3.5	-2.9	-2.0	V
V_{G2L}	Low	I_{D2}=12 V_{POL}=14 I_{GO2}=-10	-3.5	-2.9	-2.0	V
V_{G2H}	High	I_{D2}=8 V_{POL}=14 I_{GO2}=0	0.4	0.75	1.0	V
	Output Voltage					
V_{G3L}	Gate 3 Low	I_{D3}=12 I_{GO3}=-10	-3.5	-2.9	-2.0	V
V_{G3H}	High	I_{D3}=8 I_{GO3}=0	0.4	0.75	1.0	V

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
DRAIN CHARACTERISTICS						
I_D	Current		8	10	12	mA
 ΔI_{DV} ΔI_{DT}	Current Change with V_{CC} with T_j	 V_{CC}= 5 to 10V T_j=-40 to +70°C		 0.2 0.05		 %/V %/°C
V_{D1}	Drain 1 Voltage:High ZNBG3010 ZNBG3011	 I_{D1}=10mA, V_{POL}=15.5V I_{D1}=10mA, V_{POL}=15.5V	 2.0 1.8	 2.2 2.0	 2.4 2.2	 V V
V_{D2}	Drain 2 Voltage:High ZNBG3010 ZNBG3011	 I_{D2}=10mA, V_{POL}=14V I_{D2}=10mA, V_{POL}=14V	 2.0 1.8	 2.2 2.0	 2.4 2.2	 V V
V_{D3}	Drain 3 Voltage:High ZNBG3010 ZNBG3011	 I_{D3}=10mA, V_{POL}=15.5V I_{D3}=10mA, V_{POL}=15.5V	 2.0 1.8	 2.2 2.0	 2.4 2.2	 V V
 ΔV_{DV} ΔV_{DT}	Voltage Change with V_{CC} with T_j	 V_{CC}= 5 to 10V T_j=-40 to +70°C		 0.5 50		 %/V ppm
 I_{L1} I_{L2}	Leakage Current Drain 1 Drain 2	 V_{D1}=0.1V, V_{POL}=14V V_{D2}=0.1V, V_{POL}=15.5V			 10 10	 μA μA
POLARITY SWITCH CHARACTERISTICS						
I_{POL}	Input Current	V_{POL}=25V (Applied via R_{POL}=10kΩ	10	20	40	μA
V_{TPOL}	Threshold Voltage	(Applied via R_{POL}=10kΩ	14	14.75	15.5	V
T_{SPOL}	Switching Speed				100	μs

Notes:

1. The negative bias voltages specified are generated on-chip using an internal oscillator. Two external capacitors, C_{NB} and C_{SUB}, of 47nF are required for this purpose.

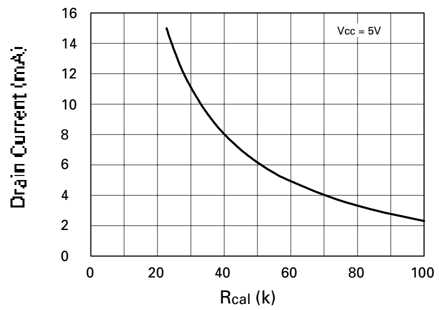
2. The characteristics are measured using an external reference resistor R_{CAL} of value 33k wired from pins R_{CAL} to ground.

3. Noise voltage is not measured in production.

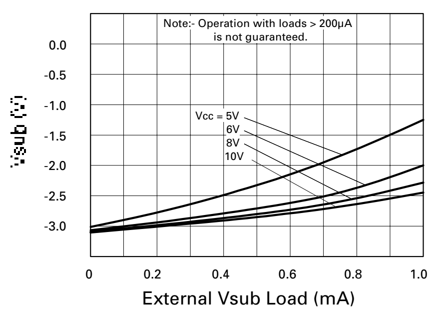
4. Noise voltage measurement is made with FETs and gate and drain capacitors in place on all outputs. C_G, 4.7nF, are connected between gate outputs and ground, C_D, 10nF, are connected between drain outputs and ground.

ZNBG3010
ZNBG3011

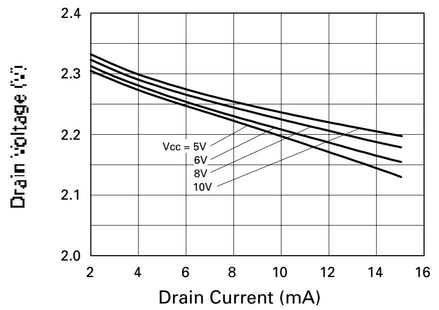
TYPICAL CHARACTERISTICS



JFET Drain Current v Rcal

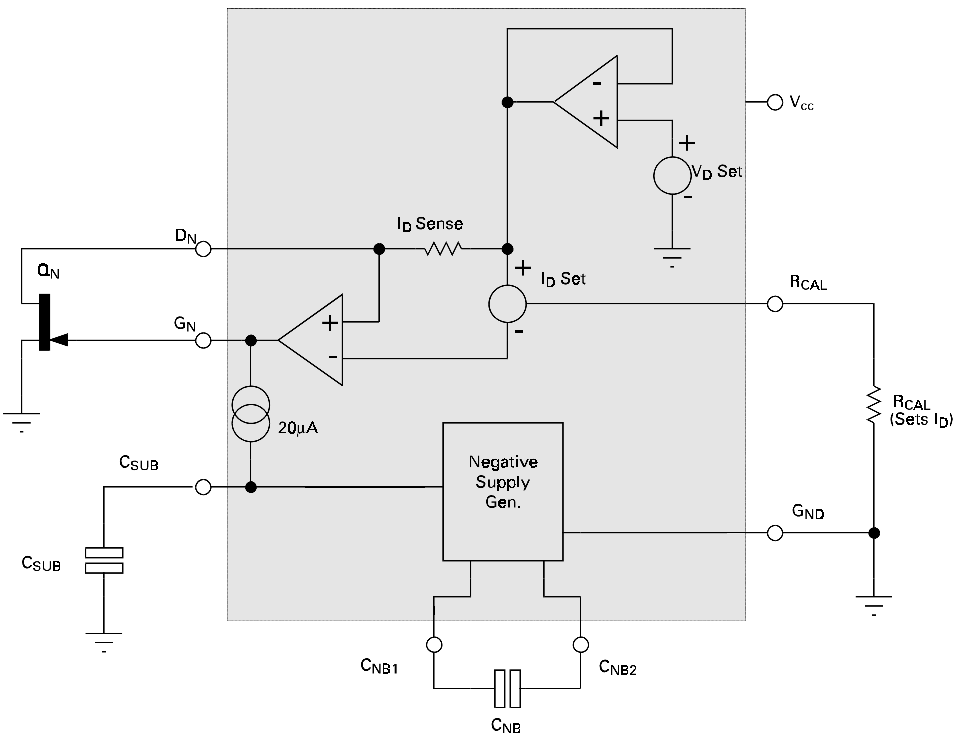


Vsub v External Load



JFET Drain Voltage v Drain Current

FUNCTIONAL DIAGRAM



FUNCTIONAL DESCRIPTION

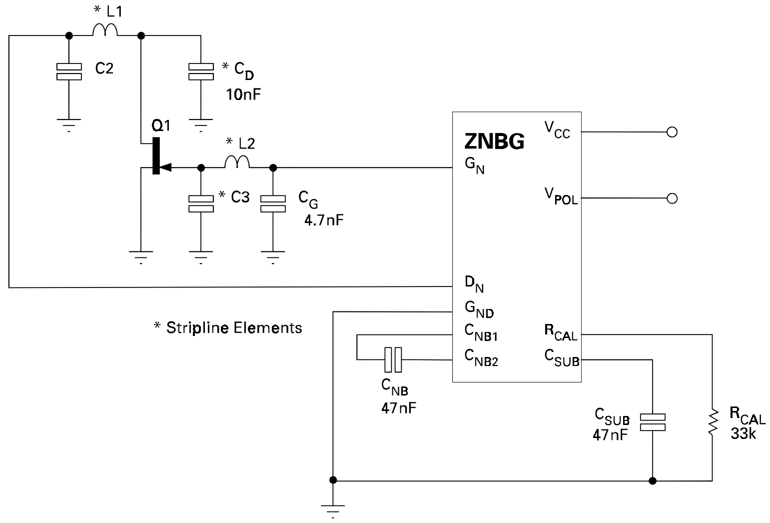
The ZNBG devices provide all the bias requirements for external FETs, including the generation of the negative supply required for gate biasing, from the single supply voltage.The diagram above shows a single stage from the ZNBG series. The ZNBG3010/11 contains 3 such stages. The negative rail generator is common to both devices.

The drain voltage of the external FET Q_N is set by the ZNBG device to its normal operating voltage. This is determined by the on board V_D Set reference, for the ZNBG3010 this is nominally 2.2 volts whilst the ZNBG3011 provides nominally 2 volts.

The drain current taken by the FET is monitored by the low value resistor I_D Sense. The amplifier driving the gate of the FET adjusts the gate voltage of Q_N so that the drain current taken matches the current called for by an external resistor R_{CAL}.

Since the FET is a depletion mode transistor, it is often necessary to drive its gate negative with respect to ground to obtain the required drain current. To provide this capability powered from a single positive supply, the device includes a low current negative supply generator. This generator uses an internal oscillator and two external capacitors, C_{NB} and C_{SUB}.

APPLICATIONS CIRCUIT



APPLICATIONS INFORMATION

The above is a partial application circuit for the ZNBG series showing all external components required for appropriate biasing. The bias circuits are unconditionally stable over the full temperature range with the associated FETs and gate and drain capacitors in circuit.

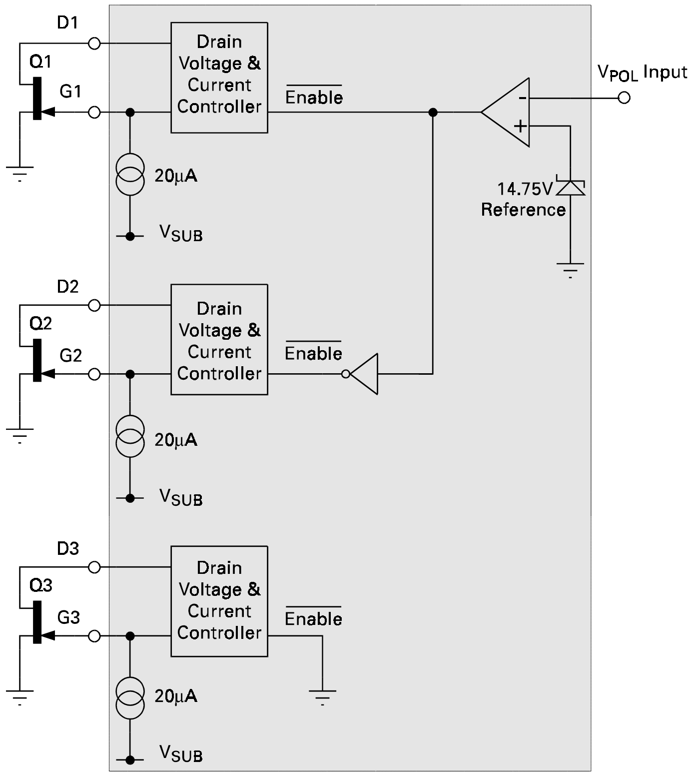
Capacitors C_D and C_G ensure that residual power supply and substrate generator noise is not allowed to affect other external circuits which may be sensitive to RF interference. They also serve to suppress any potential RF feedthrough between stages via the ZNBG device. These capacitors are required for all stages used. Values of 10nF and 4.7nF respectively are recommended however this is design dependent and any value between 1nF and 100nF could be used.

The capacitors C_{NB} and C_{SUB} are an integral part of the ZNBGs negative supply generator. The negative bias voltage is generated on-chip using an internal oscillator. The required value of capacitors C_{NB} and C_{SUB} is 47nF. This generator produces a low current supply of approximately -3 volts. Although this generator is intended purely to bias the external FETs, it can be used to power other external circuits via the C_{SUB} pin.

Resistor R_{CAL} sets the drain current at which all external FETs are operated. If any bias control circuit is not required, its related drain and gate connections may be left open circuit without affecting the operation of the remaining bias circuits.

The ZNBG devices have been designed to protect the external FETs from adverse operating conditions. With a JFET connected to any bias circuit, the gate output voltage of the bias circuit can not exceed the range -3.5V to 1V, under any conditions including powerup and powerdown transients. Should the negative bias generator be shorted or overloaded so that the drain current of the external FETs can no longer be controlled, the drain supply to FETs is shut down to avoid damage to the FETs by excessive drain current.

The following schematic shows the function of the V_{POL} input. Only one of the two external FETs numberd Q1 and Q2 are powered at any one time, their selection is controlled by the input V_{POL}. This input is designed to be wired to the power input of the LNB via a high value (10k) resistor. With the input voltage of the LNB set at or below 14V, FET Q2 will be enabled. With the input voltage at or above 15.5V, FET Q1 will be enabled. The disabled FET has its gate driven low and its drain terminal is switched open circuit. It is permissible to connect the drain pins D1 and D2 together if required by the application circuit. FET number Q3 is always active regardless of the voltage applied to V_{POL}.



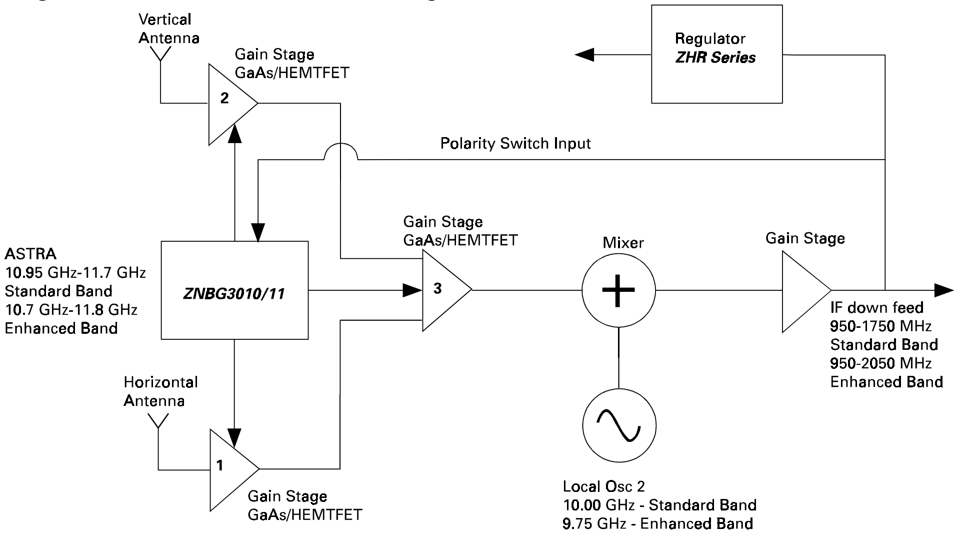
Control Input Switch Function

Input Sense	Polarisation	Select
≤14 volts	Vertical	FET Q2
≥ 15.5 volts	Horizontal	FET Q1

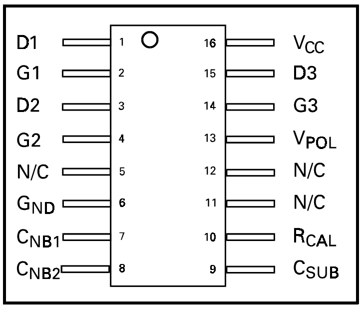
APPLICATIONS INFORMATION (Continued)

The following block diagram shows the main section of an LNB designed for use with the Astra series of satellites. The ZNBG3010/11 is the core bias and control element of this circuit. The ZNBG provides the negative rail, FET bias control and polarisation switch control, with the minimum of external components. Compared to other discrete component solutions the ZNBG circuit reduces component count and overall size required.

Single Standard/ Enhanced LNB block diagram.



CONNECTION DIAGRAM

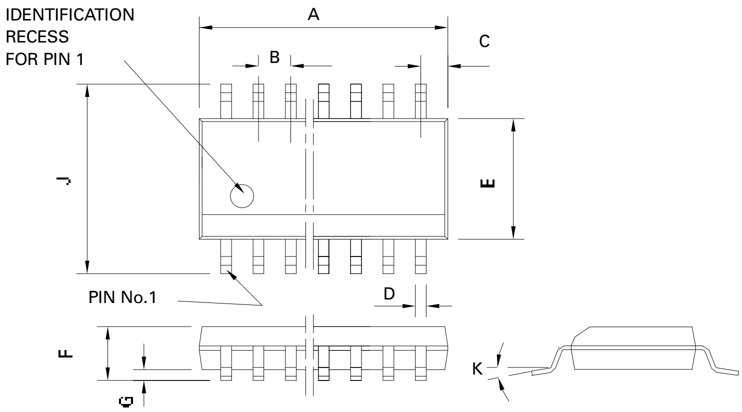


ORDERING INFORMATION

Part Number	Package	Part Mark
ZNBG3010Q16	QSOP16	ZNBG3010
ZNBG3011Q16	QSOP16	ZNBG3011

ZNBG3010
ZNBG3011

PACKAGE DIMENSIONS



PIN	Millimetres		Inches	
	MIN	MAX	MIN	MAX
A	4.80	4.90	0.189	0.196
B	0.635		0.025 NOM	
C	0.177	0.267	0.007	0.011
D	0.20	0.30	0.008	0.012
E	3.81	3.99	0.15	0.157
F	1.35	1.75	0.053	0.069
G	0.10	0.25	0.004	0.01
J	5.79	6.20	0.228	0.244
K	0°	8°	0°	8°

ZETEX

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