



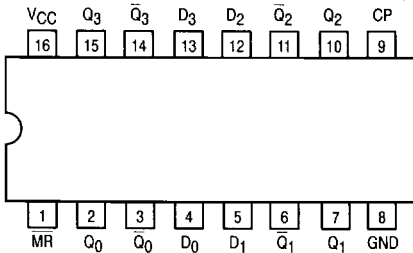
QUAD D FLIP-FLOP

The LSTTL/MSI SN54/74LS175 is a high speed Quad D Flip-Flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW to HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

The LS175 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Edge-Triggered D-Type Inputs
- Buffered-Positive Edge-Triggered Clock
- Clock to Output Delays of 30 ns
- Asynchronous Common Reset
- True and Complement Output
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

- D₀-D₃ Data Inputs
- CP Clock (Active HIGH Going Edge) Input
- MR Master Reset (Active LOW) Input
- Q₀-Q₃ True Outputs (Note b)
- Q₀-Q₃ Complemented Outputs (Note b)

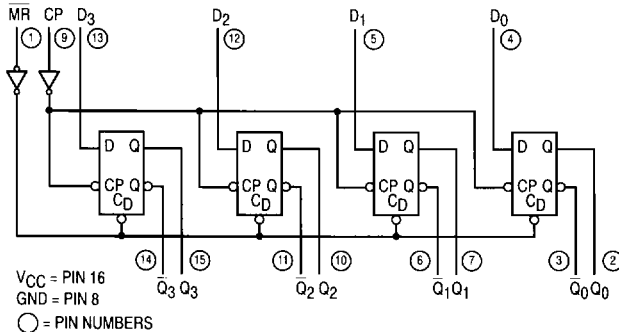
LOADING (Note a)

	HIGH	LOW
D ₀ -D ₃	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
MR	0.5 U.L.	0.25 U.L.
Q ₀ -Q ₃	10 U.L.	5 (2.5) U.L.
Q ₀ -Q ₃	10 U.L.	5 (2.5) U.L.

NOTES:

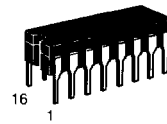
- 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

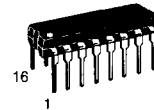


SN54/74LS175

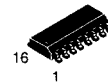
QUAD D FLIP-FLOP LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

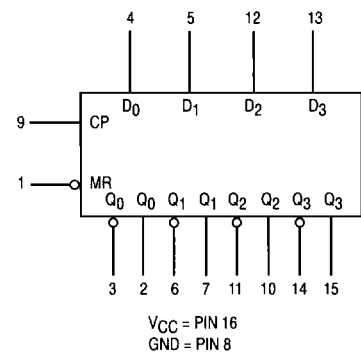


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

- SN54LSXXXJ Ceramic
- SN74LSXXXN Plastic
- SN74LSXXXD SOIC

LOGIC SYMBOL



SN54/74LS175

FUNCTIONAL DESCRIPTION

The LS175 consists of four edge-triggered D flip-flops with individual D inputs and Q and \bar{Q} outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW to HIGH Clock (CP) transition, causing individual Q and \bar{Q} outputs to follow. A

LOW input on the Master Reset (\overline{MR}) will force all Q outputs LOW and \bar{Q} outputs HIGH independent of Clock or Data inputs.

The LS175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

TRUTH TABLE

Inputs (t = n, MR = H)	Outputs (t = n+1) Note 1	
D	Q	\bar{Q}
L	L	H
H	H	L

Note 1: t = n + 1 indicates conditions after next clock.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			18	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS175

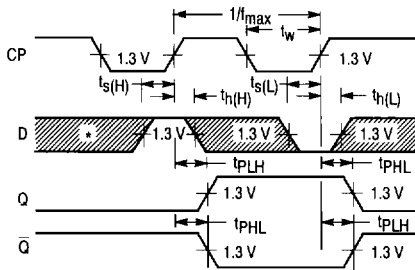
AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f_{MAX}	Maximum Input Clock Frequency	30	40		MHz	$V_{\text{CC}} = 5.0\text{ V}$ $C_L = 15\text{ pF}$
t_{PLH} t_{PHL}	Propagation Delay, $\overline{\text{MR}}$ to Output		20 20	30 30	ns	
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		13 16	25 25	ns	

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{W}	Clock or $\overline{\text{MR}}$ Pulse Width	20			ns	$V_{\text{CC}} = 5.0\text{ V}$
t_{s}	Data Setup Time	20			ns	
t_{h}	Data Hold Time	5.0			ns	
t_{rec}	Recovery Time	25			ns	

AC WAVEFORMS



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 1. Clock to Output Delays, Clock Pulse Width, Frequency, Setup and Hold Times Data to Clock

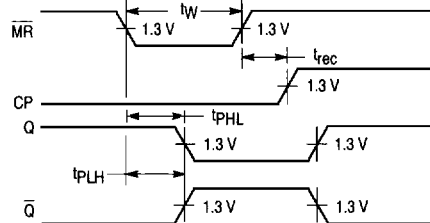


Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

DEFINITIONS OF TERMS

SETUP TIME (t_{s}) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_{h}) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recog-

nition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.