19-0792; Rev 0; 4/07

EVALUATION KIT AVAILABLE

1.62V to 3.6V Improved High-Speed LLT

General Description

The MAX13042E–MAX13045E 4-channel, bidirectional level translators provide the level shifting necessary for 100Mbps data transfer in multivoltage systems. The MAX13042E–MAX13045E are ideally suited for level translation in systems with four channels. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. Logic signals present on the V_L side of the device appear as a high-voltage logic signal on the V_{CC} side of the device and vice-versa.

The MAX13042E–MAX13045E operate at full speed with external drivers that source as little as 4mA output current or larger. Each input/output (I/O) channel is pulled up to V_{CC} or V_L by an internal 30µA current source, allowing the MAX13042E–MAX13045E to be driven by either push-pull or open-drain drivers.

The MAX13042E–MAX13045E feature an enable (EN) input that places the devices into a low-power shutdown mode when driven low. The MAX13042E–MAX13045E feature an automatic shutdown mode that disables the part when V_{CC} is less than V_L. The state of I/O $V_{CC\_}$ and I/O $V_{L\_}$ during shutdown is chosen by selecting the appropriate part version. (See the *Ordering Information/Selector Guide*).

The MAX13042E–MAX13045E operate with V_{CC} voltages from +2.2V to +3.6V and V_L voltages from +1.62V to +3.2V, making them ideal for data transfer between low-voltage ASIC/PLDs and higher voltage systems. The MAX13042E–MAX13045E are available in 12-bump UCSP™ (1.54mm x 2.12mm) and 14-pin TDFN (3mm x 3mm) packages, and operate over the extended -40°C to +85°C temperature range.

Applications

CMOS Logic-Level Translation

Low-Voltage ASIC Level Translation

Cell Phones

SPI™, MICROWIRE™ Level Translation

Portable POS Systems

Portable Communication Devices

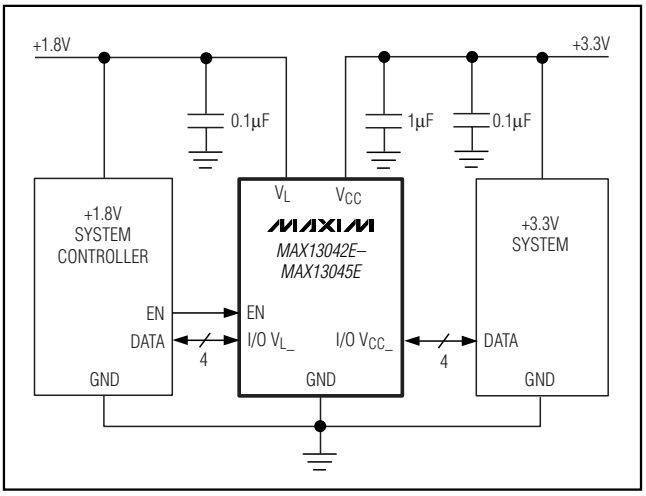
GPS

Telecommunications Equipment

Features

- **Compatible with 4mA Input Drivers or Larger**
- **100Mbps Guaranteed Data Rate**
- **Four Bidirectional Channels**
- **Enable Input**
- **±15kV ESD Protection on I/O $V_{CC\_}$ Lines**
- **+1.62V ≤ V_L ≤ +3.2V and +2.2V ≤ V_{CC} ≤ +3.6V Supply Voltage Range**
- **12-Bump UCSP (1.54mm x 2.12mm) and 14-Pin TDFN (3mm x 3mm) Lead-Free Packages**

Typical Operating Circuit



UCSP is a trademark of Maxim Integrated Products, Inc.
SPI is a trademark of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

Pin Configurations appear at end of data sheet.

Ordering Information/Selector Guide continued at end of data sheet.

Ordering Information/Selector Guide

PART	PIN-PACKAGE	I/O $V_{L\_}$ STATE DURING SHUTDOWN	I/O $V_{CC\_}$ STATE DURING SHUTDOWN	TOP MARK	PKG CODE
MAX13042EEBC+T	12 UCSP-12	High Impedance	High Impedance	ADQ	B12-3
MAX13042EETD+T	14 TDFN-EP**	High Impedance	High Impedance	ADE	T1433-2

***Note:** All devices operate over the -40°C to +85°C temperature range.*
+Denotes a lead-free package.
**Future product—contact factory for availability.*
***EP = Exposed paddle.*

1.62V to 3.6V Improved High-Speed LLT

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC}, V_L .....-0.3V to +4V
I/O $V_{CC\_}$ ..... -0.3V to (V_{CC} + 0.3V)
I/O $V_{L\_}$ .....-0.3V to (V_L + 0.3V)
EN.....-0.3V to +4V
Short-Circuit Duration I/O $V_{L\_}$, I/O $V_{CC\_}$ to GND .....Continuous
Continuous Power Dissipation (T_A = +70°C)
12-Bump UCSP (derate 6.5mW/°C above +70°C) 519mW
14-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.2V to +3.6V, V_L = +1.62V to +3.2V, EN = V_L, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
V_L Supply Range	V_L		1.62		3.2	V
V_{CC} Supply Range	V_{CC}		2.2		3.6	V
Supply Current from V_{CC}	I_{QVCC}	I/O $V_{CC\_}$ = V_{CC}, I/O $V_{L\_}$ = V_L			25	µA
Supply Current from V_L	I_{QVL}	I/O $V_{CC\_}$ = V_{CC}, I/O $V_{L\_}$ = V_L			10	µA
V_{CC} Shutdown Supply Current	$I_{SHDN-VCC}$	T_A = +25°C, EN = GND		0.1	1	µA
V_L Shutdown-Mode Supply Current	$I_{SHDN-VL}$	T_A = +25°C, EN = GND		0.1	1	µA
		T_A = +25°C, EN = V_L, V_{CC} = GND		0.1	4	
I/O $V_{CC\_}$, I/O $V_{L\_}$ Tri-State Leakage Current	I_{LEAK}	T_A = +25°C, EN = GND		0.1	2	µA
EN Input Leakage Current	I_{LEAK_EN}	T_A = +25°C			1	µA
V_L - V_{CC} Shutdown Threshold High	V_{TH_H}	V_{CC} rising (Note 3)	0	0.1V_L	0.8	V
V_L - V_{CC} Shutdown Threshold Low	V_{TH_L}	V_{CC} falling (Note 3)	0	0.12V_L	0.8	V
I/O $V_{CC\_}$ Pulldown Resistance During Shutdown	$R_{VCC\_PD\_SD}$	MAX13043E/MAX13045E	10	16.5	23	kΩ
I/O $V_{L\_}$ Pulldown Resistance During Shutdown	$R_{VL\_PD\_SD}$	MAX13044E/MAX13045E	10	16.5	23	kΩ
I/O $V_{L\_}$ Pullup Current	$I_{VL\_PU\_}$	I/O $V_{L\_}$ = GND, I/O $V_{CC\_}$ = GND	20		65	µA
I/O $V_{CC\_}$ Pullup Current	$I_{VCC\_PU\_}$	I/O $V_{CC\_}$ = GND, I/O $V_{L\_}$ = GND	20		65	µA
I/O $V_{L\_}$ to I/O $V_{CC\_}$ DC Resistance	R_{IOVL_IOVCC}	(Note 4)		3		kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.2V to +3.6V, V_L = +1.62V to +3.2V, EN = V_L, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD PROTECTION						
I/O $V_{L\_}$, EN		Human Body Model		±2		kV
I/O $V_{CC\_}$		Human Body Model, C_{VCC} = 1µF		±15		kV
		IEC 61000-4-2 Air-Gap Discharge, C_{VCC} = 1µF		±15		
		IEC 61000-4-2 Contact Discharge, C_{VCC} = 1µF		±8		
LOGIC LEVELS						
I/O $V_{L\_}$ Input-Voltage High Threshold	V_{IHL}	(Note 5)	V_L - 0.2			V
I/O $V_{L\_}$ Input-Voltage Low Threshold	V_{ILL}	(Note 5)			0.15	V
I/O $V_{CC\_}$ Input-Voltage High Threshold	V_{IHC}	(Note 5)	V_{CC} - 0.4			V
I/O $V_{CC\_}$ Input-Voltage Low Threshold	V_{ILC}	(Note 5)			0.2	V
EN Input-Voltage-High Threshold	V_{IH}		V_L - 0.4			V
EN Input-Voltage-Low Threshold	V_{IL}				0.4	V
I/O $V_{L\_}$ Output-Voltage High	V_{OHL}	I/O $V_{L\_}$ source current = 20µA	2/3 V_L			V
I/O $V_{L\_}$ Output-Voltage Low	V_{OLL}	I/O $V_{L\_}$ sink current = 20µA, I/O $V_{CC\_}$ < 0.2V			1/3 V_L	V
I/O $V_{CC\_}$ Output-Voltage High	V_{OHC}	I/O $V_{CC\_}$ source current = 20µA	2/3 V_{CC}			V
I/O $V_{CC\_}$ Output-Voltage Low	V_{OLC}	I/O $V_{CC\_}$ sink current = 20µA, I/O $V_{L\_}$ < 0.15V			1/3 V_{CC}	V
RISE-/FALL-TIME ACCELERATOR STAGE						
Accelerator Pulse Duration		On falling edge		3.5		ns
		On rising edge		3.5		
V_L Output Accelerator Source Impedance		V_L = 1.62V		24		Ω
		V_L = 3.2V		11		
V_{CC} Output Accelerator Source Impedance		V_{CC} = 2.2V		13		Ω
		V_{CC} = 3.6V		9		
V_L Output Accelerator Sink Impedance		V_L = 1.62V		14		Ω
		V_L = 3.2V		10		
V_{CC} Output Accelerator Sink Impedance		V_{CC} = 2.2V		11		Ω
		V_{CC} = 3.6V		9		

TIMING CHARACTERISTICS

(+2.2V ≤ V_{CC} ≤ +3.6V, +1.62V ≤ V_L ≤ +3.2V; $C_{IOVL\_}$ ≤ 15pF, $C_{IOVCC\_}$ ≤ 10pF; R_{SOURCE} < 150Ω, rise/fall time < 3ns, EN = V_L, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{CC\_}$ Rise Time	t_{RVCC}	Figure 1			2.5	ns
I/O $V_{CC\_}$ Fall Time	t_{FVCC}	Figure 1			2.5	ns
I/O $V_{L\_}$ Rise Time	t_{RVL}	Figure 2			2.5	ns
I/O $V_{L\_}$ Fall Time	t_{FVL}	Figure 2			2.5	ns
Propagation Delay (Driving I/O $V_{L\_}$)	$t_{PVL-VCC}$	Figure 1			6.5	ns
Propagation Delay (Driving I/O $V_{CC\_}$)	$t_{PVCC-VL}$	Figure 2			6.5	ns
Channel-to-Channel Skew	t_{SKEW}	(Note 4)			0.7	ns
Propagation Delay From I/O $V_{L\_}$ to I/O $V_{CC\_}$ after EN	t_{EN-VCC}	Figure 3		5		µs
Propagation Delay From I/O $V_{CC\_}$ to I/O $V_{L\_}$ after EN	t_{EN-VL}	Figure 3		5		µs
Maximum Data Rate		Push-pull operation	100			Mbps

Note 1: All units are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by correlation and design and not production tested.

Note 2: V_L must be less than or equal to V_{CC} during normal operation. However, V_L can be greater than V_{CC} during startup and shutdown conditions.

Note 3: When V_{CC} is below V_L by more than the V_L - V_{CC} shutdown threshold, the device turns off its pullup generators and the I/Os enter their respective shutdown states.

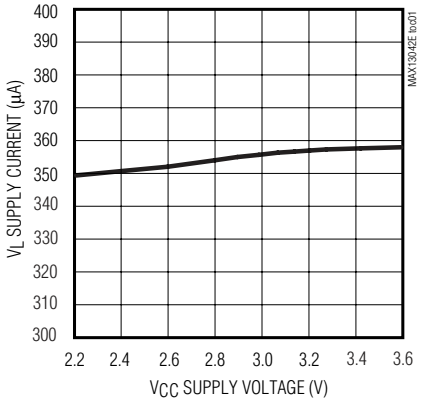
Note 4: Guaranteed by design.

Note 5: Input thresholds are referenced to the boost circuit.

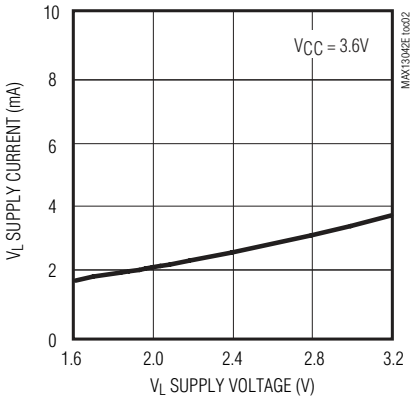
Typical Operating Characteristics

(V_{CC} = 3.3V, V_L = 1.8V, $C_{IOVCC\_}$ = 10pF, $C_{IOVL\_}$ = 15pF, R_{SOURCE} = 150Ω, data rate = 100Mbps, push-pull driver, T_A = +25°C, unless otherwise noted.)

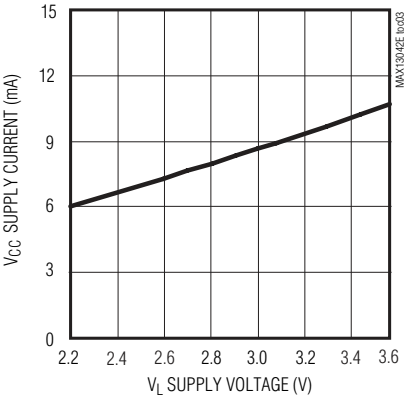
V_L SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE (DRIVING ONE I/O $V_{L\_}$)



V_L SUPPLY CURRENT vs. V_L SUPPLY VOLTAGE (DRIVING ONE I/O $V_{CC\_}$)



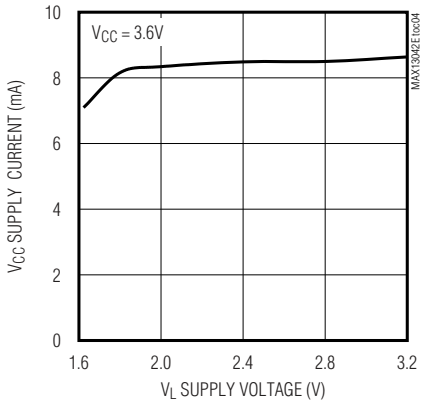
V_{CC} SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE (DRIVING ONE I/O $V_{L\_}$)



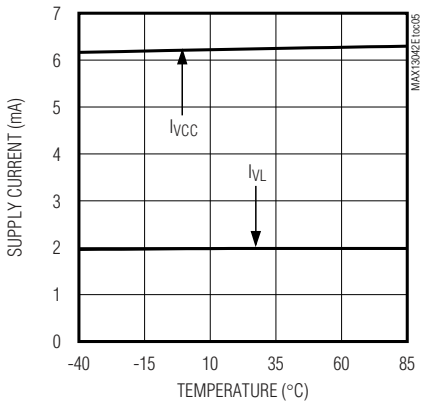
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, V_L = 1.8V, $C_{IOVCC\_}$ = 10pF, $C_{IOVL\_}$ = 15pF, R_{SOURCE} = 150Ω, data rate = 100Mbps, push-pull driver, T_A = +25°C, unless otherwise noted.)

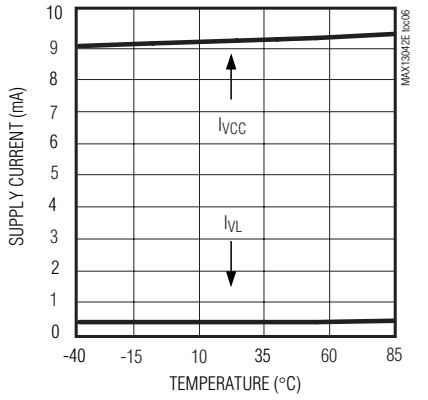
V_{CC} SUPPLY CURRENT vs. V_L SUPPLY VOLTAGE (DRIVING ONE I/O $V_{CC\_}$)



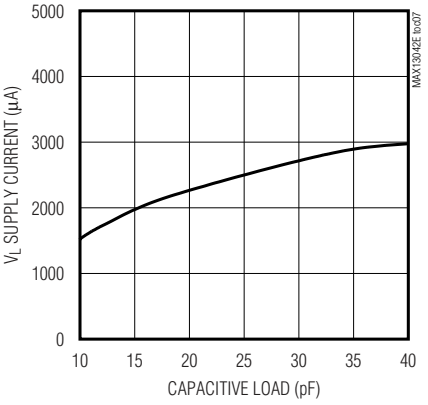
SUPPLY CURRENT vs. TEMPERATURE (DRIVING ONE I/O $V_{CC\_}$)



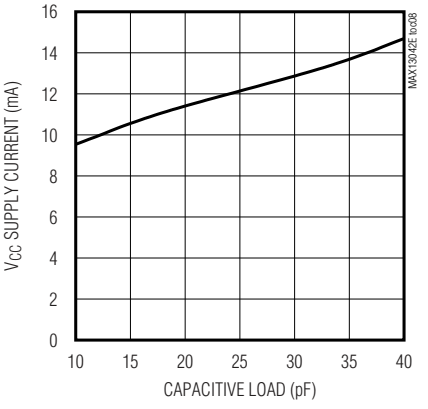
SUPPLY CURRENT vs. TEMPERATURE (DRIVING ONE I/O $V_{L\_}$)



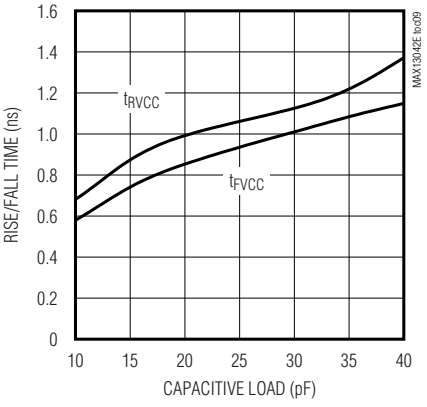
V_L SUPPLY CURRENT vs. CAPACITIVE LOAD ON I/O $V_{L\_}$ (DRIVING ONE I/O $V_{CC\_}$)



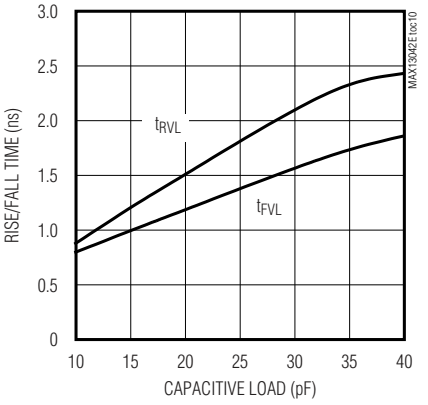
V_{CC} SUPPLY CURRENT vs. CAPACITIVE LOAD ON I/O $V_{CC\_}$ (DRIVING ONE I/O $V_{L\_}$)



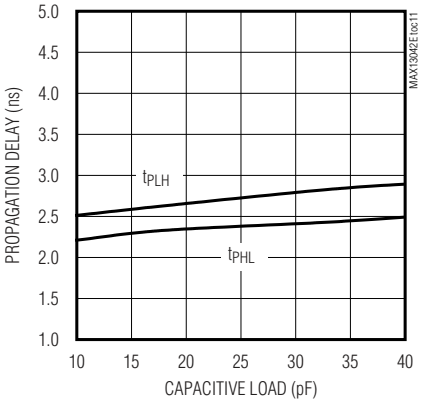
RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O $V_{CC\_}$ (DRIVING I/O $V_{L\_}$)



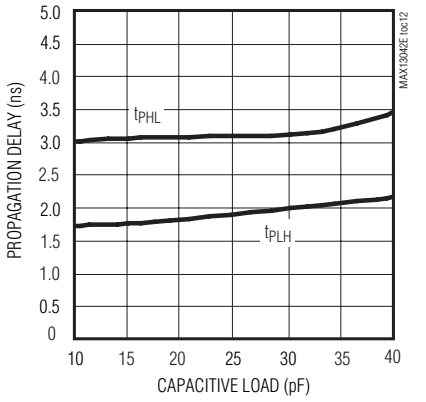
RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O $V_{L\_}$ (DRIVING I/O $V_{CC\_}$)



PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O $V_{CC\_}$ (DRIVING I/O $V_{L\_}$)



PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O $V_{L\_}$ (DRIVING I/O $V_{CC\_}$)

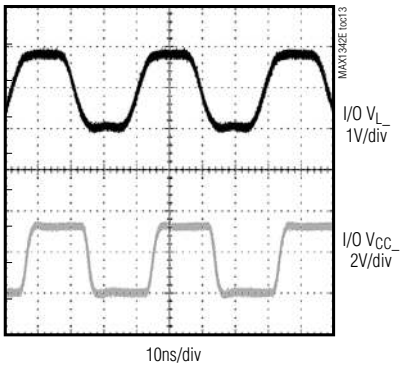


1.62V to 3.6V Improved High-Speed LLT

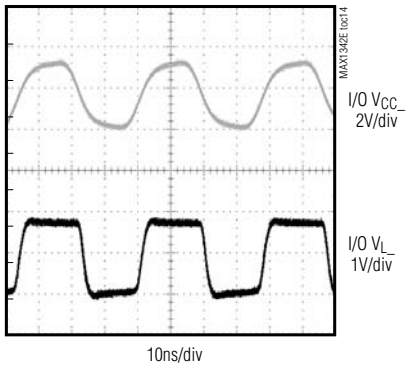
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, V_L = 1.8V, $C_{IOVCC\_}$ = 10pF, $C_{IOVL\_}$ = 15pF, R_{SOURCE} = 150Ω, data rate = 100Mbps, push-pull driver, T_A = +25°C, unless otherwise noted.)

TYPICAL I/O $V_{L\_}$ DRIVING (FREQUENCY = 26MHz, $C_{IOVCC\_}$ = 40pF)



TYPICAL I/O $V_{CC\_}$ DRIVING (FREQUENCY = 26MHz, $C_{IOVL\_}$ = 15pF)



Pin Description

PIN		NAME	FUNCTION
UCSP	TDFN		
A1	8	I/O V_{CC}4	Input/Output 4. Referenced to V_{CC}.
A2	10	I/O V_{CC}3	Input/Output 3. Referenced to V_{CC}.
A3	12	I/O V_{CC}2	Input/Output 2. Referenced to V_{CC}.
A4	14	I/O V_{CC}1	Input/Output 1. Referenced to V_{CC}.
B1	9	V_{CC}	Power-Supply Voltage, +2.2V to +3.6V. Bypass V_{CC} to GND with a 0.1µF ceramic capacitor. For full ESD protection, connect an additional 1µF ceramic capacitor from V_{CC} to GND as close to the V_{CC} input as possible.
B2	6	V_L	Logic Supply Voltage, +1.62V to +3.2V. Bypass V_L to GND with a 0.1µF ceramic capacitor placed as close to the device as possible.
B3	2	EN	Enable Input. Drive EN to GND for shutdown mode, or drive EN to V_L or V_{CC} for normal operation.
B4	13	GND	Ground
C1	7	I/O V_L4	Input/Output 4. Referenced to V_L.
C2	5	I/O V_L3	Input/Output 3. Referenced to V_L.
C3	3	I/O V_L2	Input/Output 2. Referenced to V_L.
C4	1	I/O V_L1	Input/Output 1. Referenced to V_L.
—	4, 11	N.C.	No Connection. Leave N.C. unconnected.
—	EP	EP	Exposed Pad. Connect exposed pad to GND.

Test Circuits/Timing Diagrams

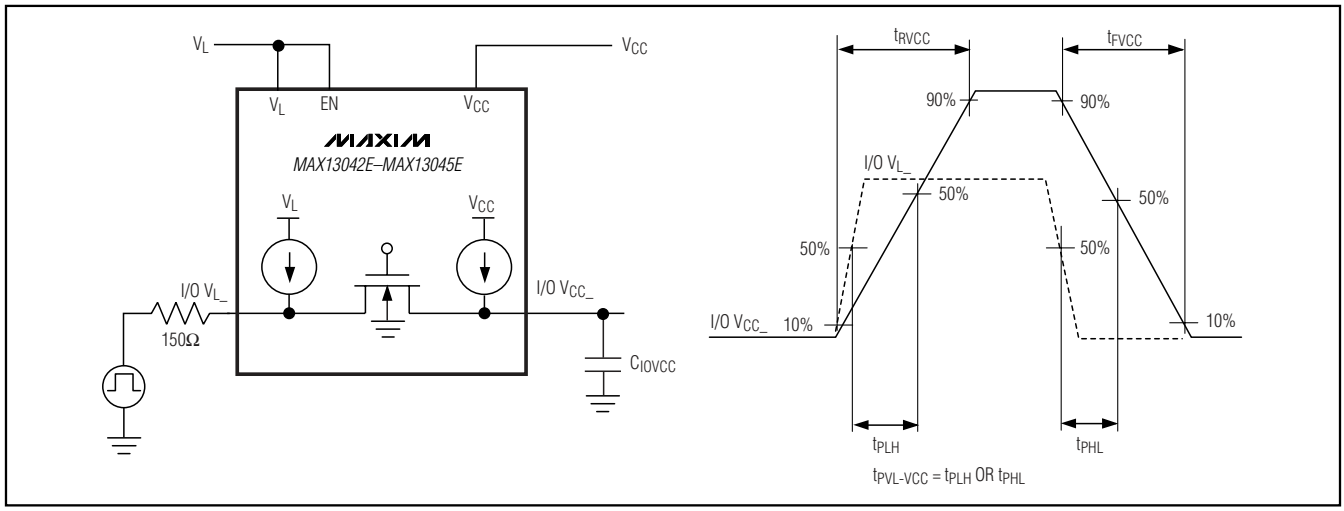


Figure 1. Push-Pull Driving I/O $V_{L\_}$ Test Circuit and Timing

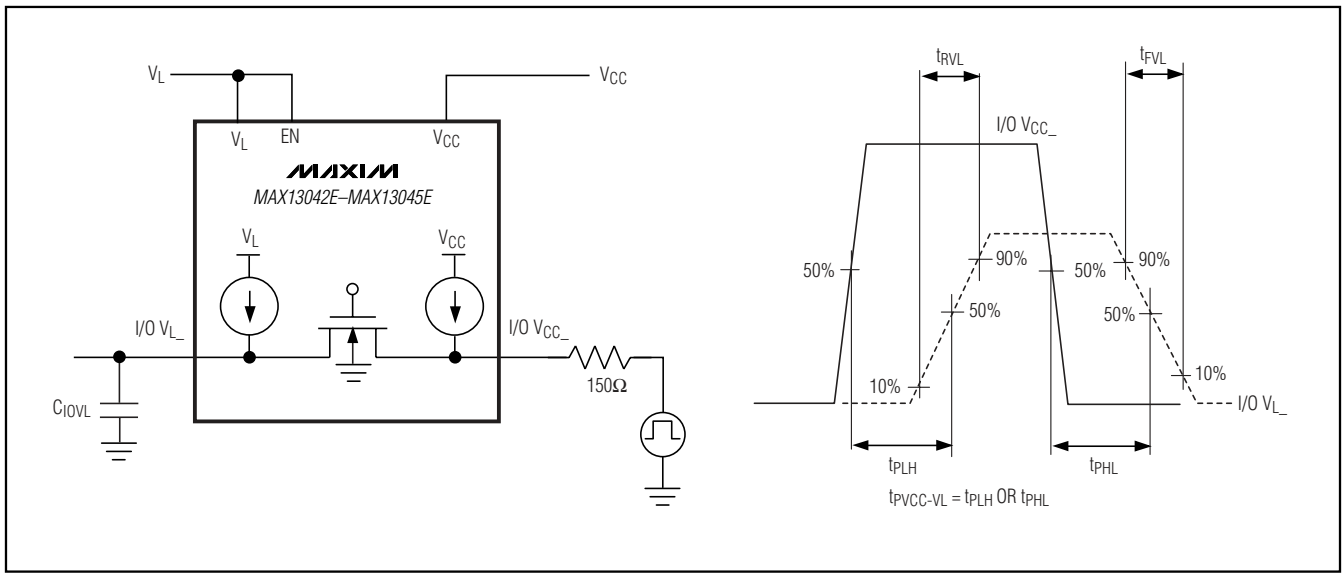


Figure 2. Push-Pull Driving I/O $V_{CC\_}$ Test Circuit and Timing

1.62V to 3.6V Improved High-Speed LLT

Test Circuits/Timing Diagrams (continued)

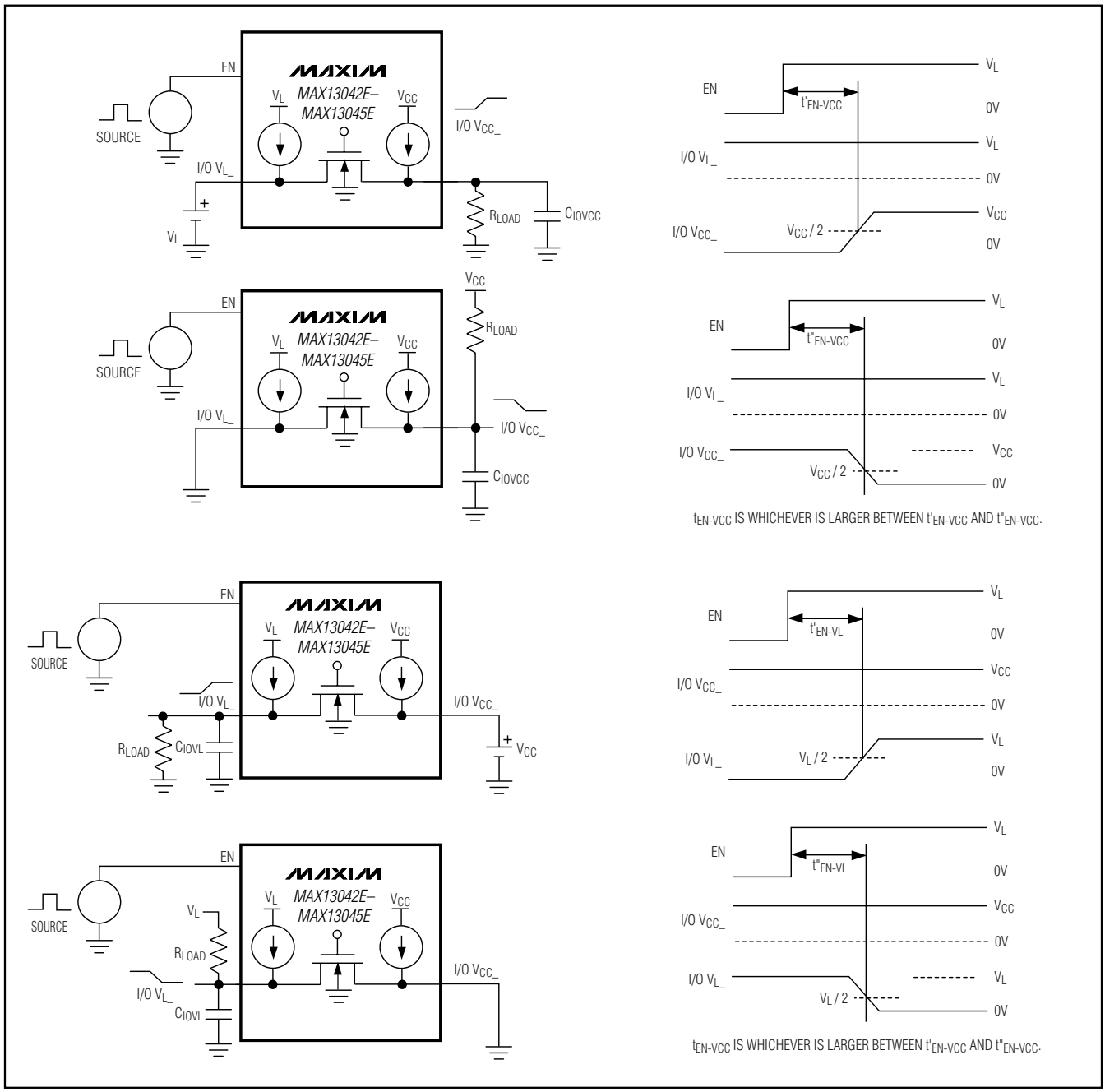
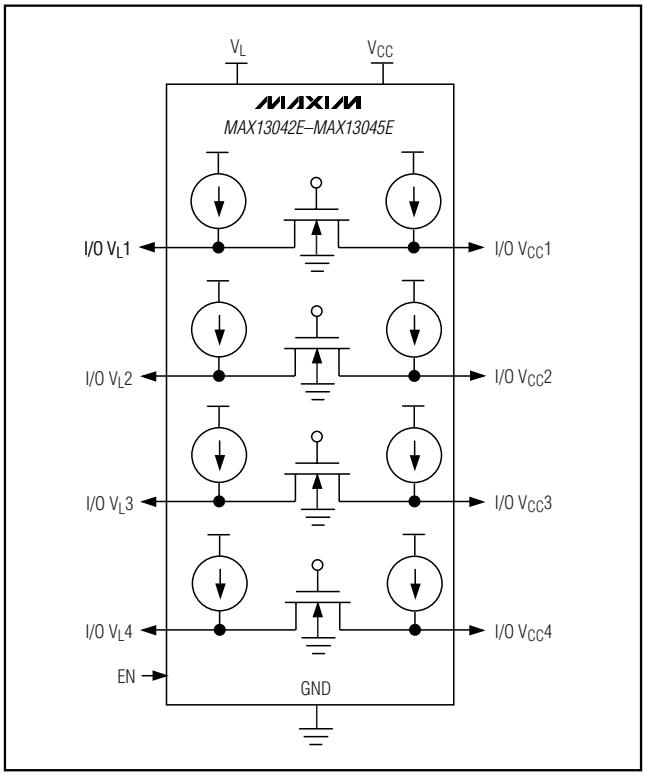


Figure 3. Enable Test Circuit and Timing

Functional Diagram



Detailed Description

The MAX13042E–MAX13045E 4-channel, bidirectional level translators provide the level shifting necessary for 100Mbps data transfer in multivoltage systems. The MAX13042E–MAX13045E are ideally suited for level translation in systems with four channels. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. Logic signals present on the V_L side of the device appear as a high-voltage logic signal on the V_{CC} side of the device and vice-versa.

The MAX13042E–MAX13045E operate at full speed with external drivers that source as little as 4mA output current. Each I/O channel is pulled up to V_{CC} or V_L by an internal 30µA current source, allowing the MAX13042E–MAX13045E to be driven by either push-pull or open-drain drivers.

The MAX13042E–MAX13045E feature an enable (EN) input that places the devices into a low-power shutdown mode when driven low. The MAX13042E–MAX13045E feature an automatic shutdown mode that disables the part when V_{CC} is less than V_L. The state of I/O $V_{CC\_}$ and I/O $V_{L\_}$ during shutdown is chosen by selecting the appropriate part version (see the *Ordering Information/ Selector Guide*).

The MAX13042E–MAX13045E operate with V_{CC} voltages from +2.2V to +3.6V and V_L voltages from +1.62V to +3.2V.

Level Translation

For proper operation, ensure that $+2.2V \le V_{CC} \le +3.6V$, $+1.62V \le V_L \le V_{CC} - 0.2V$. When power is supplied to V_L while V_{CC} is missing or less than V_L, the MAX13042E–MAX13045E automatically enter a low-power mode. The devices will also enter shutdown mode when EN = 0V. This allows V_{CC} to be disconnected and still have a known state on I/O $V_{L\_}$. The maximum data rate depends heavily on the load capacitance (see the Rise/Fall Time vs. Capacitive Load graphs in the *Typical Operating Characteristics*), output impedance of the driver, and the operating voltage range.

Input Driver Requirements

The MAX13042E–MAX13045E architecture is based on an nMOS pass gate and output accelerator stages (Figure 6). The accelerators are active only when there is a rising/falling edge on a given I/O. A short pulse is then generated where the output accelerator stages become active and charge/discharge the capacitances at the I/Os. Due to its architecture, both input stages become active during the one-shot pulse. This can lead to current feeding into the external source that is driving the translator. However, this behavior helps to speed up the transition on the driven side.

The MAX13042E–MAX13045E have internal current sources capable of sourcing 30µA to pull up the I/O lines. These internal-pullup current sources allow the inputs to be driven with open-drain drivers as well as push-pull drivers. It is not recommended to use external pullup resistors on the I/O lines. The architecture of the MAX13042E–MAX13045E permits either side to be driven with a minimum of 4mA drivers or larger.

Output Load Requirements

The MAX13042E–MAX13045E I/O are designed to drive CMOS inputs. Do not load the I/O lines with a resistive load less than 25kΩ and do not place an RC circuit at the input of these devices to slow down the edges. If a slower rise/fall time is required, refer to the MAX3000E/ MAX3001E logic-level translator data sheet.

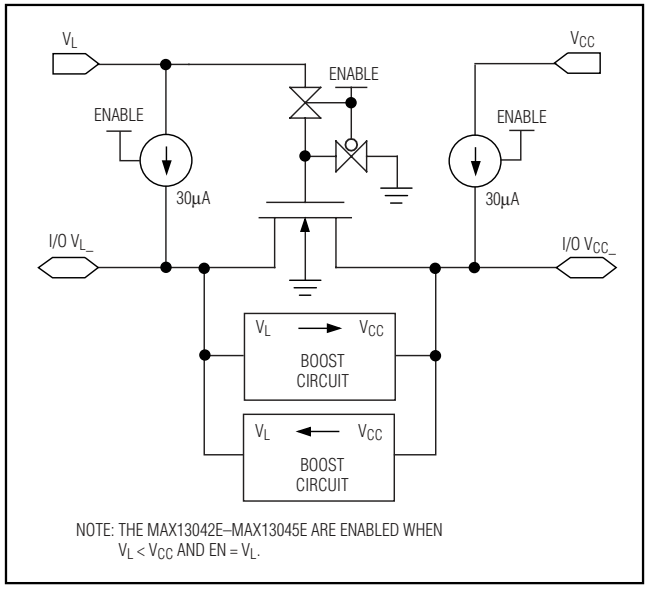


Figure 4. Simplified Functional Diagram for One I/O Line

Shutdown Mode

The MAX13042E–MAX13045E feature an enable (EN) input that places the devices into a low-power shutdown mode when driven low. The MAX13042E–MAX13045E feature an automatic shutdown mode that disables the part when V_{CC} is unconnected or less than V_L.

Applications Information

Layout Recommendations

Use standard high-speed layout practices when laying out a board with the MAX13042E–MAX13045E. For example, to minimize line coupling, place all other signal lines not connected to the MAX13042E–MAX13045E at least 1x the substrate height of the PCB away from the input and output lines of the MAX13042E–MAX13045E.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_L and V_{CC} to ground with 0.1µF ceramic capacitors. Place all capacitors as close to the power-supply inputs as possible. For full ESD protection, bypass V_{CC} with a 1µF ceramic capacitor located as close to the V_{CC} input as possible.

Unidirectional vs. Bidirectional Level Translator

The MAX13042E–MAX13045E bidirectional level translators can operate as a unidirectional device to translate signals without inversion. These devices provide the smallest solution (UCSP package) for unidirectional level translation without inversion.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Use with External Pullup/ Pulldown Resistors

Due to the architecture of the MAX13042E–MAX13045E, it is not recommended to use external pullup or pulldown resistors on the bus. In certain applications, the use of external pullup or pulldown resistors is desired to have a known bus state when there is no active driver on the bus. The MAX13042E–MAX13045E include internal pullup current sources that set the bus state when the device is enabled. In shutdown mode, the state of I/O V_{CC}_ and I/O V_L_ is dependent on the selected part version (see the *Ordering Information/Selector Guide*).

Open-Drain Signaling

The MAX13042E–MAX13045E are designed to pass open-drain as well as CMOS push-pull signals. When used with open-drain signaling, the rise time will be dominated by the interaction of the internal pullup current source and the parasitic load capacitance. The MAX13042E–MAX13045E include internal rise-time accelerators to speed up transitions, eliminating any need for external pullup resistors. For applications such as I^2C or 1-wire that require an external pullup resistor, please consult the MAX3378E and MAX3396E data sheets.

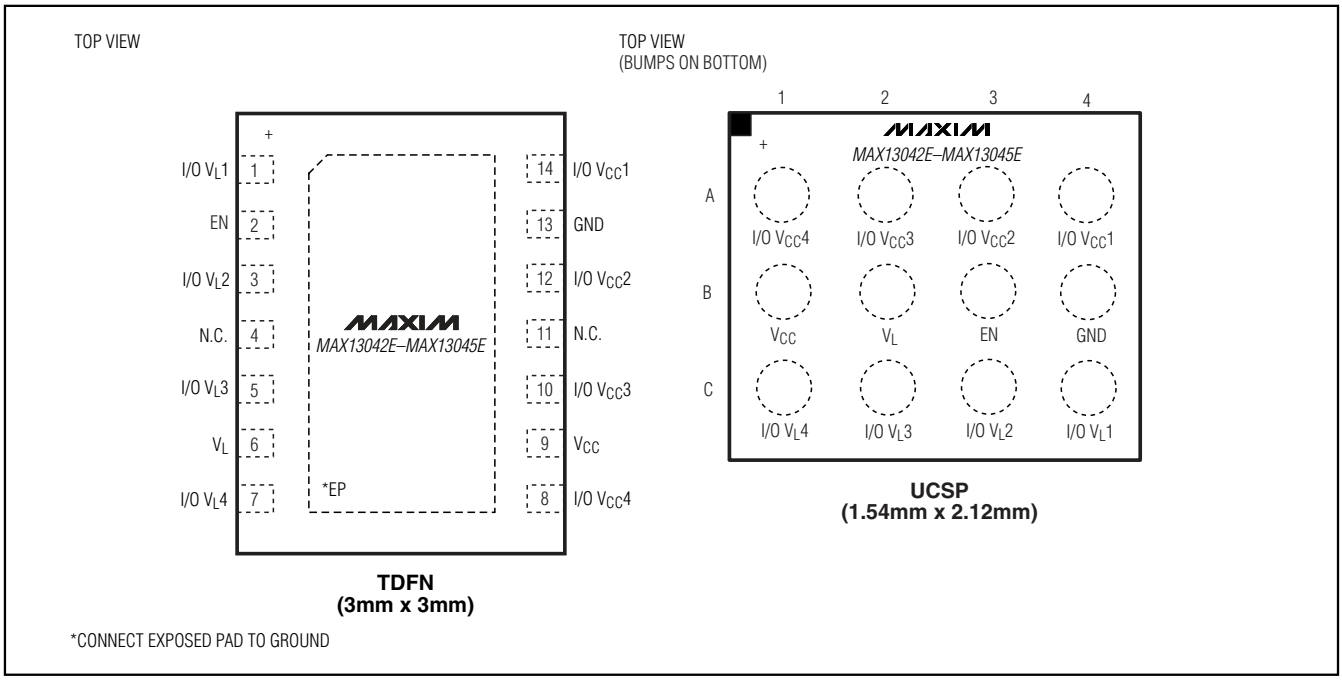
UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profiles, as well as the latest information on reliability testing results, go to Maxim's website at www.maxim-ic.com/ucsp to find the Application Note: *UCSP – A Wafer-Level Chip-Scale Package.*

Chip Information

PROCESS: BiCMOS

Pin Configurations



Ordering Information/Selector Guide (continued)

PART	PIN-PACKAGE	I/O V_L_ STATE DURING SHUTDOWN	I/O V_{CC}_ STATE DURING SHUTDOWN	TOP MARK	PKG CODE
MAX13043EEBC+T	12 UCSP-12	High Impedance	16.5kΩ to GND	ADR	B12-3
MAX13043EETD+T	14 TDFN-EP**	High Impedance	16.5kΩ to GND	ADF	T1433-2
MAX13044EEBC+T*	12 UCSP-12	16.5kΩ to GND	High Impedance	ADS	B12-3
MAX13044EETD+T*	14 TDFN-EP**	16.5kΩto GND	High Impedance	ADG	T1433-2
MAX13045EEBC+T*	12 UCSP-12	16.5kΩ to GND	16.5kΩ to GND	ADT	B12-3
MAX13045EETD+T*	14 TDFN-EP**	16.5kΩ to GND	16.5kΩ to GND	ADH	T1433-2

Note: *All devices operate over the -40°C to +85°C temperature range.*

+Denotes a lead-free package.

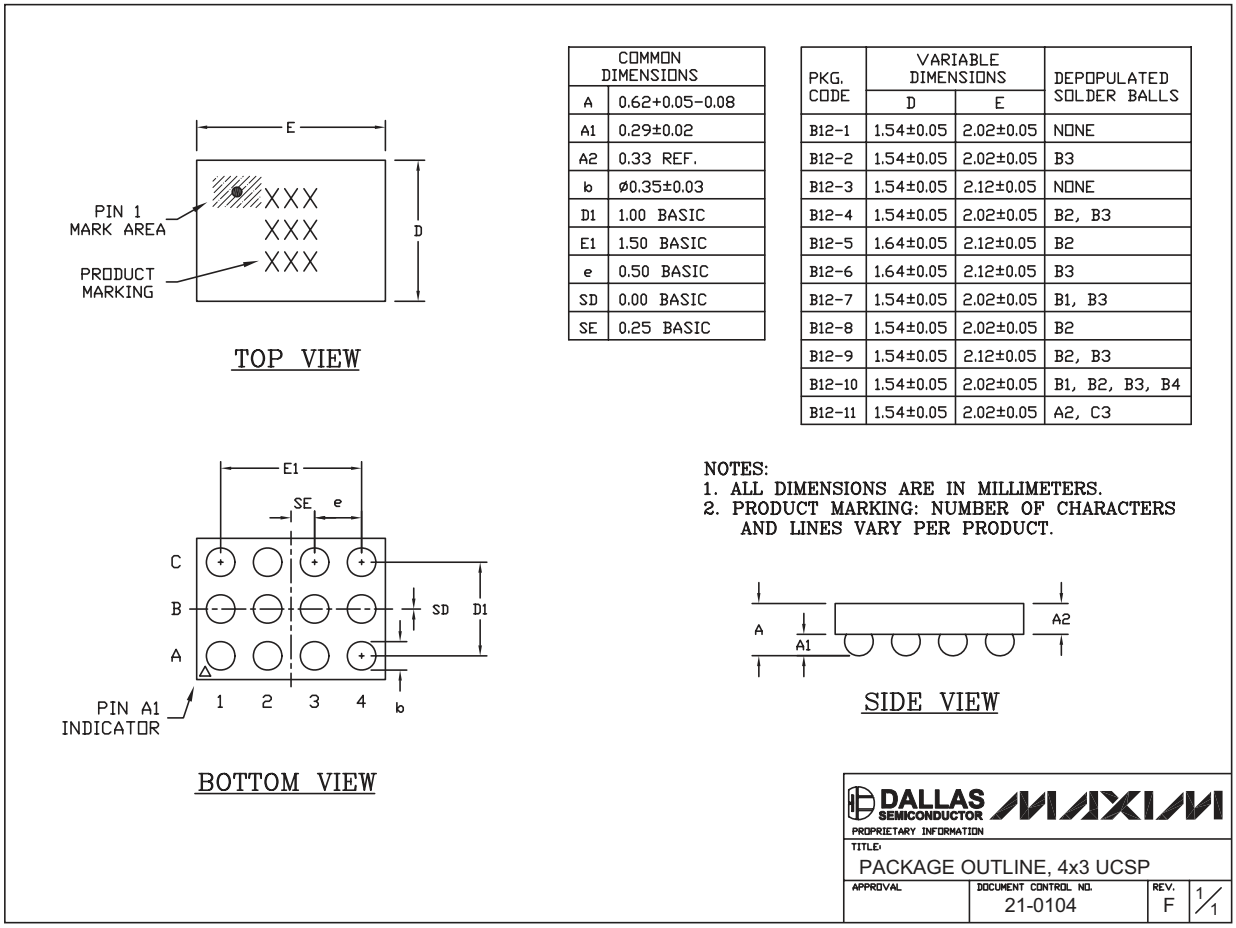
**Future product—contact factory for availability.*

***EP = Exposed paddle.*

1.62V to 3.6V Improved High-Speed LLT

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

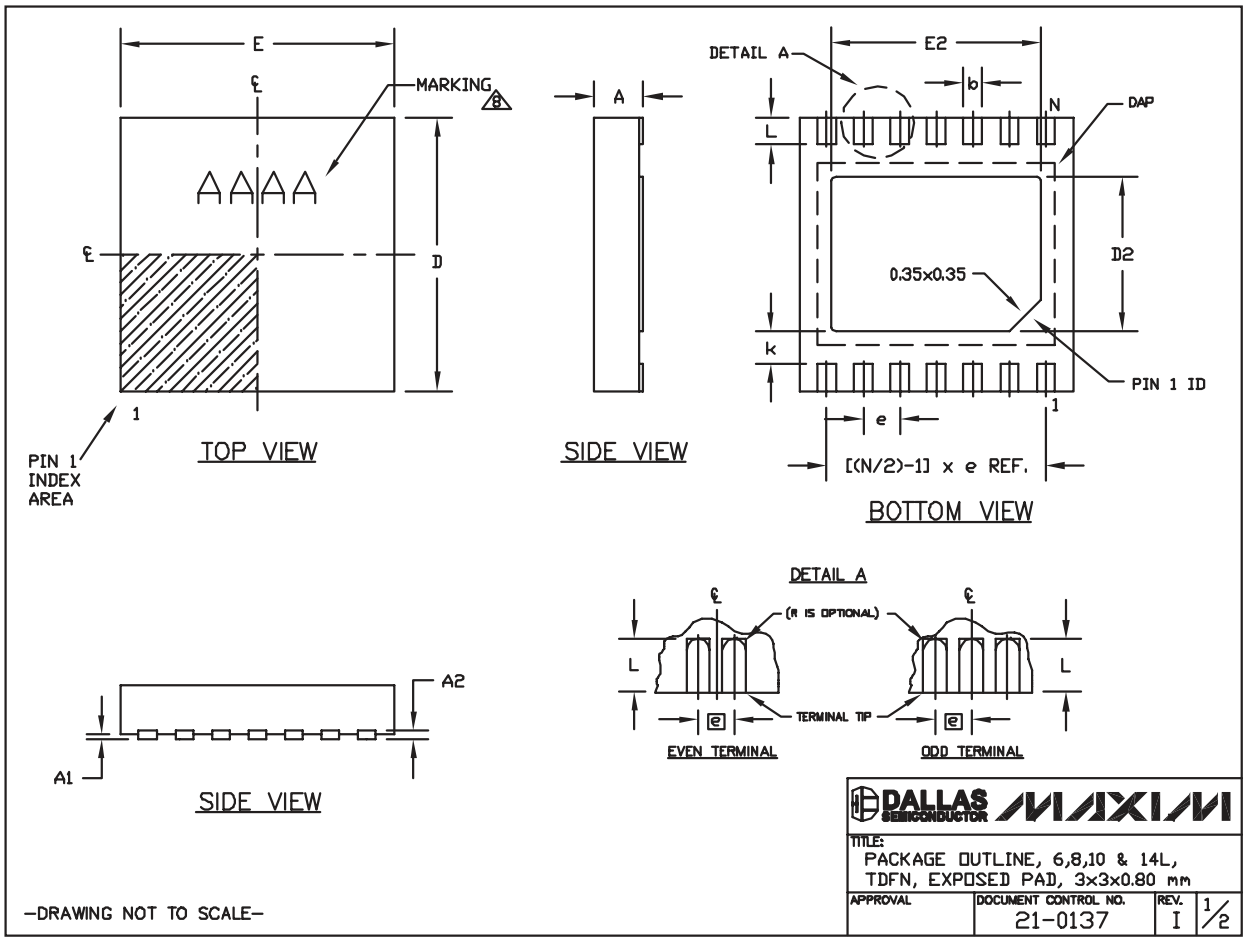


COMMON DIMENSIONS	
A	0.62±0.05–0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.00 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B12-1	1.54±0.05	2.02±0.05	NONE
B12-2	1.54±0.05	2.02±0.05	B3
B12-3	1.54±0.05	2.12±0.05	NONE
B12-4	1.54±0.05	2.02±0.05	B2, B3
B12-5	1.64±0.05	2.12±0.05	B2
B12-6	1.64±0.05	2.12±0.05	B3
B12-7	1.54±0.05	2.02±0.05	B1, B3
B12-8	1.54±0.05	2.02±0.05	B2
B12-9	1.54±0.05	2.12±0.05	B2, B3
B12-10	1.54±0.05	2.02±0.05	B1, B2, B3, B4
B12-11	1.54±0.05	2.02±0.05	A2, C3

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	I	2/2

–DRAWING NOT TO SCALE–