PTFA070601E
PTFA070601F

green Product

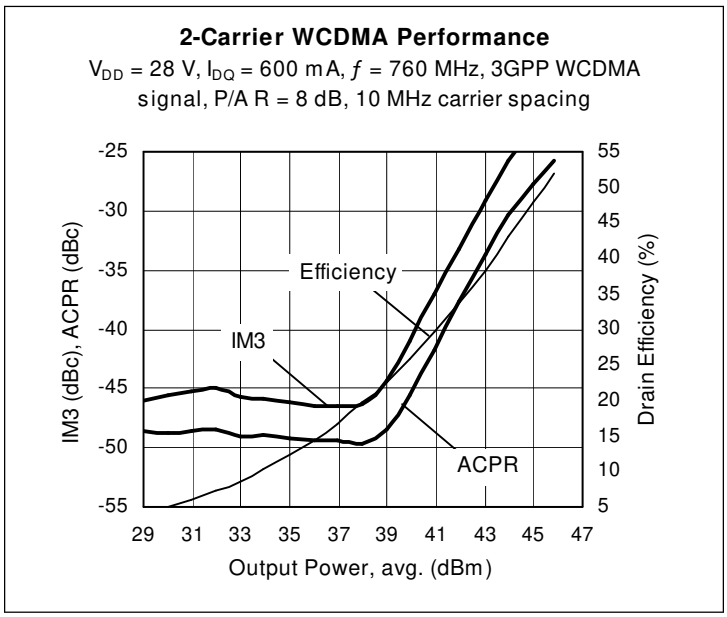
Thermally-Enhanced High Power RF LDMOS FETs
60 W, 725 – 770 MHz

Description

The PTFA070601E and PTFA070601F are 60-watt LDMOS FETs designed for cellular power amplifier applications in the 725 to 770 MHz band. Features include input matching and thermally-enhanced packages with slotted or earless flanges. Manufactured with Infineon's advanced LDMOS process, these devices provide excellent thermal performance and superior reliability.

PTFA070601E
Package H-36265-2

PTFA070601F
Package H-37265-2



Features

- Broadband internal matching
- Typical WCDMA performance, 760 MHz, 28 V
  - Average output power = 12 W
  - Gain = 19 dB
  - Efficiency = 29%
- Typical CW performance, 760 MHz, 28 V
  - Output power at P–1dB = 60 W
  - Gain = 19 dB
  - Efficiency = 72%
- Integrated ESD protection: Human Body Model, Class 2 (minimum)
- Excellent thermal stability, low HCI drift
- Capable of handling 10:1 VSWR @ 28 V, 60 W (CW) output power
- Pb-free and RoHS-compliant

RF Characteristics

WCDMA Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)
V_{DD} = 28 V, I_{DQ} = 600 mA, P_{OUT} = 12 W AVG, f = 760 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Intermodulation Distortion	IMD	—	–37	—	dBc
Gain	G_{ps}	—	19	—	dB
Drain Efficiency	η_D	—	29	—	%

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics (cont.)

Two-tone Measurements (tested in Infineon test fixture)

V_{DD} = 28 V, I_{DQ} = 600 mA, P_{OUT} = 60 W PEP, f = 760 MHz, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	18	19.5	—	dB
Drain Efficiency	η_D	46.5	48	—	%
Intermodulation Distortion	IMD	—	–31	–29	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 µA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10.0	µA
On-State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.15	—	Ω
Operating Gate Voltage	V_{DS} = 28 V, I_{DQ} = 600 mA	V_{GS}	2.0	2.3	3.0	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA

Maximum Ratings

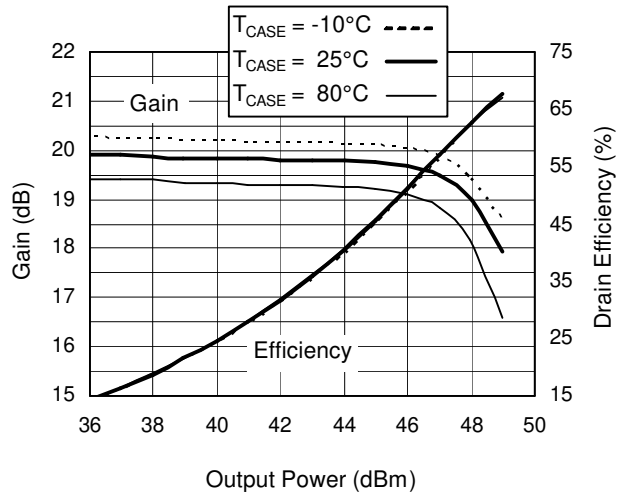
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–0.5 to +12	V
Junction Temperature	T_J	200	°C
Total Device Dissipation	P_D	219	W
Above 25°C derate by		1.25	W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 60 W CW)	$R_{\theta JC}$	0.8	°C/W

Ordering Information

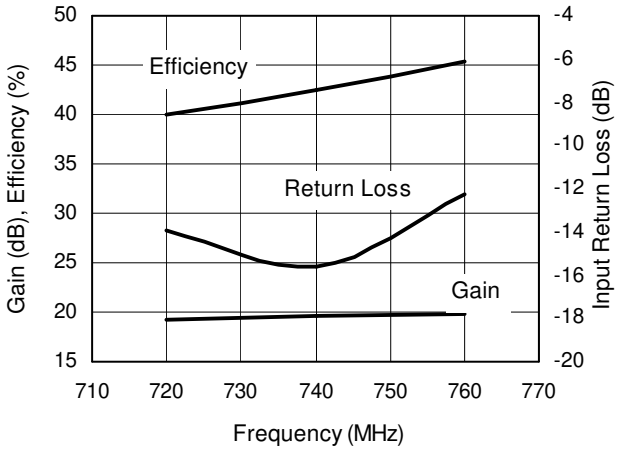
Type and Version	Package Outline	Package Description	Shipping	Marking
PTFA070601E V4	H-36265-2	Thermally-enhanced, slotted flange, single-ended	Tray	PTFA070601E
PTFA070601F V4	H-37265-2	Thermally-enhanced, earless flange, single-ended	Tray	PTFA070601F

Typical Performance (data taken in a production test fixture)

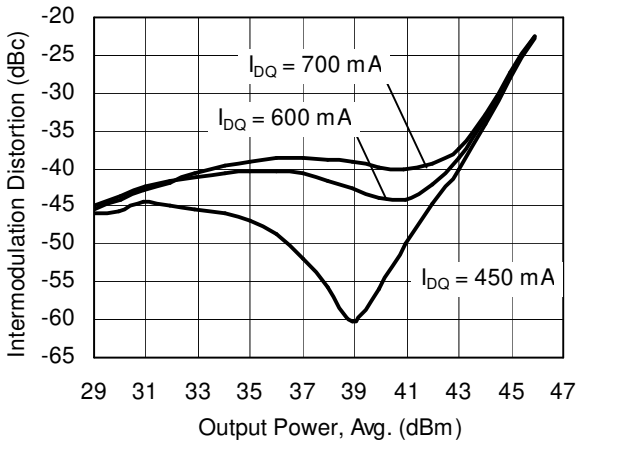
Power Sweep, CW Conditions
V_{DD} = 28 V, I_{DQ} = 600 mA, f = 760 MHz



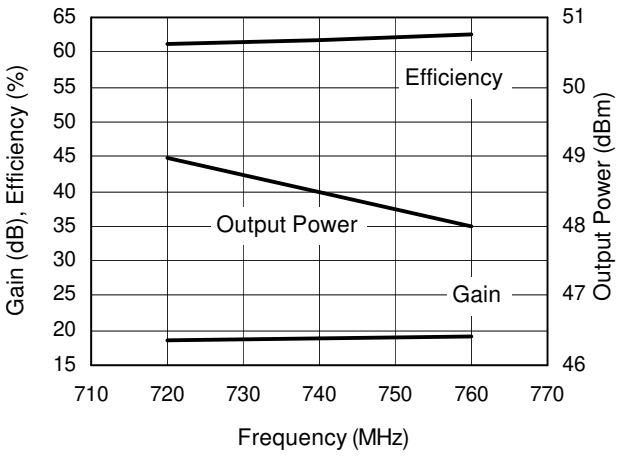
Broadband Performance
V_{DD} = 28 V, I_{DQ} = 600 mA, P_{OUT} = 45 dBm



IM3 vs. Output Power at Selected Biases
V_{DD} = 28 V, f = 760 MHz, tone spacing = 1 MHz

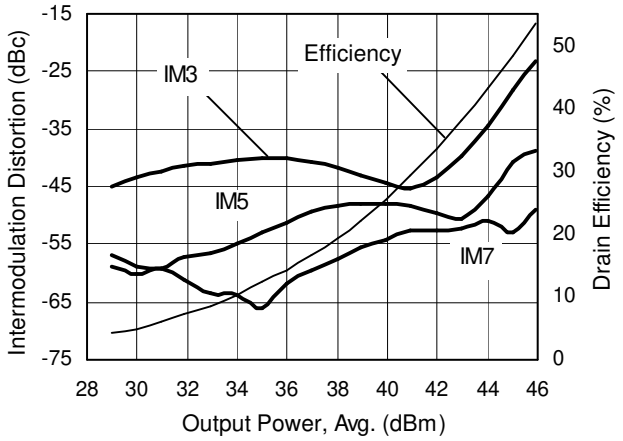


Broadband Performance (at P–1dB)
V_{DD} = 28 V, I_{DQ} = 600 mA

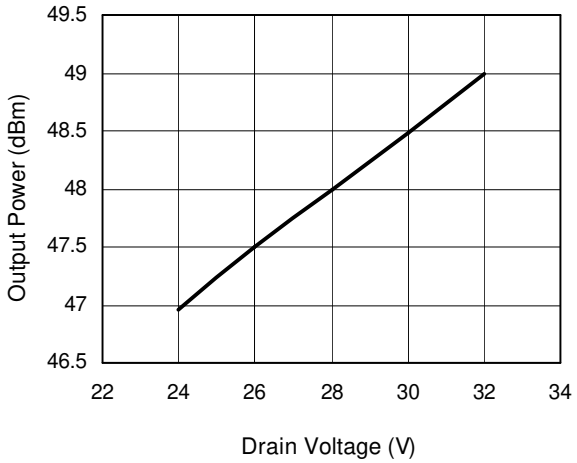


Typical Performance (cont.)

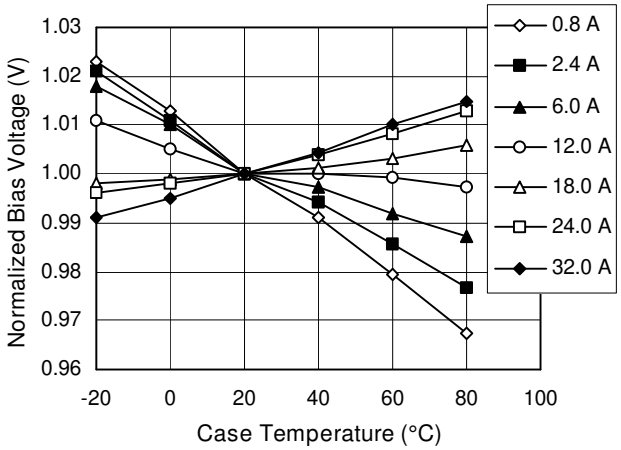
Intermodulation Distortion vs. Output Power
V_{DD} = 28 V, I_{DQ} = 600 mA,
f = 760 MHz, tone spacing = 1 MHz



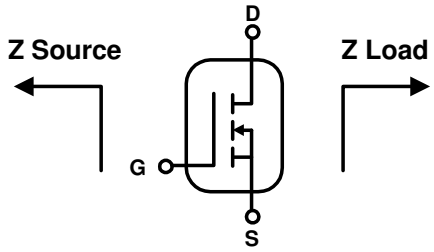
Output Power (P–1dB) **vs. Drain Voltage**
I_{DQ} = 600 mA, f = 760 MHz

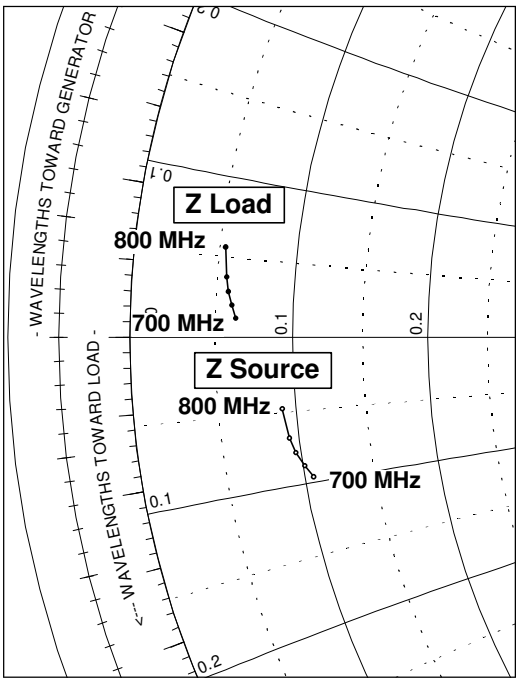


Bias Voltage vs. Temperature
Voltage normalized to typical gate voltage,
series show current



Broadband Circuit Impedance

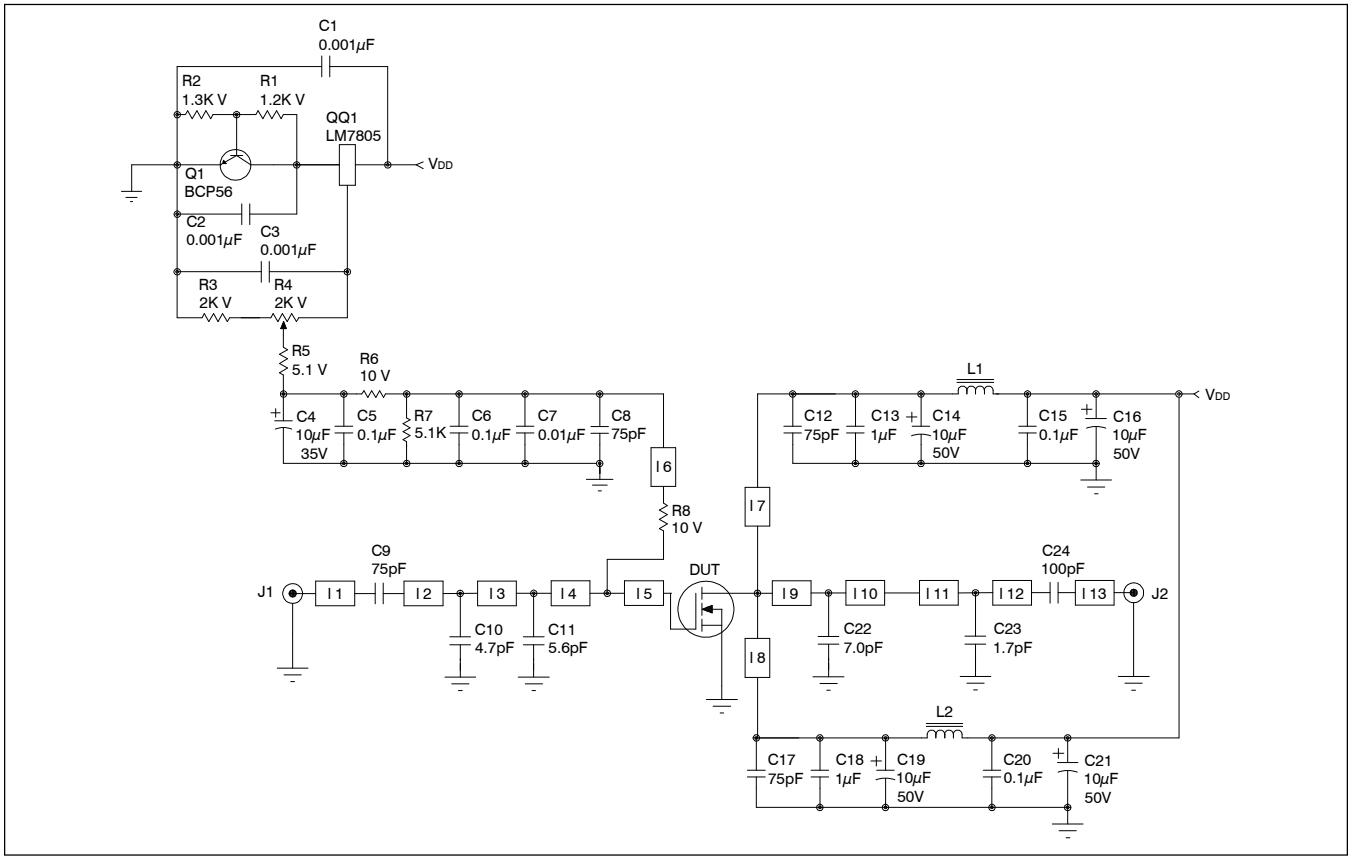




Frequency	Z Source Ω		Z Load Ω	
MHz	R	jX	R	jX
700	5.32	–4.82	3.14	0.61
720	5.07	–4.40	3.01	1.02
740	4.84	–3.91	2.88	1.44
760	4.69	–3.40	2.79	1.90
800	4.55	–2.39	2.69	2.82

See next page for circuit information

Reference Circuit

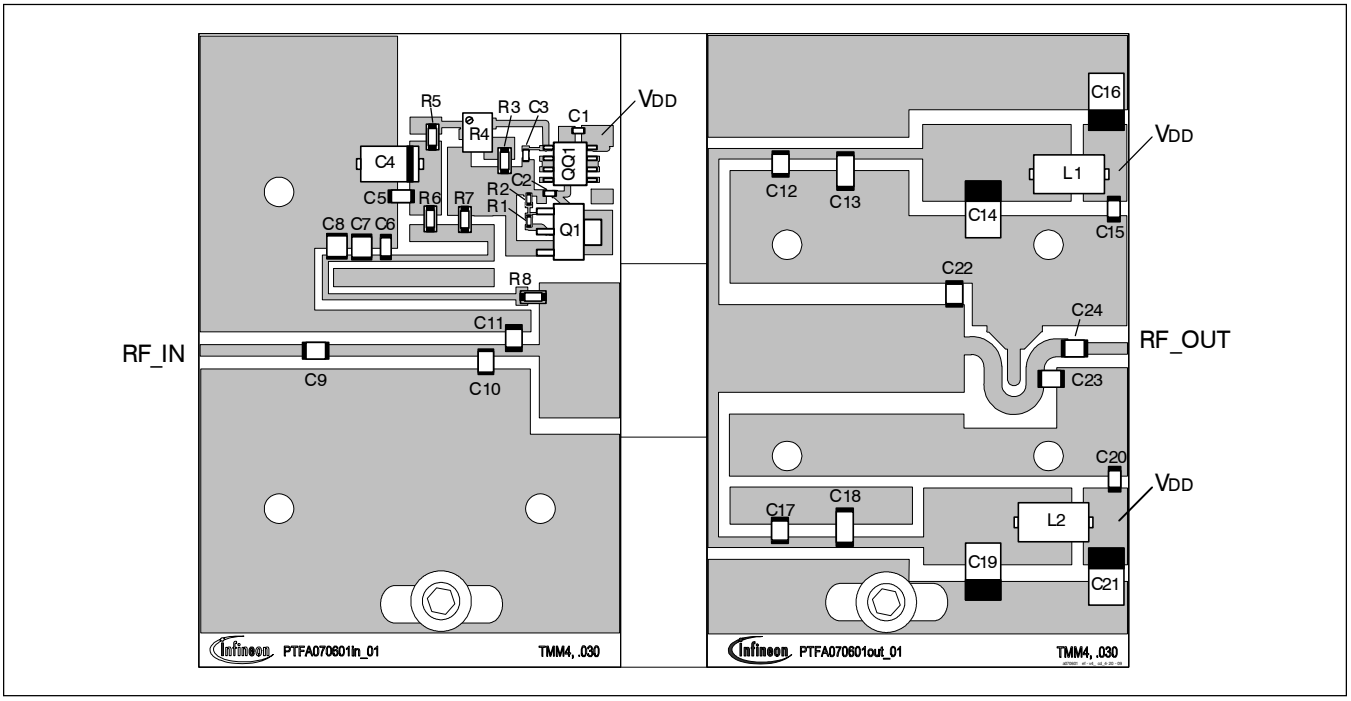


Reference circuit schematic diagram for ƒ = 760 MHz

Circuit Assembly Information			
DUT	PTFA070601E or PTFA070601F	LDMOS Transistor	
PCB	0.76 mm [.030"] thick, ε_r = 4.5	Rogers TMM4	2 oz. copper

Microstrip	Electrical Characteristics at 760 MHz	Dimensions: L x W (mm)	Dimensions: L x W (in.)
ℓ1	0.056 λ, 50.0 Ω	12.19 x 1.37	0.480 x 0.054
ℓ2	0.091 λ, 50.0 Ω	19.81 x 1.37	0.780 x 0.054
ℓ3	0.016 λ, 50.0 Ω	3.56 x 1.37	0.140 x 0.054
ℓ4	0.011 λ, 50.0 Ω	2.29 x 1.37	0.090 x 0.054
ℓ5	0.050 λ, 7.5 Ω	9.58 x 16.21	0.377 x 0.638
ℓ6	0.128 λ, 66.5 Ω	28.45 x 0.79	1.120 x 0.031
ℓ7, ℓ8	0.123 λ, 52.2 Ω	26.67 x 1.27	1.050 x 0.050
ℓ9	0.146 λ, 11.0 Ω	28.58 x 10.54	1.125 x 0.415
ℓ10	0.005 λ, 11.0 Ω	0.97 x 10.54	0.038 x 0.415
ℓ11	0.075 λ, 37.8 Ω	15.82 x 2.16	0.623 x 0.085
ℓ12	0.026 λ, 37.8 Ω	5.56 x 2.16	0.219 x 0.085
ℓ13	0.022 λ, 50.0 Ω	4.70 x 1.37	0.185 x 0.054

Reference Circuit (cont.)



Reference circuit schematic diagram for ƒ = 760 MHz

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 µF	Digi-Key	PCC1772CT-ND
C4	Tantalum capacitor, 10 µF, 35 V	Digi-Key	399-1655-2-ND
C5, C6, C15, C20	Capacitor, 0.1 µF	Digi-Key	PCC104BCT-ND
C7	Capacitor, 0.01 µF	ATC	200B 103
C8, C9, C12, C17	Ceramic capacitor, 75 pF	ATC	100B 750
C10	Ceramic capacitor, 4.7 pF	ATC	100B 4R7
C11	Ceramic capacitor, 5.6 pF	ATC	100B 5R6
C13, C18	Capacitor, 1.0 µF	ATC	920C105
C14, C16, C19, C21	Tantalum capacitor, 10 µF, 50 V	Garrett Electronics	TPSE106K050R0400
C22	Ceramic capacitor, 7.0 pF	ATC	100B 7R0
C23	Ceramic capacitor, 1.7 pF	ATC	100B 1R7
C24	Ceramic capacitor, 100 pF	ATC	100B 101
L1, L2	Ferrite, 8.9 mm	Elna Magnetics	BDS 4.6/3/8.9-4S2
Q1	Transistor	Infineon Technologies	BCP56
QQ1	Voltage regulator	National Semiconductor	LM7805
R1	Chip resistor 1.2k ohms	Digi-Key	P1.2KGCT-ND
R2	Chip resistor 1.3k ohms	Digi-Key	P1.3KGCT-ND
R3	Chip resistor 2k ohms	Digi-Key	P2KECT-ND
R4	Potentiometer 2k ohms	Digi-Key	3224W-202ETR-ND
R5, R7	Chip resistor 5.1k ohms	Digi-Key	P5.1KECT-ND
R6, R8	Chip resistor 10 ohms	Digi-Key	P10ECT-ND

**Gerber files for this circuit available on request*

Package Outline Specifications

Package H-36265-2

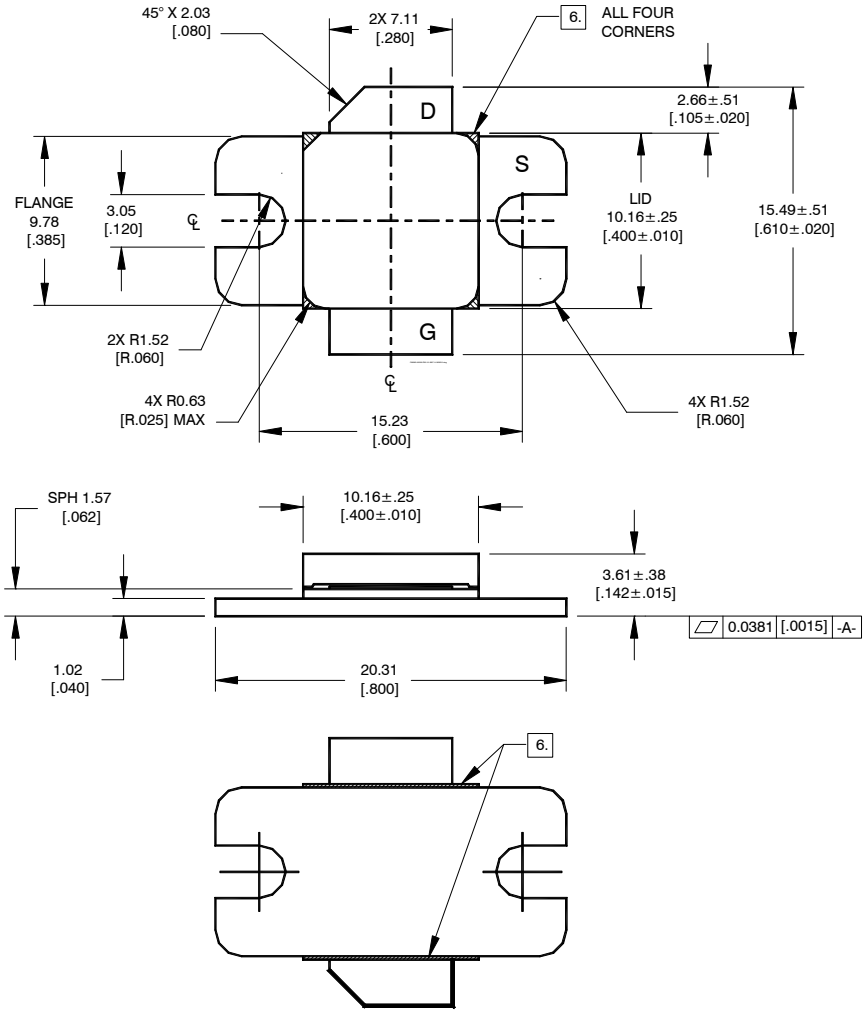
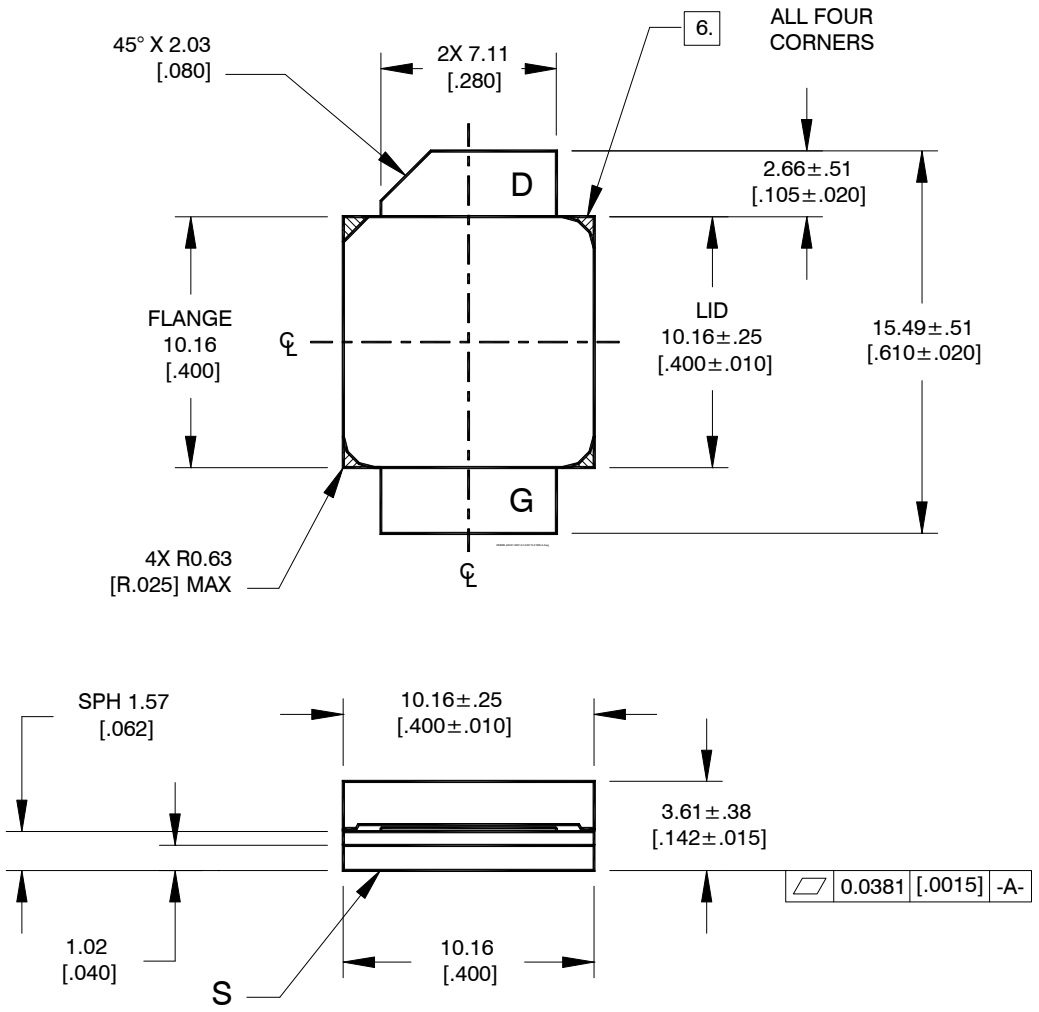


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. Pins: D = drain, S = source, G = gate.
4. Lead thickness: 0.10 +0.051/–0.025 [.004 +.002/–.001].
5. Gold plating thickness: 1.14 ± 0.38 micron [45 ± 15 microinch]
6. Exposed metal plane on top and bottom of ceramic insulator.
7. All tolerances ± 0.127 [.005] unless specified otherwise.

Package Outline Specifications (cont.)

Package H-37265-2



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PTFA0706010E/F

Revision History:	**2009-04-16**	Data Sheet
Previous Version:	None	
Page	Subjects (major changes since last revision)	

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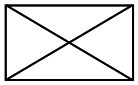

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